Ions4SET

# Ions4SET NEWSLETTER

**No. 1**
**May 2020**

Ions4SET is a running HORIZON 2020 project (GA-No. 688072) aimed to realize Single Electron Transistors (SETs) working at room temperature. The SET is based on a single Si quantum dot embedded in the oxide of a stacked $Si/SiO_2/Si$ gate-all-around nanopillar transistor and fabricated in a CMOS compatible process. Details are given at the corresponding homepage: http://www.ions4set.eu. The **NEWSLETTERS** inform in a concise form about main project results; given references provide more detailed information.

## Fabrication of vertically stacked $Si/SiO_2/Si$ nanopillars of 10 nm diameter

### Why, and how do we target so small dimensions?

SETs are devices with a very low power consumption, especially interesting for the Internet of Things market. The SET physics is based on tunnelling effect through a quantum dot between the source and drain of a gate-all-around nanopillar transistor, and typical Coulomb-blockade oscillations are observed on IV plots. Those devices can work at room temperatures and low voltages if the dimension of nanopillar and quantum dot are in the nanometer range [1]. From device simulations for various pillar geometries and dot sizes [2], as shown for the pillar diameter in **Fig. 1**, we were able to define main targeted dimensions of the stacked nanopillars (see **Fig. 2**).

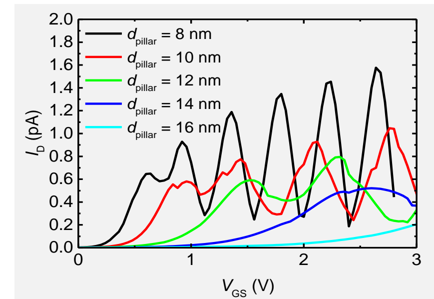


*Fig. 1: Simulated current-voltage plots with different pillar diameters.*

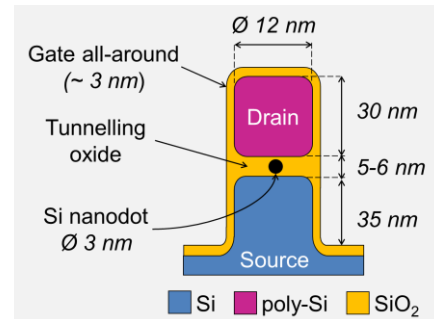


*Fig. 2: Targeted dimensions.*

**References:**

[1] X. Chen et al., "A model for energy quantization of single-electron transistor below 10nm", IEEE Int. Conf. ASIC, pp. 531–534 (2011)

[2] F. J. Klüpfel, "A Compact Model Based on Bardeen's Transfer Hamiltonian Formalism for Silicon Single Electron Transistors", IEEE Access **7**, 84053 (2019)

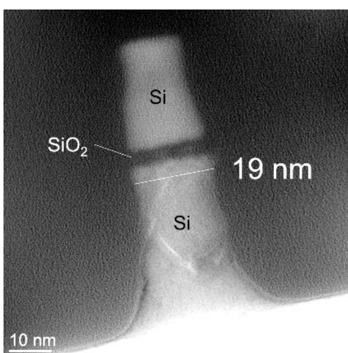


*Fig. 3: EFTEM image of a $Si/SiO_2/Si$ stacked nanopillar after e-beam lithography and reactive ion etching patterning process.*

### How do we fabricate such pillars?

CMOS compatible processes using ∅ 200-mm Si wafers and industrial equipment ensure high throughput and maturity. The process flow combines electron-beam lithography with dry reactive ion etching. A tri-layer stack of SOC/SiARC/resist has been selected for lithography and etching of the $Si/SiO_2/Si$ nanopillars. In addition, isotropic resist trimming before etching is used to further reduce the pillar dimeter [3]. This process allows to fabricate nanopillars close to 20 nm diameter with an aspect ratio of about 4:1 (**Fig. 3**).

**Reference:**

[3] M.-L. Pourteau et al., "Sub-20 nm multilayer nanopillar patterning for hybrid SET/CMOS integration", Microelectr. Engin. 2020 (in print)

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## What is the reproducibility of this process?

There are two ways of evaluating the reproducibility of a process. First, we verify its uniformity among all the dies of one ∅ 200 mm wafer by CD-SEM. The pillar diameter 3σ is 2.5 nm, meaning that 99.9% of the nanopillars have a critical dimension between 23.9 nm and 28.9 nm [3]. We also assessed the reproducibility between several wafers processed by the same process. **Fig. 4** shows the average diameter +/- 3σ for each wafer. The 3σ values of all the measurements for all wafers (15 points/ wafer) were determined to be 3.4 nm for the smallest pattern (CD30).

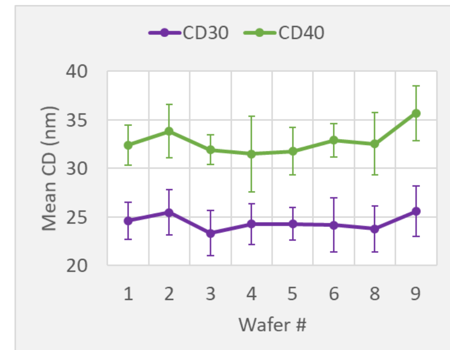


***Fig. 4**: CD after etching of two pillar sizes, for wafers of the same lot.*

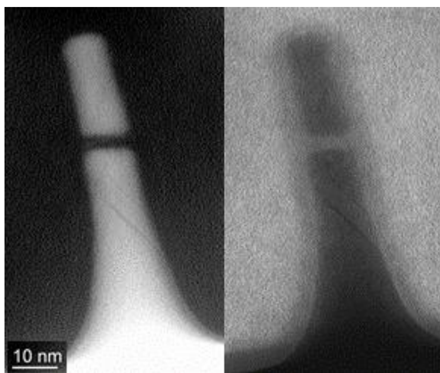


***Fig. 5**: EFTEM images (left: Si plasmon, right: $SiO_2$ plasmon) of a 10 nm stacked $Si/SiO_2/Si$ nanopillar with all-around oxide after double plasma oxidation.*

## How can we further reduce the pillar size?

By e-beam lithography and reactive ion etching nanopillars of ~ 20 nm diameter can be achieved with high yield, but this is still above the targeted value (≤ 12 nm). For further reduction, sacrificial oxidation of the pillars is applied which consumes a fraction of the Si at its surface. Subsequent removal of the oxide by diluted HF will reduce the pillar diameter. Low-temperature plasma oxidation (<400°C) [4] ensures the stability of the Si quantum dot in the oxide. By this means, nanopillars down to 10 nm diameter have been reliably fabricated (see **Fig. 5**).

**Reference:**

[4] W. Lerch et al.; "Low-temperature microwave-based plasma oxidation of Ge and Si", ECS Trans. **72**, 101 (2016).

## How do we form Si quantum dots within the pillars?

SET functionality requires the presence of a Si quantum dot in the intermediated oxide within tunnelling distances to the neighboured drain/ source regions of the stacked nanopillar. We used a Si nanodot self-assembly process, based on phase separation of a confined $SiO_x$ volume and subsequent Ostwald ripening during annealing [5]. An example of a stacked nanopillar with a single Si nanodot embedded in the oxide is shown in **Fig. 6**. Detailed information about this process will be given in the next Ions4SET Newsletter in June 2020. Stay curious.

**Reference:**

[5] X. Xu et al.; "Site-controlled formation of single Si nanocrystals in a buried $SiO_2$ matrix using ion beam mixing", Beilstein J. Nanotechn. **9**, 2883 (2018).

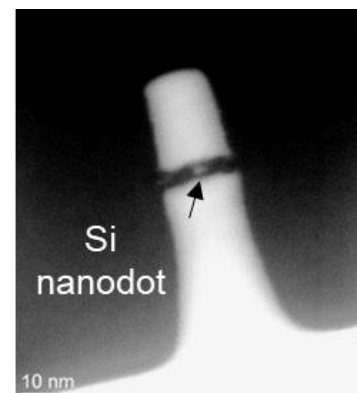


***Fig. 6**: EFTEM image of a stacked $Si/SiO_2/Si$ nanopillar with a single Si QD embedded in the oxide.*

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