Ions4SET is a running HORIZON 2020 project (GA-No. 688072) aimed to realize Single Electron Transistors (SETs) working at room temperature. The SET is based on a single Si quantum dot embedded in the oxide of a stacked Si/SiO$_2$/Si gate-all-around nanopillar transistor and fabricated in a CMOS compatible process. Details are given at the corresponding homepage: http://www.ions4set.eu. The NEWSLETTERS inform in a concise form about main project results; given references provide more detailed information.

Why, and how do we target so small dimensions?

SETs are devices with a very low power consumption, especially interesting for the Internet of Things market. The SET physics is based on tunnelling effect through a quantum dot between the source and drain of a gate-all-around nanopillar transistor, and typical Coulomb-blockade oscillations are observed on IV plots. Those devices can work at room temperatures and low voltages if the dimension of nanopillar and quantum dot are in the nanometer range [1]. From device simulations for various pillar geometries and dot sizes [2], as shown for the pillar diameter in Fig. 1, we were able to define main targeted dimensions of the stacked nanopillars (see Fig. 2).

References:

How do we fabricate such pillars?

CMOS compatible processes using ø 200-mm Si wafers and industrial equipment ensure high throughput and maturity. The process flow combines electron-beam lithography with dry reactive ion etching. A tri-layer stack of SOC/SiARC/resist has been selected for lithography and etching of the Si/SiO$_2$/Si nanopillars. In addition, isotropic resist trimming before etching is used to further reduce the pillar diameter [3]. This process allows to fabricate nanopillars close to 20 nm diameter with an aspect ratio of about 4:1 (Fig. 3).

Reference:
What is the reproducibility of this process?

There are two ways of evaluating the reproducibility of a process. First, we verify its uniformity among all the dies of one 200 mm wafer by CD-SEM. The pillar diameter 3σ is 2.5 nm, meaning that 99.9% of the nanopillars have a critical dimension between 23.9 nm and 28.9 nm [3]. We also assessed the reproducibility between several wafers processed by the same process. Fig. 4 shows the average diameter +/- 3σ for each wafer. The 3σ values of all the measurements for all wafers (15 points/wafer) were determined to be 3.4 nm for the smallest pattern (CD30).

How can we further reduce the pillar size?

By e-beam lithography and reactive ion etching nanopillars of ~20 nm diameter can be achieved with high yield, but this is still above the targeted value (≤12 nm). For further reduction, sacrificial oxidation of the pillars is applied which consumes a fraction of the Si at its surface. Subsequent removal of the oxide by diluted HF will reduce the pillar diameter. Low-temperature plasma oxidation (<400°C) [4] ensures the stability of the Si quantum dot in the oxide. By this means, nanopillars down to 10 nm diameter have been reliably fabricated (see Fig. 5).

Reference:

How do we form Si quantum dots within the pillars?

SET functionality requires the presence of a Si quantum dot in the intermediated oxide within tunnelling distances to the neighboured drain/source regions of the stacked nanopillar. We used a Si nanodot self-assembly process, based on phase separation of a confined SiOx volume and subsequent Ostwald ripening during annealing [5]. An example of a stacked nanopillar with a single Si nanodot embedded in the oxide is shown in Fig. 6. Detailed information about this process will be given in the next Ions4SET Newsletter in June 2020. Stay curiosus.

Reference:

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