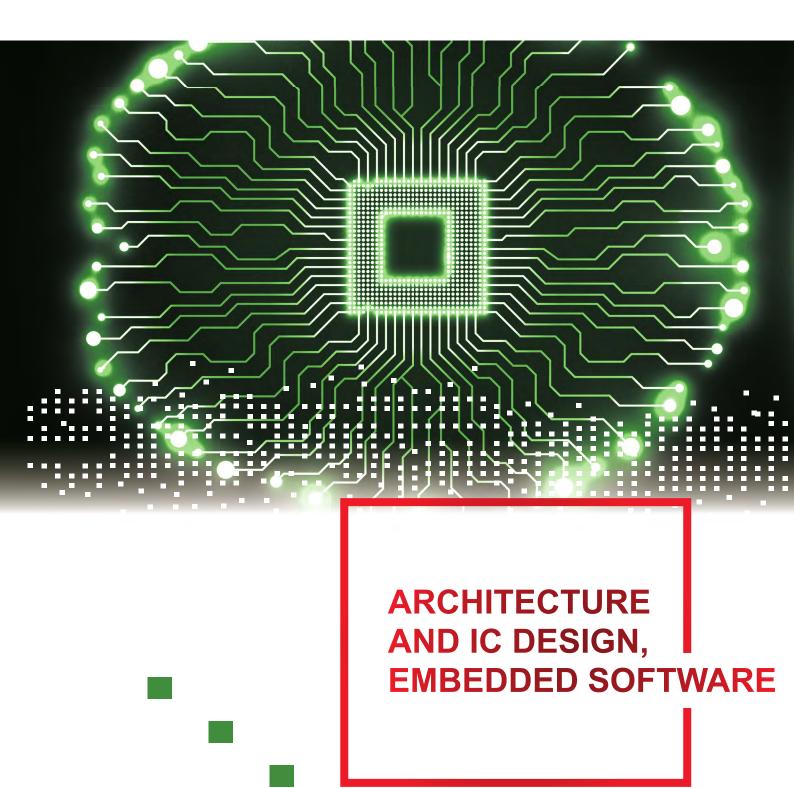


TECHNOLOGY RESEARCH INSTITUTE





TECHNOLOGY RESEARCH INSTITUTE

LETI AT A GLANCE

Founded in 1967

Based in **France** (Grenoble) with offices in **USA** (Silicon Valley) and **Japan** (Tokyo)

330

industrial partners

1,900 researchers

Committed to innovation, Leti's teams create differentiating solutions in miniaturization and energy-efficient technologies for its industrial partners.

Leti is a technology research institute at CEA, Tech and a recognized global leader focused on miniaturization technologies enabling energy-efficient and secure IoTj, Leti delivers solid expertise throughout the entire IoT, chain, from sensors to data processing and computing solutions. Leti pioneered FDSOI low power platform for IoTOM&NEMS technology for low cost multisensors solutions, CoolCube™ integration for highly connected and cost effective devices.

Leti's mission is to pioneer new technologies, enabling innovative solutions to ensure Leti's industrial partners competitiveness while creating a better future. It tackles most current global issues such as the future of industry0clean and safe energies, health and wellness, sustainable transport, information and communication technologies, space exploration and safety & securityj

For V2years, the institute has built long-term relationships with its partners: global industrial companies, SMEs and startups. It tailors innovative and differentiating solutions that strengthen their competitiveness and contribute to creating new jobs. Leti and its partners work together through bilateral projects, joint laboratories and collaborative research programs. Leti actively contributes to the creation of startups through its startup program.

Leti has signed partnerships with major research technology organizations and academic institutions. It is, a member of the Carnot Institutes network*.

*Carnot Institutes network: French network of 34 institutes serving innovation in industry.

2,760

patents in portfolio

60

startups created

€315

million budget

700

publications each year

ISO 9001

certified since 2000

CEA Tech institutes Leti and List share design, architecture & embedded software research activity in a dedicated division.

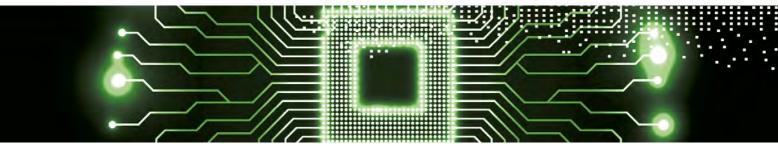
List is a key player in information and communication technologies. Its research activities are focused on digital systems that will have a major impact on society and the economy: embedded systems, ambient intelligence and information processing. List is based in CEA's Paris-Saclay campus.

In the dedicated division, more than 245 people focus on radio frequency, digital and SoC, imagers and sensors, integrated circuits, design environments and embedded software. Our research activities target the major challenges of tomorrow's systems. These include energy efficiency; complexity, especially in advanced technology nodes; reliability, including real-time constraints, security, and confidentiality; and the design of mixed-signal and heterogeneous systems (analog/digital, radio frequency, multi-physics, hardware and software).

We are preparing future systems in which computation, communication and real-world interactions will be tightly coupled. The Internet of Things and autonomous vehicles are primary examples of such applications.

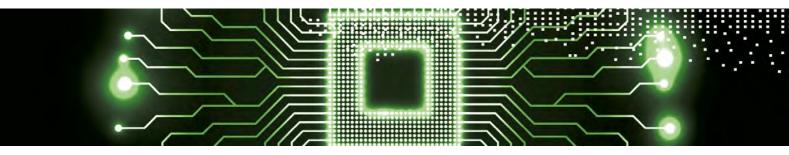
Leti and List researchers collaborate on projects for both CEA Tech's internal needs and outside customers, ranging from startups and SMEs to large international companies.

ARCHITECTURE AND IC DESIGN, EMBEDDED SOFTWARE



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EDITO

THIERRY COLLETTE

HEAD OF THE ARCHITECTURE & IC DESIGN, EMBEDDED SOFTWARE DIVISION

Information processing technologies and communications systems are everywhere, from mobile devices to household appliances, cars, portable medical devices and more. This drives the widespread development of emerging trends like the Internet of Things (IoT), Smart Cities, Autonomous Vehicles, and Smart Manufacturing—helping billions of objects around the world to connect securely and efficiently.

In peculiar, the rise of the IoT, cyber physical systems and artificial intelligence has brought the need to design novel smart devices capable of computing, sensing and communicating with extreme energy efficiency while also generating huge amounts of data in the cloud that require extensive storage and processing capacity. Real-time performance, fast data processing, low energy consumption, security and reliability are critical for IoT applications, from devices to infrastructures.

These technology challenges require a holistic approach to hardware and software. Hence, combining research between the two well-

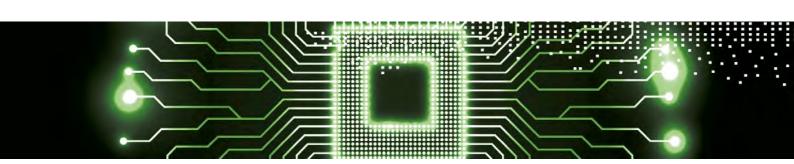


known institutes Leti and List becomes a necessity. Indeed, if Leti brings advanced know-how in integrated circuit design and testing, List has built-up renowned expertise in architecture and embedded software development.

Thus, from smart sensors and wireless connectivity to computing solutions, artificial intelligence and reliable systems, you will find in this report our latest innovations that address these upcoming challenges.

We hope you will enjoy reading this overview of our latest research,

Thierry Collette



KEY FIGURES



2 locations:
Minatec campus (Grenoble, France)
Nano-INNOV Paris-Saclay campus (Palaiseau, France)

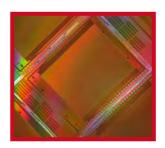
189 Permanent researchers61 PhDs and post-docs





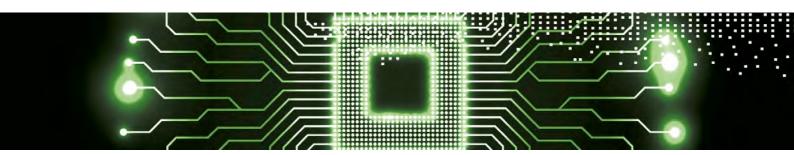
Full suite of IC CAD tools, hardware emulators, & industrial test equipment







50 granted patents49 papers, journals & books163 conferences & workshops



SCIENTIFIC ACTIVITY

Publications

208 publications in 2016, including journals and major conferences like ISSCC, RFIC/IMS, IEDM, ESSDERC, 3DIC, IEEE Sensors, DAC, DATE, SPIE, ITC, NIPS, HIPEAC, IEEE Cloud.

Prize and Awards

Best Paper Award, Izabachène et al. 'Faster Fully Homomorphic Encryption: Bootstrapping in less than 0.1 Seconds', Asiacrypt 2016. Etoiles de l'Europe 2016 Award, Levent Gürgen, ClouT FP7 Project

Experts

49 CEA experts: 5 research directors, 2 international experts. 14 researchers with habilitation qualification (to independently supervise doctoral candidates).

Scientific Committees

Editorial boards: IEEE Journal of Solid State Circuits, Journal of Low Power Electronics, ISTE-Editions.

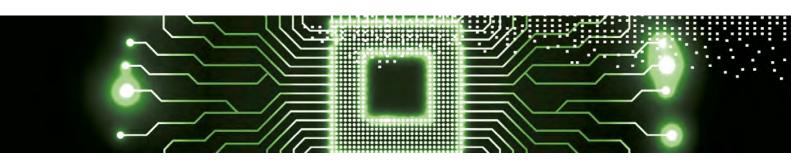
19 members of Technical Programs and Steering Committees in major conferences: ISSCC, VLSI-Circuits, ESSCIRC, DATE, ASP-DAC, ISPLED, HiPEAC, ICCAD, IJCNN, ESWeek, MPSoC.

Conferences and Workshops Organization

Real Time Networks 2016, Toulouse, France. FETCH 2016, Villard de Lans, France

International Collaborations

Collaborations with more than 20 universities and institutes worldwide, e.g. Stanford University (USA) University of California, Berkeley (USA), Columbia University (USA), Cornell University (USA), EPFL (Switzerland), ETHZ (Switzerland), CSEM (Switzerland), UCL (Belgium), UNIBO (Italy), Polito Torino (Italy), KIT (Germany), Chalmers University (Sweden), Tongji (China), Keio University (Japan), NII (Japan)...







METHODOLOGIES & HARDWARE -SOFTWARE INTEGRATION

- Performance prediction
- Code generation
- Cyber Physical Systems
- Power management
- 3D technologies

SCale: A NEW PARALLEL SYSTEMC KERNEL LEVERAGING MANYCORE ARCHITECTURES

RESEARCH TOPIC:

SystemC, parallel kernel, discrete event simulation, ESL design, acceleration, MPSoC, SCale, SESAM

AUTHORS:

N. Ventroux, T. Sassolas

ABSTRACT:

The complexity of system-level modeling is continuously increasing. Electronic System Level (ESL) design requires fast simulation techniques to control future SoC development cost and time-to-market. However, SystemC simulations are sequential and then limited by single-thread performance. This paper presents a new parallel SystemC kernel that efficiently leverages the multiple cores of a host machine, reaching high simulation performance without relaxing accuracy. This new kernel is fully compliant with existing standards and easy to integrate in any existing *SystemC* model. Evaluations show a maximum acceleration of 34x compared to *Accellera SystemC* on a 64-core AMD Opteron machine

Context and Challenges

SystemC is a hardware description language standard for system-level modeling established by major EDA vendors through the Accellera Systems Initiative and widely used in the IC industry. Together with TLM (Transaction Level Modeling), it provides an effective framework for HW/SW co-design, systemlevel modeling and performance evaluation, design space exploration (DSE), high-level verification, as well as early development of system software.

SystemC uses a cooperative multithreading technique to model concurrency, ensuring that all processes are sequentially evaluated without interruption between two wait statements. Even if the process evaluation order is unpredictable in SystemC, the sequentiality imposed by the kernel ensures deterministic and predictable simulations for early SW development and simulatorbased debugging. When the design is simulated multiple times using the same stimulus and the same version of the simulator, the process ordering between different runs will not vary.

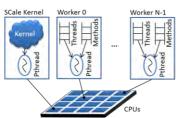


Fig. 1. SCale software architecture

On the contrary, parallel SystemC simulations can exhibit various types of dependent process behavior, such as race conditions. Apart from globally shared variables, which are often bad design practices, a typical example is the existence of shared variables between a module's processes. But TLM brings even more examples of process dependencies when, for instance, multiple TLM masters share a TLM slave and then its member variables. In this paper we propose a parallel SystemC kernel named SCale fully compliant with the standard i.e which ensures that a process evaluation behaves like an atomic section and provides a deterministic behavior along multiple executions.

Main Results

The SCale simulation kernel provides a simple set of annotation primitives that allow any SystemC model to be evaluated in parallel. Annotations allow to statically allocate SystemC threads to a given evaluation thread (aka worker). Every access to shared resources can be annotated with another primitive sc process conflict_check to ensure fully atomic evaluation of processes. All workers evaluate in parallel their allocated threads and all accesses to shared resources are monitored. At the end of each parallel evaluation phase, a dependency graph of all read/write accesses from all workers is built. If it is acyclic, it represents one equivalent sequential process evaluation that results in the same model state. Otherwise multiple workers' accesses were interleaved, breaking the atomicity rule, and information is issued to the end-user. This is likely to originate form bad modelling or bad hardware design that needs to be addressed.

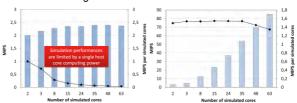


Fig. 2. Performance of SESAM [4] SystemC simulator on a 64-core using Accelera (left) and SCale (right) kernels

Consequently, while Accellera kernel's simulation speed decreases with the complexity of the model, SCale parallel evaluation provides the necessary speedup for large system validation such as MPSoC. Using a 64-core AMD Opteron host, SCale reaches acceleration of x34 compared with Accellera kernel without loss of accuracy. Compared with other parallel frameworks, SCale still provides significant acceleration of up to 44% for comparable hardware.

Perspectives

Future work will target the automatic insertion of SCale primitives to guarantee the atomic evaluation of SystemC processes of legacy models; as well as valorization through the integration in industrial ESL simulation solutions and large system simulation.

RELATED PUBLICATIONS:

- [1], N. Ventroux and T. Sassolas, "A new parallel SystemC kernel leveraging manycore architectures" in DATE'16, pp. 487-492.
- [2] J. Peeters, N. Ventroux, T. Sassolas, and L. Lacassagne, "A SystemC TLM Framework for Distributed Simulation of Complex Systems with Unpredictable Communication," DASIP'11.
 [3] N. Ventroux, J. Peeters, T. Sassolas, and J. Hoe, "Highly-Parallel Special-Purpose Multicore Architecture for SystemC/TLM Simulations," in SAMOS'2014.
- [4] N. Ventroux et al., "SESAM: an MPSoC Simulation Environment for Dynamic Application Processing," in ICESS 10.

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METHOD TO EVALUATE DATA COHERENCY PROTOCOLS WITHIN A COMPILATION TOOLCHAIN



RESEARCH TOPIC:

Many-core and MPSoCs, Parallel and distributed programming, Shared memory, Data coherency, Compilation, Simulation

AUTHORS:

L. Cudennec, S. Dahmani (UPMC/LIP6), G. Gogniat, C. Maignan (UBS/LabSTICC) and M.J. Sepulveda (TUM/ISIT)

ABSTRACT:

Shared memory is a critical issue for large distributed systems. Despite several data coherency protocols have been proposed, the selection of a protocol that best suits the application requirements remains a challenge. We focus on the analytical evaluation of the coherency configuration that stands within the optimization loop. We propose to use a TLM NoC simulator to get feedback on expected network contentions. We evaluate the approach using five workloads, three data coherency protocols and two NoC topologies. As a result, we are able to obtain a fast and accurate evaluation of the different coherency-protocol alternatives.

SCIENTIFIC COLLABORATIONS: Université Pierre et Marie Curie (Paris), Université de Bretagne Sud, Technical University of Munich

Context and Challenges

Today, many-core processors embed thousands of processing cores on a single chip with complex distributed memory systems. The shared memory paradigm is quite popular in parallel and distributed systems because the developer is not in charge of managing communications to localize and transfer data. Several data coherency models, from strong to weak have been defined and since then, there is no such protocol that fits to all applications, many-core architectures and running contexts. To transparently decide on the most relevant protocol, a regular compilation system may not afford to simulate with a high level of precision and to process all possible solutions. We propose the use of high-level cycle-accurate system model for evaluating the coherency protocols in MPSoCs.

Main Results

The coherency protocol decision process takes place within a full compilation toolchain. It attaches to each access a coherency protocol with optimized instantiating parameters. This is achieved using genetics based optimization algorithms. The evaluation can be performed by analytical or simulation models. The basic version of the simulator consists on a modular SystemC-TLM cycle accurate simulation environment composed by a set of libraries that allow the description and configuration of NoCbased MPSoCs

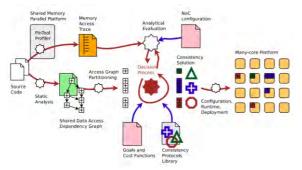


Fig. 1. Compilation toolchain for decision on data coherency

First, an input memory access trace is obtained using a dynamic binary instrumentation tool from a previous execution. The obtained traffic includes all exchanged messages involved in a memory access request. However these messages are not timestamped: there only exists a causal dependency relation. We therefore partition the set of messages (in a contiguous way), each subset being sequentially fired in the simulator, and all messages within a subset being fired in parallel. Partitioning describes different injection rates: from a full sequential trace (one message in each subset - 0%) to a full parallel trace (all messages in a single subset - 100%).

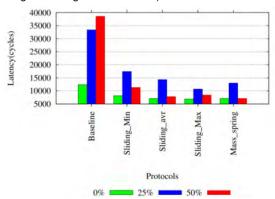


Fig. 2. Cumulative access latencies using different coherence protocols and parallel access injection rates (0% - 50%)

Using the simulator with different injection rates can reveal that a protocol may perform badly under massive parallel load. This behavior is not highlighted by a pure analytical evaluation. Processing times are also kept within reasonable bounds in order to be integrated within the multi-protocol compilation platform.

Perspectives

New evaluations metrics (e.g. Throughput, Energy) can be proposed in order to enhance the model precision. Moreover, a reverse analysis using the proposed model would allow to design a NoC configuration well adapted to a set of applications and

RELATED PUBLICATIONS:

[1] L. Cudennec, S. Dahmani, G. Gogniat, C. Maignan and M.J. Sepulveda, "Network Contention-aware Method to Evaluate Data Coherency Protocols within a

Compilation Toolchain", 10th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-16), Lyon, France, September 2016.
[2] L. Cudennec, S. Dahmani, G. Gogniat, C. Maignan and M.J. Sepulveda, "A Fast Evaluation Approach of Data Consistency Protocols within a Compilation Toolchain", Proceedings of the Fourth International Workshop on Architecture, Languages, Compilation and Hardware support for Emerging ManYcore systems (ALCHEMY 2016), San Diego, CA, USA, June 2016.

[3] J. Marandola, S. Louise and L. Cudennec, "Pattern Based Cache Coherency Architecture for Embedded Manycores", ALCHEMY, San Diego, CA, USA, June 2016

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ENSURING DEPENDABILITY AND PERFOMANCE FOR CPS: APPLICATION TO A SIGNALING SYSTEM

RESEARCH TOPIC:

Cyber-Physical Systems, System Design, Safety, Transport

AUTHORS:

Elie Soubiran (Alstom), Fateh Guenaba (Alstom), Daniela Cancilab, Ali Koudric (SystemX), Laurent Wouters (SystemX)

ABSTRACT:

This works goes through the development process of a Cyber-Physical System in the railway industry. It starts from the scenario of passengers going on and off an autonomous train and explores the engineering steps from the identification of the user needs down to the system design and implementation. The work emphasizes the iterative and collaborative nature of the engineering process with a special care for the continuous verification of engineering choices. Moreover, it studies how engineering data is shared across disciplines, as this is a key element supporting continuous verification.

SCIENTIFIC COLLABORATIONS: Alstom, IRT-SystemX

Context and Challenges

The railway urban sector currently undergoes a great transformation. The Observatory of Automated Metros (UITP) states that in 2013 there are 674 km of automated metro in operation". This number is expected to triple 5 in the next 10 years to reach 1.800km in 2025.

From a **business perspective**, we are witnessing a heavier pressure from the market for a leap forward in terms of performance, infrastructure and of course, safety. To this end, the railway industry invests almost 1000 Million e each year in research and development and there are then strong expectations for the stakeholders to deliver cost-effective services for intermediate and final 15 users: more intelligent, integrated and autonomous systems, safe access to vehicles, reduction of the CO2 footprint, etc

From an **engineering perspective**, the new generation of CBTC (Communication Based Train Control) urban transportation systems lessens this role by integrating more functions within trains themselves and by promoting Train-To-Train communications. This direction leads to more complex train systems with the development of a distributed and autonomous intelligence for their control. From a **technical perspective**, the signaling system has to guarantee the safety of trains' movements, included operational and supervision functionality.

Main Results

We introduce a design methodology tailored to railway application domain and we test it along the whole design and development chain including early verification and validation of deign choices.

The proposed methodology is compliant with the safety standards and procedures of our partner Alstom. It takes into account the iterative process and the collaborative nature of the process across engineering and safety activities.

Figure 1 shows the 6 phases required by the CENELEC safety standard. We divided them in three major stages:

 System definition, which addresses the capture and the structure of user needs into services that the system must meet

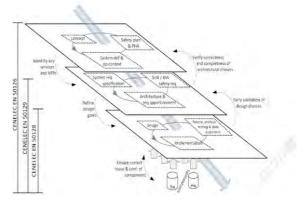


Figure 1: Combing collaborative engineering and the CENELEC process

- System Requirement and Architecture, which defines the functional and system architecture
- System Design and Implementation, which embraces the physical architecture with a breakdown into hardware and software components.

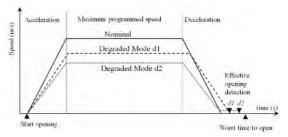


Figure 2: Study of the velocity in the opening/closing doors procedures

Perspectives

The guarantee of safety-related properties in the CPS-IoT.

RELATED PUBLICATIONS:

- [1] E. Soubiran, F. Guenab, D. Cancila, A. Koudri, L. Wouters, Ensuring Dependability and Performance for CPS Design: Application to a Signaling System, Chapter 23
- In Cyber-Physical Systems Foundations, Principle and Applications, Elsevier, 2016
 [2] D. Cancila, R. Passerone, T. Vardanega, M. Panunzio, Toward Correctness in the Specification and Handling of Non-Functional Attributes of High-Integrity Real-Time Embedded Systems, IEEE Transactions on Industrial Informatics, 2010
- [3] Daniela Cancila, Elie Soubiran, Roberto Passerone Feasibility Study in the use of contract-based approaches to deal with safety-related properties. Ada User Journal, December 2014.

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DVFS MANAGEMENT OF A SYSTEM-ON-CHIP: A Q-LEARNING BASED METHOD FOR THROUGHPUT CONSTRAINT APPLICATIONS



RESEARCH TOPIC:

Dynamic Voltage-Frequency Scaling, Reinforcement learning, Q-learning, SoC,

AUTHORS:

Anca Molnos, Suzanne Lesecq, Julien Mottin, Diego Puschini

ABSTRACT:

We investigate a new Q-learning based strategy to manage Dynamic Voltage Frequency Scaling (DVFS) on a system on chip (SoC) such that the energy consumption is reduced. We address software applications with throughput constraints. The proposed Q-learning formulation has two main advantages: it has a reduced state space to limit the overhead and it embeds a new reward function tailored for throughput-constrained applications. The DVFS manager is evaluated on a test chip executing an object recognition application. The results suggest that the proposed method reduces the energy consumed with up to 44% at the cost of occasionally increasing the number of throughput violations, when compared to state-of-the-art methods addressing the same application domain.

Context and Challenges

The success of a DVFS management policy, and hence the energy efficiency of a SoC, severely depends on the ability to react to changing application workload. Several approaches attempt to model the dynamics of applications as linear or nonlinear (e.g., fractal threshold-based). In general, building an accurate model of the dynamics of applications is a very challenging job. Today online learning methods are employed because they promise to solve the DVFS problem without needing a model of the dynamics of applications. Furthermore, to avoid the training step, recently, indirect adaptive control, referred to also as Reinforcement Learning (RL), gains in popularity.

Q-learning is a low cost, reinforcement learning approach that associates a quality and a reward to each system state, to steer management decisions. The challenge in this case is to choose the system states and the reward function such that the cost of the manager, in terms of time, energy and memory overhead, does not surpasses its benefits.

Main Results

We propose a Q-learning manager that gradually learns how the application workload varies in time, by monitoring the buffers filling evolutions over time. Furthermore, the manager reacts to these variations by setting the DVFS operating points of the platform such that the long-run SoC energy consumption is minimized and the application throughput constraint is respected.

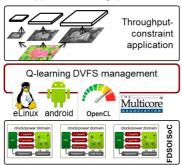


Fig. 1. The system stack

The targeted platform template consists of a host processor that controls the heavy application computation, which executes on a system-on-chip (SoC). The SoC may include several processor elements (PEs), and the DVFS may be applied to one or several processors, similar to the techniques envisioned by the FDSOI technology [1, 2]. The SoC is administrated by a Linux-based operating system which we augment with a Q-learning manager, as described Fig. 1.

We experiment with the DVFS manager on a test-board comprising an ARM host processor and a SoC with 16 processors elements, executing several applications from the domain of object recognition and data fusion. The parameters of the Q-learning methods are investigated, leading to a configuration that reduces the energy consumed with up to 44% when compared to state-of-the-art methods, i.e. non-linear and proportional-integral (PI) controller [3]. A trade-off between the application throughput and the energy consumption is enabled. In addition, these ideas are demonstrated on a commercial board as well, i.e., IMX6 from NXP Semiconductors (Fig.2).

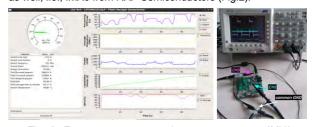


Fig. 2. Energy management demonstrator on an IMX6 board running an embedded Linux operating system.

Perspectives

The high variability exhibited by software applications and hardware platforms today demands for more investigations on methods for quicker convergence of the learning process and for dealing with non-stationary variations. Furthermore, DVFS technologies allow many voltage-frequency values, and several sleep modes. Hence future solutions should cover a large, potentially continuous decision space and complex energy models, e.g., temperature- and/or reliability-dependent.

RELATED PUBLICATIONS:

[1] D. Puschini, J. Rodas, E. Beigne, M. Altieri, S. Lesecq, "Body Bias usage in UTBB FDSOI designs: A parametric exploration approach". in special Issue: Planar Fully-Depleted SOI technology, Solid-State Electronics Elsevier Journal, Volume 117, March 2016, pages 138-145, [2] I. M. Panades et al., "A fine-grain variation-aware dynamic Vdd-hopping AVFS architecture on a 32 nm GALS MPSoC," J. Solid-State Circuits, vol. 49, no. 7, pages.

[2] I. M. Panades et al., "A fine-grain variation-aware dynamic Vdd-hopping AVFS architecture on a 32 nm GALS MPSoC," J. Solid-State Circuits, vol. 49, no. 7, pages 1475–1486, 2014.

[3] A. Molnos et al. "Energy management via PI control for data parallel applications with throughput constraints". In Proc. of International Workshop on Power And Timing Modeling Optimization and Simulation, pages 63-70, 2015.

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BODY BIAS USAGE IN UTBB FDSOI DESIGNS: A PARAMETRIC EXPLORATION APPROACH



FDSOI, Body Bias, Power Consumption

AUTHORS:

Diego Puschini, Jorge Rodas, Edith Beigne, Mauricio Altieri, Suzanne Lesecq

ABSTRACT:

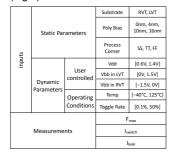
UTBB FDSOI offers an extended Body Bias operation range. This new opportunity is considered as a new degree of freedom in addition to the classic Dynamic Voltage Scaling (DVS) techniques. However, no formal or empiric tool allows to early evaluate the need for a Dynamic Body Bias (DBB) mechanism on future designs. In this work, a parametric exploration has been conducted to analyze the benefits of using Body Bias in 28 nm UTBB FDSOI circuits. This exploration contributes to the identification of conditions that make DBB more efficient than DVS, and vice versa, and when both methods are mandatory to optimize power consumption.

Context and Challenges

One of the most interesting advantages offered by UTBB FDSOI is the extended Body Bias range compared to Bulk technology. By back biasing the circuit the effective threshold voltage Vth is changed, strongly impacting the propagation delay and leakage current of the controlled gates. Body Bias has been traditionally used in Bulk technology as a passive way to compensate process variations and to dynamically reduce the leakage current of non-active parts of the circuit. In UTBB FDSOI, the range can reach 3V, increasing the effect of Body Bias, enabling more power reduction. Understanding the technology behavior on a sample digital circuit helps on the choice of the best power management strategy.

Main Results

The total power consumption of a representative digital sample circuit has been estimated thought electric simulations for a wide range of supply voltage (Vdd) and Body Bias (Vbb). This experience has been repeated in order to explore the power consumption and circuit speed (maximal applicable clock frequency, F_{max}) under different static and dynamic parameters (Fig 1).



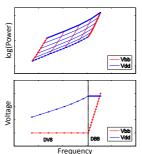


Figure 1 - Parametric exploration for power analysis

A deep analysis of results on power consumption shows that depending on the balance between static and dynamic power consumption of the circuit and the target range frequency, the circuit will be optimized through DVS, DBB or both techniques.

Based on this experiences, a methodology has been proposed to help the circuit designers to choose the best power management strategy for future designs in UTBB FDSOI. Fig 2 summarizes an example of a circuit in UTBB FDSOI using LVT gates in typical (TT) corners. Depending on the temperature and gate switching rate (circuit activity), three conditions are possible: Body Bias is only required for extreme speed-up; it is mandatory for a wide range of frequencies; or it only helps to optimize power consumption under specific conditions in low clock frequencies.

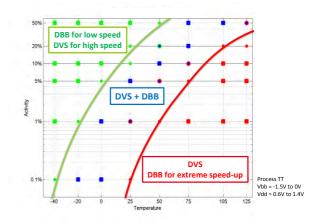


Figure 2 - Power domination for different activity and temperature configurations

Perspectives

The results of this exploration can be integrated into a circuit design methodology, optimizing power management techniques embedded in future circuits and taking advantage of Body Bias opportunities of UTBB FDSOI.

RELATED PUBLICATIONS:

[1] Diego Puschini, Jorge Rodas, Edith Beigne, Mauricio Altieri, Suzanne Lesecq, "Body Bias usage in UTBB FDSOI designs: A parametric exploration approach", Solid-State Electronics, Volume 117, March 2016, Pages 138-145, ISSN 0038-1101, https://doi.org/10.1016/j.sse.2015.11.019.

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3DIP: AN ITERATIVE PARTITIONING TOOL FOR MONOLITHIC 3D IC

RESEARCH TOPIC:

Monolithic 3D; High Density IC; 3D partitioning; CoolCube™

AUTHORS:

G. Berhault, S. Thuries, F. Galea, L. Zaourar

ABSTRACT:

We propose a new partitioning tool for 2-tier Cell-on-Cell Monolithic 3D (M3D) ICs before placement. It is based on a fast and iterative algorithm that explores the space of solutions and minimizes the estimated cost of wires with balanced area between tiers without limiting the number of Monolithic Intertier Vias (MIV). A mathematical formulation of the 3D partitioning problem and a comprehensive framework, based on simulated annealing (SA) algorithm coupled with a dedicated cost function, are detailed and compared with Min-Cut (MC) partitions commonly used. It appears that our solution can decrease the estimated total cost of wires by 41% and 45% for an LDPC and FFT/AES units. It also reduces the total cost of wires by 30% to 44% compared to the MC algorithm for the same units and with no significant increase in runtime.

Context and Challenges

Previous works proposed straightforward partitions [1] [2], or Min-Cut based partitions [3]. These methods tend to limit the number of MIVs, that is no more relevant for M3D, and do not explore all the possibilities.

Main Results

In this study, we propose a new partitioning tool before placement step based on an exhaustive and iterative algorithm to minimize the estimated wire cost with balanced area between both tiers within two main contributions: a mathematical formulation of the M3D partitioning problem, and a full partitioning framework based on simulated annealing algorithm with performance comparison to a commonly used MC algorithm implemented in hMetis tool.

A framework has been established to generate 3D netlists from a netlist obtained through a commercial 2D synthesis tool as illustrated below. It is composed of three main parts: a tool which converts the netlist into a hypergraph suited for the partitioning tool; a partitioning tool implementing either a min-cut algorithm or the proposed solution of an SA algorithm with a cost function aiming at decreasing the estimated hyperedge weight (HW) while preserving the area balance; and a tool which converts original netlist into 3 netlists

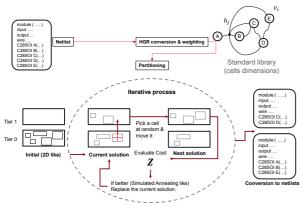
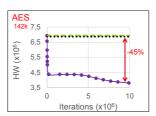


Fig. 1. 3DIP Framework and Cost Function (below)

$$HW_{h_j} = \left(\sum_{i=0}^{N-1} \left[(W_{v_i} + H_{v_i}) M_{ij} X_{i0} \right] \right)^2 + \left(\sum_{i=0}^{N-1} \left[(W_{v_i} + H_{v_i}) M_{ij} X_{i1} \right] \right)^2$$

The wire length is correlated to the wire cost HW that is estimated based on the Half-Perimeter Wire Length (HPWL) model. The algorithm starts with all the cells on the same level. That is why the hyperedge weight starts from the 2D hyperedge weight and also why the cut number starts from 0.



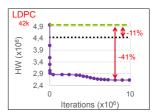


Fig. 2. 3DIP wire cost reduction compared to 3D and MinCut

The number of cuts (MIVs) is closely linked to the hyperedge weight reduction (compared to the 2D hyperedge weight taken as a reference). Indeed, the MC algorithm has a small number of cuts and it almost does not reduce the hyperedge weight, around 1% or even 11% in reduction, while SA algorithm can reduce the hyperedge weight up to 45%. The MC partitionings have a total hyperedge weight close to the 2D design hyperedge weight because, as its name implies, it minimizes the number of cuts. Therefore, the MC partitioning returns 2 graphs that are almost independent, thus having two 2D circuits. Since the sum of the hyperedge weight of two 2D circuits is the same as the 2D original design, the MC Hyperedge weight is close to the 2D hyperedge weight. As expected, the MC algorithm minimizes the number of cuts while our SA algorithm tends to maximize them in order to reduce the total hyperedge weight.

Perspectives

It appears that best gains are reached by increasing the MIV number contrary to min-cut algorithm commonly used for 3D IC design. The presented work constitutes a first step towards a full Monolithic 3D placer.

RELATED PUBLICATIONS:

- [1] Berhault, G., et al., "3DIP: An Iterative Partitioning Tool For Monolithic 3D IC", IEEE International Conference on 3D System Integration (3DIC) 2016
- [2] Billoint, O. et al., "A comprehensive study of Monolithic 3D cell on cell design using commercial 2D tool", DATE 2015
 [3] Sarhan, H., et al., "An Unbalanced Area Ratio Study for High Performance Monolithic 3D Integrated Circuits", ISVLSI 2015.
 [4] Panth, S. et al., "Placement-driven partitioning for congestion mitigation in monolithic 3D IC designs", TCAD 2015

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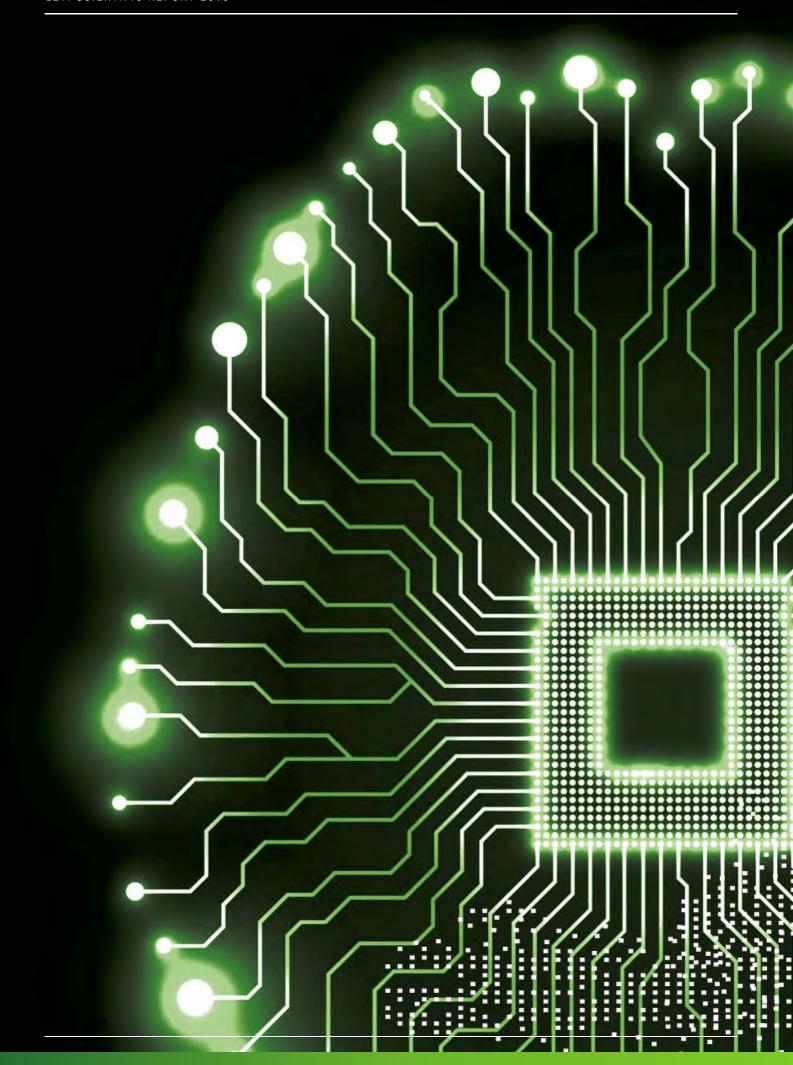
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2.

COMPUTING SOLUTIONS: MULTI/MANY CORES, ARCHITECTURES & SOFTWARE

- Performance prediction
- Code generation
- Cyber Physical Systems
- Power management
- 3D technologies



HIGH PERFORMANCE COMPUTING, COMPILATION, CODE SPÉCIALISATION AND COMPUTER **ARCHITECTURE: CROSS DOMAIN APPROACHES**

RESEARCH TOPIC:

Compiler, Just in time compilation, High performance Architecture, Cache, Prefetching, In Memory Computing

AUTHORS:

H.P. Charles, S. Lesecq, S. Mancini (UGA), L. Vincent (TIMA, Persyval), J.F. Méhaut (Inria)

ABSTRACT:

High performance computing is a very hard research task and results are no more to be search in one domain. Effort should be spread across multiple research domains: computer architecture and memory hierarchy are a central point but compilers and applications are closely coupled and have huge impact on performance. This synthesis shows results spreading from hardware architecture up to applications for High performance computing. It is amazing to see that those results come from collaborations between scientists from different domains: computer architecture, control command theory, compilers and code optimization.

SCIENTIFIC COLLABORATIONS: INRIA (Grenoble), TIMA (Grenoble)

Context and Challenges

This work deals with High performance Computing. Using efficiently the huge computing power of modern computer becomes more and more complex. However, interesting results can be achieved at the frontier of different scientific domains: Hardware-Software interactions. , Compilers, Cross domains Researches.

Main Results

This page will illustrate some of our results in this field.

In the PhD thesis [1], the author has shown that developing a powerful parallel application using floating point arithmetic on a Java virtual machine is possible but many options can be used: code polymorphism, native code or Java Virtual Machine tuning, but unfortunately there is no universal efficient method. This results was a collaboration between an industrial and academic

Similarly in [2] we showed that the polymorphism used at high level in Java can be useful in the IoT domain, on embedded platform by specializing the OS network stack. In this case the collaboration lies between the OS level and the dynamic

A more complex approach as shown interesting results in [3] where a dynamic on-line auto tuning is able to adapt a running binary code at run-time by regenerating binary code at run-time for a vectorized benchmark (PARVEC). The global view of the framework is shown in Fig 1. In this case the collaboration is between a dynamic application and the code generator.

5G telecommunication algorithms are very compute intensive and run it on complex MPSoC is challenging because of the complex partition to do between hardware blocks and classical CPU parts. The article [4] and the corresponding PhD thesis has shown that an approach using actor model and a dynamic compilation scheme based on LLVM can be used to take care of the dynamic reconfigurations needed by the 5G algorithms.

At an even lower level, the memory hierarchy become complex and dynamic applications, such as image transformations algorithms, does not take fully advantage of the data caches. Designing a new data prefetcher, using control command theory,

was a successful approach [5].

Surprisingly, the results on auto-tuning framework and the data prefetcher use a similar feedback scheme similar to the figure 1.

At an even lower level, the publication [6], which is a collaboration between memory architects and compilers specialists showed that special memory blocks can be designed to speed-up memory intensive applications. DRC2 is a new "In memory computing" architecture that implements very efficiently basic operations directly in memory.

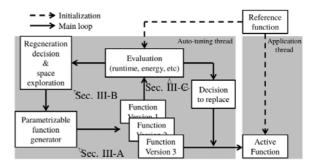


Fig 1: Architecture of the run-time auto-tuning framework

Perspectives

Because High Performance Computing has no definitive solution for performance portability across time, many cross domains collaboration should continue to investigate opportunities offered by new architectures.

RELATED PUBLICATIONS:

- [1] Halli, N., "Code optimization for high-performance Java application", PhD Thesis, 2016, University Grenoble Alpes
- [2] Courousse, D.; et al., "Approximate Computing on Resource-Constrained Embedded Devices with Runtime Code Generation", WAPCO 2016.
 [3] Endo, F., et al., "Pushing the Limits of Online Auto-tuning: Machine Code Optimization in Short-Running Kernels" IEEE 10th MCSoC, 2016, France.
 [4] Dardaillon, et al. "A New Technique for Compilation of Software Defined Radio Applications on Heterogeneous MPSoC", ACM TACO 13(2), 2016.
 [5] Vincent, L; et al., "Model Free Adaptive Data Prefetching using Hypothesis Tests" 53rd DAC, 2016, USA.
- [6] Akyel, K.; et al., "DRC 2: Dynamically Reconfigurable Computing Circuit based on Memory Architecture", IEEE ICRC, 2016, USA.

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LEVERAGING DISTRIBUTED GRAPHLAB FOR PROGRAM TRACE ANALYSIS



RESEARCH TOPIC:

Graph-processing, Parallel processing, GraphLab, Programming Environments, Software Monitoring and measurements, Big Data

AUTHORS:

J.Collet, T.Sassolas, Y.Lhuillier, R.Sirdey J.Carlier (Heudiasyc Lab, UTC)

ABSTRACT:

Graph-mining is a class of data-mining problems where programs involve the processing of data modeled as graphs. These applications often exhibit irregular and data- dependent communication patterns, hampering parallelization opportunities on distributed architectures. Considering an in-house use-case, program trace analysis for parallelization optimizations, we study the benefits and limits of GraphLab, a graph-processing framework, for a tangible application with input instances up to 40 million vertices and 50 million edges. An in-depth analysis of the GraphLab system was conducted to evaluate its performance and scalability in the context of program trace analysis.

SCIENTIFIC COLLABORATIONS: Heudiasyc (Compiegne)

Context and Challenges

The graph-mining area is a data-mining domain of interest in which large graphs are processed to extract higher-level information. Graph processing is key in different domains such as biology, web analysis, security or social networks. With the advent of big data, processing power and memory are more and more needed. To address these needs, parallel programming tools leveraging large scale distributed architectures appeared. Unfortunately, none of the traditional parallelization approaches (e.g. OpenMP or MPI) are suitable for such irregular applications. As a matter of fact, historical High-Performance Computing applications included regular algorithms (e.g. physics simulations) for which pure-MPI programs are suitable. In opposition, recent irregular graph-processing applications (e.g. graph-traversal) would be costly to implement using explicit MPI communication

To tackle the challenge of deploying scalable processing graphrelated programs, many dedicated frameworks appeared. Such tools come in many different flavors, with specific programming models, memory views, languages or associated toolsets. In this context and considering a novel application, it is then a real challenge to choose the most appropriate graph processing infrastructure as literature exhibits global trends, but no clear winner. Indeed, part of the difficulty to design a system for graphrelated applications lies in the lack of objective benchmarks. Moreover, as input data greatly influences the execution behavior of an algorithm it is then difficult to predict its performances.

In this work, we study processing performance behaviors in the context of a novel application leveraging GraphLab, a graphprocessing framework for distributed architectures. To this extent, a 7-node distributed cluster and varying Input data sizes were used to assess the scalability of the system. In particular, several metrics were used to analyze GraphLab's performance, including throughput measurements (Fig. 1) or scalability (Fig. 2).

Main Results

We conducted experiments to measure the performance of GraphLab on an in-house program trace analysis algorithm [2]. This investigation led us to highlight different operating ranges, leveraging better understanding of our testbed's behavior for further performance predictions or platform tuning.

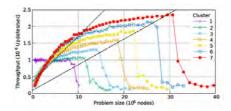


Fig. 1: GraphLab implementation performances in terms of macro-operations per seconds with varying cluster and problem sizes

The study shows that, with respect to scale, three operating ranges can be observed (Fig. 1). On the left part, the cluster is underloaded and nodes are inefficiently used. On the center part, machines are sufficiently loaded and performances are improved when adding machines. On the right part, the problem becomes too large and the cluster runs out of memory.

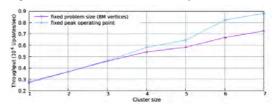


Fig. 2: Performance scalability for a fixed problem size (in purple) and for a fixed operating point (in blue) with varying machine scale. This figure illustrates that scalability may be achieved with growing problem and cluster sizes

Moreover, we observed that operating scalability is achievable with the considered system, as soon as problem size grows, advocating for GraphLab's relevance in such context.

Perspectives

We aim at generalizing the outcomes of such experiments by studying operating performance behaviors of different algorithmic use-cases [3] and hardware architectures. In particular, the relevance of micro-server architectures shall be explored in future works.

RELATED PUBLICATIONS:

- [1] J. Collet, T. Sassolas, Y. Lhuillier, R. Sirdey, J. Carlier, "Leveraging Distributed GraphLab for Program Trace Analysis", in proc. IEEE HPCS, July, 2016
- [2] A. Guerre, J.-T. Acquaviva, and Y. Lhuillier, "A unified methodology for a fast benchmarking of parallel architecture," in Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014, March 2014, pp. 1–4.
 [3] J. Collet, T. Sassolas, Y. Lhuillier, R. Sirdey, J. Carlier, "Exploration of de Bruijn Graph filtering for *de novo* assembly using GraphLab", 2017 (under publication)



TRANSACTION PARAMETERIZED DATAFLOW: A MODEL FOR CONTEXT-DEPENDENT STREAMING APPLICATIONS



Dataflow, Programming models, Real-time applications

AUTHORS:

XK. Do, S. Louise, A. Cohen (INRIA)

ABSTRACT:

Static dataflow programming models are well suited to the development of embedded many-core systems. However, complex signal and media processing applications often display dynamic behavior that do not fit the classical static restrictions. We propose Transaction Parameterized Dataflow (TPDF), a new model of computation combining integer parameters and a new type of control actor to allow topology changes and time constraints enforcement. We present static analyses and introduce also a static scheduling heuristic to map TPDF to massively parallel embedded platforms.

SCIENTIFIC COLLABORATIONS: ENS Ulm, INRIA

Context and Challenges

The broader availability of low-power many-core platforms - such as the MPPA-256 chip from Kalray (256 cores) or Epiphany from Adapteva (64 cores) - opens new opportunities for system designers. The complexity of these platforms also pushes for practical solutions accessible to domain experts, facilitating efficient mapping, performance tuning and analysis of applications.

Programming languages based on dataflow models of computation have emerged as a comprehensive solution towards the automation of embedded system design. Dataflow application are modeled as a directed graph where nodes represents actors (iterated execution of tasks) and edges represent communication channels. Among these, decidable dataflow models in the SDF or CSDF [2, 3] family are useful for their predictability, formal abstraction, and amenability to powerful optimization techniques. However, for signal processing applications, it is not always possible to represent all of the functionality in terms of purely decidable dataflow representations; typical challenges include variable data rate processing, multi-standard or multi-mode signal processing operation, and data-dependent forms of adaptive signal processing behavior.

Main Results

We introduce a new dynamic Model of Computation (MoC), called Transaction Parameterized Dataflow (TPDF), allowing variable production and consumption rates and dynamic changes of the graph topology. TPDF is designed to be statically analyzable regarding the essential deadlock and boundedness properties, while avoiding the aforementioned restrictions of decidable dataflow models.

Figure 1 shows a simple TPDF graph where actors have constant or parametric rates (e.g., p for the output rate of A). The repetition vector is [2; 2p; p; p; 2p; 2p]. C is a control actor and e_5 is a control channel. A sample execution of the graph is the following: A fires and produces p tokens on e_1 . Then B fires and produces one token on edge e_2 , e_3 , e_4 . Only E can fire because there are enough tokens on its input edge and produce one token on edge e_7 . E (and E if necessary) will fire a second time and produce another token on edge e_2 , e_3 , e_4 . Then E, E and E will fire and produce E, E and E token on edge E. Finally,

 ${\it F}$ fires two times, each time it consumes one token from its control port. This token determines in which mode ${\it F}$ will be fired. In this case, ${\it F}$ can choose two tokens from e6 or one from e7 and remove remaining tokens. This continues until each actor has fired a number of times equal to its repetition count.

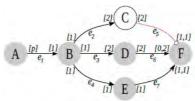


Fig. 1. A simple TPDF graph with integer parameter p and control actor ${\it C}$

We have applied the TPDF approach to an OFDM demodulator from the domain of cognitive radio, which is one of the fundamental subsystems of LTE and WiMAX wireless communication systems.

Figure 2 presents the minimum buffer size required by the application, depending on the vectorization degree and the symbol length. We find out that the buffer size increases proportionally to the vectorization degree and we have an improvement of 29% in comparison with the implementation by using CSDF.

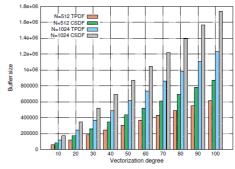


Fig. 2. Minimum buffer size increased proportionally to the vectorization degree

RELATED PUBLICATIONS:

[1] XK. Do, S. Louise and A. Cohen, "Transaction Parameterized Dataflow: A model for context-dependent streaming applications", in Design, Automation Test in Europe (DATE) 2016

[2] XK. Do, S. Louise, and A. Cohen. Comparing the Streamlt and Σ C Languages for Manycore Processors. Fourth International workshop on Data-Flow Models for extreme scale computing (DFM-14), Canada 2014
[3] XK. Do, S. Louise and A. Cohen "Managing the Latency of Data-Dependent Tasks in Embedded Streaming Applications" in International Symposium on Embedded

[3] XK. Do, S. Louise and A. Cohen "Managing the Latency of Data-Dependent Tasks in Embedded Streaming Applications" in International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC), 2015

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AN INTERMEDIATE REPRESENTATION TO MAP WORKLOADS ON HETEROGENEOUS PARALLEL SYSTEMS



RESEARCH TOPIC:

Intermediate Representation, Heterogeneous systems, parallel compilers

AUTHORS:

N. Benoit (ATOS Serviware), S. Louise

ABSTRACT:

Current trends in computer architecture show that we aim towards more cores and more heterogeneity. As an extensive knowledge of processor's internals cannot be a prerequisite to their programming these systems require the compilation flow to evolve and cope with parallel and heterogeneity issues. In this work, we start from a specific Intermediate Representation (IR) to explore the configuration space of Single Program Multiple Data (SPMD) program mapping on heterogeneous targets. Our experimental results show a very good accuracy of our tools to predict real world performance on several case study for classic heterogeneous systems.

SCIENTIFIC COLLABORATIONS: UVSQ)

Context and Challenges

Parallel programming is challenging in many aspects, and the performance of parallel programs relies on multiple factors. Furthermore, two architectures may not expose the same levels of parallelism and overheads for its exploitation. As the number of core rises in the future, and heterogeneity is thought to increase also, adapting old programs to new architectures is mandatory. But doing so for every release of new models of processors would be costly and time consuming. This is something that should be better handled by specialized compilation tools.

We provide an overview of our work on Intermediate Representation (IR) to find the degree of affinity between cores and portions of code. After that we show how we designed an oracle of performance so that to distribute workloads efficiently between cores. We validated this approach on benchmarks.

Main Results

In this work, we defined an IR, that is to say a mathematical model of the output of a parallelizing compiler. In our case, we use a hierarchical graph that can account for dependencies, as shown in Fig. 1.

Dependency accounting allows for a natural parallelization of code. The hierarchical aspect allows for choosing the correct coarsening of parallel code.

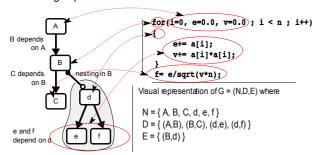


Fig. 1. IR graph model of a snippet of code; d is hierarchically included in B, e and f can be in parallel

In order to match any core in a heterogeneous system with any independent partition we use a very simple performance oracle

that attributes processing intensity to any type of low-level instruction. The oracle is coupled with a simple execution model that models how parallel processing kernels can be executed in the targeted heterogeneous architecture [1,2].

We evaluated our results on several systems including homogeneous architectures with heterogeneous task sets, and also a simple heterogeneous architecture consisting in a GPGPU targeted with automatically generated CUDA kernels and generals tasks executing on a 4 core Intel processor, as seen in Fig. 2.

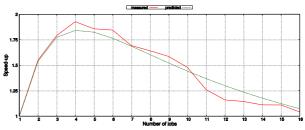


Fig. 2. Comparison between predicted performance and actual performance on GPGPU (Nvidia) and the number of threads on the main 4-core Intel CPU performing DCT on 9.10⁴ macroblocks

The predicted performance matches tightly the actual observed performance of the system, even with the simplified hypotheses we made (within 5%).

It validates our approach to partition and match automatically the parallel jobs on heterogeneous systems. While automatic partitioning is still a difficult task, this work lays the road to a heterogeneous parallel future.

Perspectives

To finalize the work toward achieving a fully parallelizing framework that allows for automatic placement of jobs on heterogeneous architectures, we will require probably a combination of hints in the source code (a la OpenMP, e.g. to easily identify massively parallel parts) and an efficient heuristic to place the partitioned jobs on the most efficient core for the job on heterogeneous systems. This is something we can expect to implement in our GCC plugin [3]

RELATED PUBLICATIONS:

- [1] N Benoit and S Louise, "A performance prediction for automatic placement of heterogeneous workloads on many-cores", Embedded Multicore/Many-core Systems-on-Chip (MCSoC), 2015 IEEE 9th International Symposium on, pp 159-166.
 [2] N Benoit and S Louise, "Kimble: a hierarchical intermediate representation for multi-grain parallelism", Proceedings of the Workshop on Intermediate
- [2] N Benoit and S Louise, "Kimble: a hierarchical intermediate representation for multi-grain parallelism", Proceedings of the Workshop on Intermediat Representations, 2011, pp 21-28
- [3] N. Benoit and S. Louise, «Extending GCC with a multi-grain parallelism adaptation framework for MPSoCs", GCC for Research Opportunities Workshop, 2010

PATTERN BASED CACHE COHERENCY ARCHITECTURE FOR EMBEDDED MANYCORES



RESEARCH TOPIC:

Many-core systems, Memory coherence, Memory access patterns »

AUTHORS:

J. Marandola (USP), S. Louise, L. Cudennec

ABSTRACT:

Modern parallel programming frameworks like OpenMP often rely on shared memory concepts to harness the processing power of parallel systems. But for embedded devices, memory coherence protocols tend to account for a sizable portion of chip's power consumption. This is why any means to lower this impact is important.

Our idea for this issue is to use the fact that most of usual workloads display a regular behavior with regards to their memory accesses to prefetch the relevant memory lines in locale caches of execution cores on a manycore system.

SCIENTIFIC COLLABORATIONS: University of Sao Paulo (Brazil))

Context and Challenges

OpenMP is a successful and usual parallel programming paradigm. In a time when multi- and many- core systems are becoming prevalent even in embedded systems, parallelization is a key element for harnessing the processing power of these new platforms. But OpenMP behave better and is easier to utilize with hardware memory coherence, although the energy/power cost of communication associated is significant for the embedded world. Therefore any means to decrease the communication overhead would be a step toward a better use of OpenMP in embedded software

Main Results

In this work, we use the fact that memory accesses display usually very regular behaviors. Our contributions are the specifications of an IP for prefetching memory access patterns, and a hybrid protocol which extends the classic MESI/baseline architecture to reduce the control and coherence related traffic by an order of magnitude. The new protocol adds to the baseline (e.g. MESI) protocol a Pattern Home Node that allows for prefetching memory access patterns in cache memories (Fig. 1)

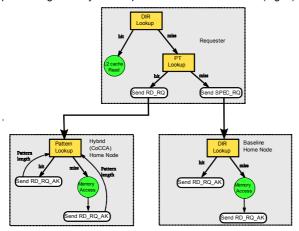
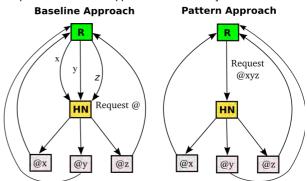


Fig. 1. The baseline protocol enhanced by the Pattern based protocol

For regular memory accesses which are a usual characteristic of lots of embedded softwares, the reduction in communication scales linearly with the number of prefetched lines, as seen in Fig. 2. As this is a prefetch unit, it also has an important influence on the performance of the application on such a system.



Total: 9 messages exchanged

Total: 7 messages exchanged

Fig. 2. Comparison between Baseline and Pattern based protocols. The number of communication decrease with the number of cache lines in the pattern.

We showed that for a first set of seven benchmark programs including h263 decoder and encoder, FFT, and Image filtering, a limited set of 1 to 11 prefetch 1D-patterns and 0 to 9 1D-invalidation patterns suffice to account for all the accesses. For 2D patterns the number is reduce to a maximum of 2.

In the same time, the execution time is reduced up to 70% for memory bound programs and about 30% for others.

Perspectives

We expect this to lower the power and energy consumption of embedded memory coherence. Nonetheless, even if we showed a drastic reduction in coherence messages and overall communication in meshed many-core processors, implementing the protocol in an energy and power aware simulator of the architecture is still future work. This would fully validate this approach.

RELATED PUBLICATIONS:

[1] J. Marandola, S. Louise, L. Cudennec, "Pattern Based Cache Coherency Architecture for Embedded Manycores,", Procedia Computer Science, Elsevier, ICCS 2016, pp 1542-1553.

[2] J. Marandola, S. Louise, L. Cudennec, J-T Acquaviva, D A Bader, " Enhancing cache coherent architectures with access patterns for embedded manycore systems", IEEE System on Chip (SoC), 2012 International Symposium on, pp 1-7.

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EUROSERVER: SHARE-ANYTHING SCALE-OUT MICRO-SERVER DESIGN



RESEARCH TOPIC:

Server architecture, Virtualization software

AUTHORS:

J. Martin, I. Dor, Y. Durand, M. Marazakis (FORTH), J. Goodacre (ARM), D. Fuin (STM), P. Carpenter (BSC), J. Thomson (ONAPP), E. Matus (TUDresden), A. Bruno (NEAT), P. Stenstrom (Chalmers)

ABSTRACT:

The EUROSERVER consortium has developed a micro-server solution for current cloud computer infrastructure. It combines efficient ARM v8 processors, innovative memory schemes and specific software solutions for virtualization. Its innovative architecture is based on interconnected compute "coherence islands" for an optimal balance between data locality and transfer efficiency. The structure is organized around several independent chiplets implementing the coherence islands. The coupling between chiplets is achieved via high-speed serial links. The system is integrated onto a cost-effective organic interposer solution.

SCIENTIFIC COLLABORATIONS: FORTH, ARM, STM, BSC, ONAPP Ltd, TU DRESDEN, Chalmers University of Technology, NEAT

Context and Challenges

The EUROSERVER design approach is focused on scalability and energy efficiency. Unlike the current PC-based approaches which place the processor as master of the platform, EUROSERVER introduces smaller cores within independent compute units using their own memory. In addition to the improvement of the global energy bill, this approach offers a major economic advantage since the cost of building and assembling smaller chiplets is lower than the cost of the equivalent monolithic system-on-chip.

Main Results

The EUROSERVER system architects have reconsidered the balance between memory, I/Os and computing within the system to accommodate architectural shift from "big" processors to more numerous but smaller cores. The platform structure is reorganised in accordance: (relatively) small chiplets bring the low-power cores together with the distributed infrastructure for memory and I/Os. At system level, a single substrate, called interposer, carries the high speed interconnection between the chiplets within a single System-In-package.

This approach not only brings the I/Os into the silicon device, in order to remove the energy overheads of a backplane bus, but its nano-technological device integration enables cost effective connectivity between compute units and I/O interfaces.

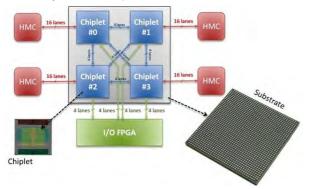


Fig.1: EUROSERVER compute unit structure

Each chiplet has its dedicated coherent memory space. But for the sake of software flexibility, memory may also be addressed globally by the applications: each compute unit allows remote access to its local memory through a system-level memory management unit, the hardware also supports direct memory access between the memories of multiple compute units, with a relaxed level of coherence that preserves efficiency.

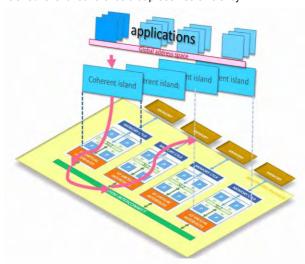


Fig.2: The applications can access any compute node memory across the different coherent island of each chiplet.

Perspectives

The EUROSERVER architecture paves the path for the use of "small" cores in micro-servers, with the perspective of x4 energy savings in server infrastructures. But the outcome is more general: this new approach to System-in-Package design enables application-specific optimisation for other applications, still with an economic model that reduces the cost of such device by an order of magnitude while potentially increasing the overall capabilities of a silicon device.

RELATED PUBLICATIONS:

[1] M. Marazakis, J. Goodacre, D. Fuin, P. Carpenter, J. Thomson, E. Matus, A. Bruno, P. Stenstrom, J. Martin, Y. Durand & I. Dor, "EUROSERVER: Share-anything scale-out micro-server design." in Proceedings of the 19th Design, Automation and Test in Europe Conference and Exhibition, DATE 2016, 14 March 2016 through 18 March 2016, pp. 678-683.

March 2016, pp. 678-683.
[2] Y. Durand, P. M. Carpenter, S. Adami, A. Bilas, D. Dutoit, A. Farcy, G. Gaydadjiev, J. Goodacre, M. Katevenis, M. Marazakis, E. Matus, I. Mavroidis & J. Thomson, "EUROSERVER: Energy Efficient Node for European Micro-Servers," 2014 17th Euromicro Conference on Digital System Design, Verona, 2014, pp. 206-213.



A 4X4X2 HOMOGENEOUS SCALABLE 3D NETWORK-ON-CHIP CIRCUIT WITH 326 MFLIT/S 0.66 PJ/BIT ROBUST AND FAULT TOLERANT ASYNCHRONOUS 3D LINKS

RESEARCH TOPIC:

3D technology, TSV, NoC, asynchronous logic, thermal dissipation, test, fault tolerance

AUTHORS:

P. Vivet, Y. Thonnart, R. Lemaire, C. Santos, E. Beigné, F. Darve, I. Miro-Panades, D. Lattard, D. Dutoit, F. Clermidy

ABSTRACT:

By shortening communication distance across dies, 3D technologies are a key to continued improvements in computing density. This work presents a homogeneous 3D circuit composed of regular tiles assembled using a 4x4x2 network-on-chip, using robust and fault tolerant asynchronous 3D links, providing 326 MFlit/s @ 0.66pJ/bit, fabricated in a CMOS 65nm technology and using TSVs in a Face2Back configuration. The self-adaptation to temperature of the 3D NoC link performances thanks to asynchronous logic has been exhibited by hotpots injection in the circuit. The circuit scalability has been verified in simulation up to 8 circuit layers.

SCIENTIFIC COLLABORATIONS: TIMA (Grenoble)

Context and Challenges

For High Performance Computing (HPC), the never ending quest of additional computing capability is hitting strong limits, mostly the power wall and the memory wall. The 3D technology by using so-called TSVs (Through Silicon Via) offers the possibility to integrate more cores, closer to the memories, with reduced power consumption thanks to smaller communication distances [3]. For such 3D technologies, the main challenges are to design energy efficient 3D communication infrastructure, to offer test strategy and to handle related power and thermal dissipation issues

Main Results

A complete 3D asynchronous Network-on-Chip architecture is designed and proposes a scalable and modular packet switched communication infrastructure, with a 3D mesh-based topology, implementing four 3D vertical links. The asynchronous logic allows to get rid of any timing assumptions between the adjacent dies. Each 3D link is composed of a routing stage, a pipeline stage, a design-for-test stage, and a final stage with a logical interface composed of µ-buffer cells. These cells provide level shifter, ESD protection, and buffering capability to drive a TSV middle. The 3DNOC is then fully implemented with a standardcell methodology, without the requirement of a complex PHY for chip-to-chip interface communication.

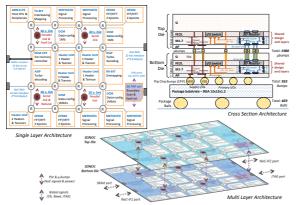


Fig. 1. 3DNOC circuit: architecture, cross section, and layers

The 3DNOC circuit [2] is composed of 2 layers, and targets a 4G Telecommunication baseband application. The circuit is implemented in a 65nm technology, using 1980 TSVs middle.

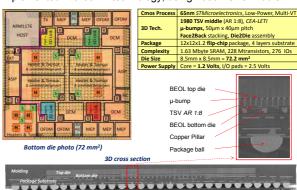


Fig. 2. 3DNOC circuit: floorplan, technology, and cross section.

For reliability aspects, a fault tolerant architecture is proposed with spare TSVs and a two steps test-and-repair mechanism based on JTAG protocol. Four different 3D NOC vertical links are implemented, offering an aggregate bandwidth of 8 GByte/sec. The 32-bit 3D link offer a throughput of 326MFlit/s and an energy efficiency of 0.66pJ/bit, which represents respectively +20% and +40% better performances compared to state of the art.

The asynchronous logic is robust to temperature variation, which has been exhibited by hotspot injection with a live demonstration. The scalability of the 3DNOC circuit has been further studied in simulation, showing the correctness of its power grid network and it's thermal dissipation capabilities [1].

Perspectives

This work is a first step towards building large scale many-core systems. This robust, scalable and modular communication architecture can be applied to homogeneous or heterogeneous multi-cores. The next step consists in applying such 3DNOC to chiplet-based 3D partitioning where large dies are partitioned in smaller dies, called chiplet, assembled in 3D onto an active interposer, interconnected with such a 3D NoC [3].

RELATED PUBLICATIONS:

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3D DESIGN-FOR-TEST ARCHITECTURE BASED ON IJTAG/IEEE1687 USING CHIPLET-FOOTPRINTS FOR TESTING A MULTI-CHIPLET ACTIVE INTERPOSER 3D SYSTEM

RESEARCH TOPIC:

3D testability, Know Good Die, TSV defect, IJTAG, IEEE 1687

AUTHORS:

J. Durupt, P. Vivet, J. Schloeffel (Mentor Graphics)

ABSTRACT:

In order to increase circuit yield, 2.5D technology have been introduced to partition a single large circuit in multiple circuits, which are primary tested, then assembled in 3D onto a passive silicon interposer. Active interposer is nowadays envisioned in order to provide added values within the interposer and 3D system. In this work, a 3D Design-for-Test architecture is proposed for testing multi-chips stacked onto an active interposer. The 3D test architecture allows the modular test of any chiplets; it is implemented using IJTAG IEEE1687 standard, and offers easy test pattern retargeting from chiplet pre-bond test to the 3D circuit final test.

Context and Challenges

3D stacking technology using TSVs (Through Silicon Via) offers new opportunities by using heterogeneous technologies. Chiplet partitioning and Active Interposers are envisioned to provide further added value in the system while preserving cost [2]. For such 3D architecture, testability is a clear challenge, with new defect sources (TSV cracks, mis-alignement, etc), where a Known Good Die (KGD) test strategy must be defined. The test architecture must offer pre-bond test of the chiplets (before 3D assembly), and the final test (after 3D assembly), while testing all die features to ensure high test coverage of logic, memories, and 3D interconnects [3]. A last challenge concerns the Automatic Test Pattern Generation (ATPG) engineering effort, where an easy re-targeting of test patterns from pre-bond to post-bond test should be proposed to reduce test development efforts.

Main Results

For testing such large systems, with high level of maturity, a complete 3D Design-for-Test architecture is proposed within the active interposer [1].

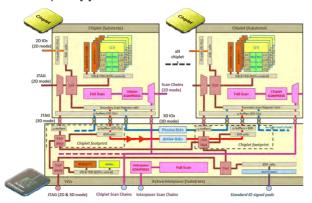


Fig. 1. Active Interposer 3D Test Architecture Overview

It is based on two main test structures: i) a IJTAG test interface, using IEEE1687 standard, which offers access to Boundary Scan Chains, for testing individually all 3D interconnections (either passive links or active links), and for controlling the memories

BIST (Built-In-Self-test); ii) a full scan network using test compression, in order to test the full logic stack, with a reduced pin count at the 3D interface.

The main design innovation is coming from the chiplet footprint proposal, allowing to test individually each chiplet, either in standalone for pre-bond test or attached onto the active interposer for final test. Moreover, a specific care must be taken in order to provide the required test pads for the probe card, since the small pitch $\mu\text{-bumps}$ cannot be directly accessed by any probe card.

Regarding test flow, a complete ATPG methodology has been developed allowing the easy test pattern retargeting of chiplet test patterns to interposer-level chiplet test patterns. The test flow is based on IEEE1687 IJTAG standard, and implemented using Tessent tools from Mentor Graphics.

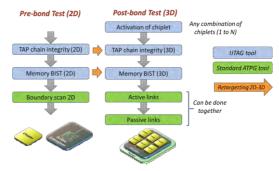


Fig. 2. 3D test pattern generation, using Mentor Tessent tools.

Perspectives

The proposed 3D test architecture allows to test large scale 3D system. It has been applied to the INTACT circuit [2], which is currently in fabrication; the test architecture will then be exercised on an industrial automatic test equipment.

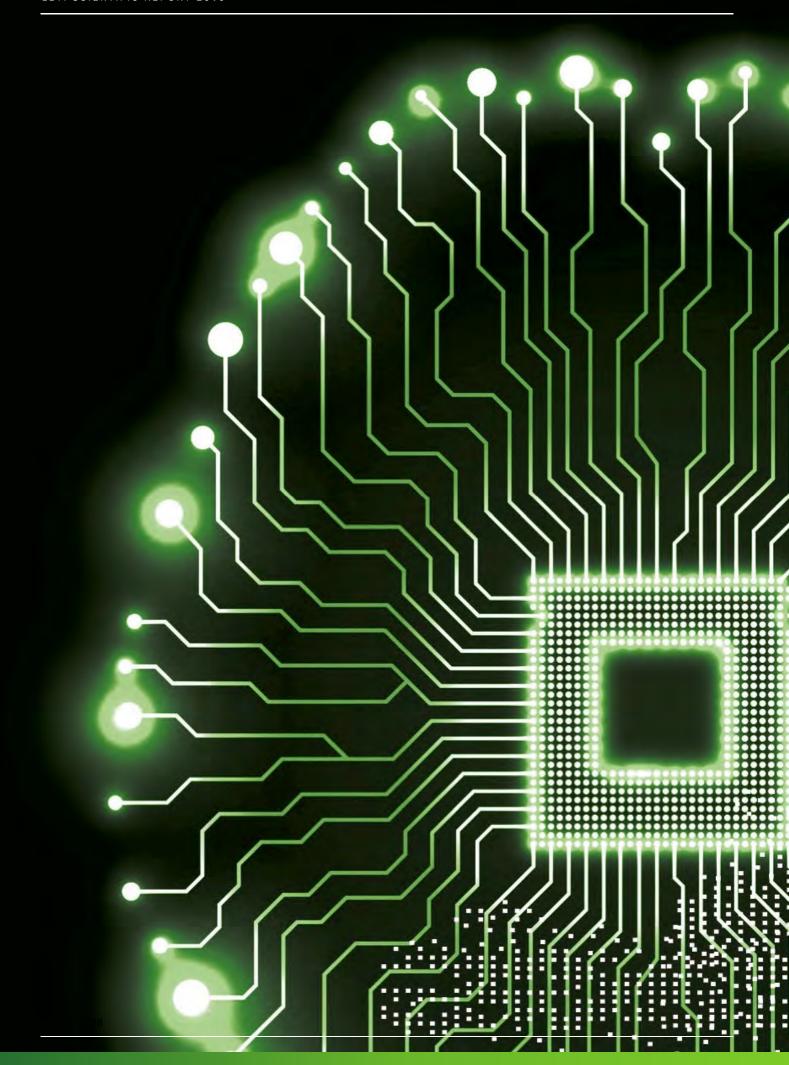
Regarding standardization aspects, the test architecture is based on existing test standard, namely IEEE1687, and implemented using a state-of-the-art test tool chain. The main challenge and next step is to adopt the proposed test architecture, within the ogoing 1848 3D test standard under definition.

RELATED PUBLICATIONS:

[1] J. Durupt, P. Vivet, J. Schloeffel, "IJTAG supported 3D DFT using Chiplet-Footprints for testing Multi-Chips Active Interposer System", European Test Symposium, ETS'2016, Amsterdam, Nederland's, May 2016.

[2] D. Lattard, L. Arnaud, A. Garnier, N. Bresson, F. Bana, R. Segaud, A. Jouve, H. Jacquinot, S. Moreau, K. Azizi-Mourier, C. Chantre, P. Vivet, G. Pillonnet, F. Casset, F. Ponthenier, A. Farcy, S. Lhostis, J. Michailos, A. Arriordaz, S. Cheramy, "ITAC: a complete 3D integration test platform", 3DIC'2016 Conference, San Francisco, USA, Dec 2016.







3.

WIRELESS COMMUNICATIONS

- Channel Awareness
- RF Analog to Information Converter
- Ultra-Wide Band
- Power Amplifiers
- Test of mmW circuits

CHANNEL AWARE RECEIVER FRONT END FOR LOW POWER 2.4 GHZ WIRELESS SENSOR NETWORK: A SYSTEM LEVEL ANALYSIS



Channel aware receiver, Low Noise Amplifier (LNA), RF front end, WSN

AUTHORS:

Jennifer Zaini, Frédéric Hameau, Thierry Taris (IMS Bordeaux), Dominique Morche, Le Quang Vinh Tran (ERCOM Telecom) and Patrick Audebert

ABSTRACT:

In this paper, a system level analysis for channel aware receiver is described. Based on a real-time estimation of the received power, this study proposes an optimization of the sensitivity ranges for such adaptive receiver. From the performances vs power consumption trade-off and a statistical analysis of the received power, smart threshold optimization leads to a significant increase of Wireless Sensor Network (WSN) battery lifetime by factors up to 5 or 6.

SCIENTIFIC COLLABORATIONS: IMS Bordeaux

Context and Challenges

As wirelessly connected objects are increasingly inviting themselves into daily life, the research field of the Internet of Things (IoT) is becoming a hot topic of interest. The wide development of WSNs unveils new design requirements in terms of energy-efficiency and form factor. Standards like IEEE802.15.4 or Bluetooth Low Energy (BLE) focusing on short-range low power operation, optimize the trade-off between performance and power consumption. Circuit structures have already been designed to achieve low power consumption with acceptable performance. In order to guarantee the QoS for every channel condition, a receiver is traditionally designed to only address the worst case. However, the probability to be in the worst case (-90dBm) is seldom happening and the highest probability of the received signal power is ranging from -80dBm to -70dBm, as depicted in Fig. 1. In an uni-performance receiver, 100% of the usage time is dedicated to the highest power consumption whereas a channel aware receiver consists in scaling its performances based on the variations of the channel. Therefore, most of the time the receiver performances can be significantly relaxed, as well as its power consumption.

Main Results

Fig. 1 highlights two thresholds (T1 and T2) for the received signal power, defining the three reconfiguration modes of the tunable receiver. The gain G on the battery lifetime depended on the usage time percentage, the power consumption for each mode normalized with respect to the power consumption of the high performance mode.

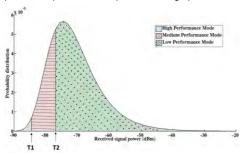


Fig. 1 Probability distributions of the received signal power at the input for three reconfiguration modes.

Fig. 2 depicts the gain reached for every thresholds configuration according to the power consumption of the State of the Art Receivers and the usage time defined in Fig. 1. The best configuration offers a gain of 5 with T1= -85dBm and T2= -75dBm. These two thresholds define the limits of the modes. It yields the best trade-off between performances and power consumption of the receiver.

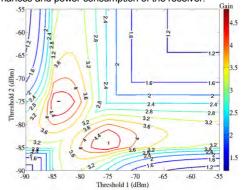


Fig. 2 Thresholds optimization for three reconfiguration modes

This work shows that if the receiver is for 76% and 23% of its usage time in respectively low and medium performance modes with a power consumption divided by respectively 7 and 3, and the remaining time at the worst case, the battery lifetime of the receiver part is multiplied by more than 5.

Perspectives

A three modes receiver with reconfiguration modes depending on the state of the channel is a promising solution for power consumption and form factor reductions. With the defined thresholds, the specifications on the blocks of the receiver can be derived. The perspectives are to proposed tunable blocks such as LNA and/or mixer respecting these three performances modes.

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[2] J. Zaini, F. Hameau, T. Taris, D. Morche, L. Q. V. Tran, and P. Audebert, "Channel aware receiver front end for low power 2.4 GHz Wireless Sensor Network: A system level analysis," in 2016 14th IEEE International New Circuits and Systems Conference (NEWCAS), 2016, pp. 1–4.

NON-UNIFORM WAVELET BANDPASS SAMPLING FOR COMPRESSIVE RF FEATURES ACQUISITION



RESEARCH TOPIC:

Analog to information converter, cognitive radio, compressive sensing, feature extraction

AUTHORS:

Michaël Pelissier, Christoph Studer (Cornell University),

ABSTRACT:

Feature extraction from wideband radio-frequency (RF) signals, such as spectral activity, interferer energy and type, or direction-of-arrival, finds use in a growing number of applications. Compressive sensing (CS)-based analog-to-information (A2I) converters enable the design of inexpensive and energy-efficient wideband RF sensing solutions for such applications. However, most A2I architectures suffer from a variety of real-world impairments. We propose a novel A2I architecture, referred to as non-uniform wavelet bandpass sampling (NUWBS). Our architecture extracts a carefully-tuned subset of wavelet coefficients directly in the RF domain, which mitigates the main issues of most existing A2I converters.

SCIENTIFIC COLLABORATIONS: Cornell University

Context and Challenges

CS-based A2I converters that leverage spectrum sparsity are a promising solution for wideband RF feature acquisition applications. CS enables the acquisition of larger bandwidths with relaxed sampling-rate requirements, thus enabling inexpensive, faster, and potentially more energy-efficient solutions than traditional Nyquist analog-to-digital converters (ADCs).

Main Results

We propose a novel A2I converter for cognitive RF receivers, i.e., radio receivers that are assisted with an A2I converter specifically designed for RF feature extraction. As illustrated in Fig. 1, the A2I converter bypasses conventional RF circuitry and extracts a small set of features directly from the incoming RF signals in the analog domain. The acquired features can then be used by the RF frontend for parameter tuning (e.g., of filters) or by the digital signal processing (DSP) stage. Our approach, referred to as non-uniform wavelet bandpass sampling, combines wavelet preprocessing with non-uniform sampling, which mitigates the key issues of existing A2I solutions, such as signal noise, aliasing, and sensitivity to clock jitter.

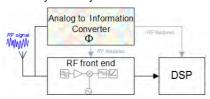


Fig1 : Overview of a cognitive radio receiver: A traditional RF front-end is enhanced with an A2I converter. that extracts RF features directly from the incoming analog RF signals

The operating principle of NUWBS is illustrated in Fig. 2. NUWBS first multiplies the input signal x(t) with a wavelet comb and then, integrates over the support of each wavelet, and subsamples the resulting wavelet coefficients. In discrete time, the equivalent compressive sensing matrix Φ for NUWBS can be described by taking a small set Ω of rows of a wavelet frame. Wavelets can be generated efficiently in hardware. In particular, we are interested in Gabor or Morlet-like waveforms with a given center frequency f° , bandwidth $(1/\tau)$, and phase (determined by the sample instant).

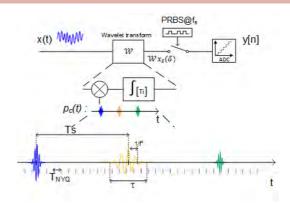


Fig2: Generic serial NUWBS architecture to acquire Gabor frame or wavelet samples.

Each wavelet sample corresponds to point-wise multiplication of the sparse signal spectrum with the bandpass filter equivalent to the Fourier transform of the wavelet. Hence, each wavelet captures a different portion of the sparse spectrum with a different phase and bandwidth. Such wavelets can be generated in hardware by leveraging extensive prior work in the field of ultrawideband (UWB) impulse radio.

NUWBS has the following key advantages over existing methods. First, the analog wavelet transform reduces the bandwidth of the input signal x(t), which relaxes the bandwidth of the sample-and-hold (S&H) circuit and the ADC. Second, NUWBS enables full control over a number of parameters, which enables one to tune the wavelets to the signal class to be acquired. We have shown that NUWBS exhibits similar success and failure rates as predicted by the theoretical I1-norm phase transition graph. Hence, NUWBS enables hardware-friendly RF feature extraction while delivering a performance that is close to the theoretical performance limits.

Perspectives

Our solution finds potential broad use in a variety of RF receivers targeting spectrum awareness or assisting conventional RF chains with tuning parameters. The proof of concept relying on custom ASIC design of NUWBS solution is part of ongoing work.

RELATED PUBLICATIONS:

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ESTIMATION METHOD OF POWER SPECTRAL DENSITY FOR ULTRA WIDEBAND IMPULSE RADIO SIGNAL CMOS IMPLEMENTATION OF A SPECTRAL CALIBRATION SYSTEM FOR IR-UWB TRANSMITTERS

RESEARCH TOPIC:

Fourier transform, Impulse radio, Instantaneous frequency, Power spectral density, Transmitter calibration, Ultra-wideband

AUTHORS:

A. Goavec, M. Zarudniev, R. Vauché (IM2NP), F. Hameau, J. Gaubert (IM2NP), E. Mercier

ABSTRACT:

For about a decade, Ultra-WideBand (UWB) technology has demonstrated its potential for high and low data rate short range wireless communications. Moreover it offers high localization performances by accurate measurement of the time of flight thanks to its robustness to multipath fading [1]. But, according to the state of the art, in order to comply with existing power emission constraints, UWB transmitters cannot completely exploit their promising features in terms of cost, consumption, spectral efficiency or emitting range. The proposed method allows future hardware CMOS implementation of self-calibration systems for IR-WUB TX.

SCIENTIFIC COLLABORATIONS: IM2NP, Marseille

Context and Challenges

In order to generate a signal with ultra-large bandwidth, a way is to use impulse modulation of short pulses since this allows to reduce the complexity and the cost of the transmitter [2]. But in order to enable the coexistence and dissemination of UWB systems and to establish communications between UWB devices, the power emission constraints for transmitters, defined by regulation entities (FCC, ETSI) and standards (IEEE) are very challenging to respect because of steep power limits. Moreover Impulse Radio (IR) circuits are disturbed by Process-Voltage-Temperature (PVT) variations that cause performance degradations [2], impacting notably the emitted pulse Power Spectral Density (PSD) shape. For example, the PSD in Fig. 1 is asymmetrical and it is above the mask around 500 MHz.

Main Results

In order to guarantee that the pulse PSD fits on the emission mask, it could be interesting to build smart on-chip calibration system for IR-UWB transmitters (TX) which have often a lot of control possibilities. The aim of such systems would be to modify the emitted pulse in order to fix the mask exceedance with minimum repercussions on the other parts of the PSD (Fig. 1 -[3]).

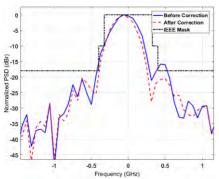


Figure 1. Example of a PSD before and after correction

In Fig. 2 such a calibration system is represented with an IR-UWB transceiver. On the TX side, a calibration loop is used in

order to adjust the transmitter emission before the antenna when the TX is in calibration mode. This loop can be disconnected from the transceiver thanks to a calibration switch in order to not disturb its operation in the normal TX mode. Then, information would be extracted from the output of the transmitter and a control method should act on the possible control knobs of the transmitter in order to calibrate the PSD [3].

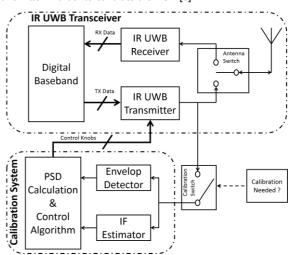


Figure 2. PSD Calibration System & IR-UWB Transceiver

To extract the required information from the signal, it was proposed in [3] a generic way to approximate the impulse radio signal in time domain by a simple representation, based on the envelope and the Instantaneous Frequency (IF) of the signal, in order to estimate the frequency domain characteristics of the signal on a digital embedded unit.

In [4] it was shown by simulation that it is feasible to extract onchip the envelope and the IF with CMOS integrated devices.

Perspectives

With the possibility to estimate on CMOS transistor level the PSD of an impulse signal, it is conceivable to implement a calibration system which could improve IR-UWB TX performances.

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 [3] A. Goavec, M. Zarudniev, R. Vauché, F. Hameau, J. Gaubert and E. Mercier, "An Efficient Method of Power Spectral Density Estimation for On-Chip IR-UWB Transmitter Self-Calibration," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 3, pp. 686-695, March 2017.

 [4] A. Goavec, R. Vauché, J. Gaubert, F. Hameau, M. Zarudniev and E. Mercier, "Instantaneous frequency measurement for IR-UWB signal in CMOS 130 nm," 2016
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RECONFIGURABLE POWER AMPLIFIER IN RF SOI TECHNOLOGY



RESEARCH TOPIC:

Power Amplifier (PA), SOI, Reconfigurable PA, Tunable matching network (TMN)

AUTHORS:

P. Ferris, A. Serhan, A. Giry, J.-D. Arnould (IMEP), J.-M. Fournier (IMEP)

ABSTRACT:

RF SOI technology is a key enabling technology for the integration of high performance RF power amplifiers and front-end modules. In this research work, a high efficiency reconfigurable multimode multiband power amplifier and a low loss tunable output matching network have been designed and integrated in a 130nm RF SOI technology.

SCIENTIFIC COLLABORATIONS: IMEP, Grenoble

Context and Challenges

The need for wireless devices with smaller form factor and reduced cost is driving research towards flexible power amplifiers (PA) with a high integration level to efficiently afford multimode and multiband requirements for LTE-A and upcoming 5G applications. The concept of reconfigurable PA appears as a promising solution to reduce the size and cost of future multimode multiband PA (MMPA) modules. RF SOI technology with high resistivity substrate paves the way to high performance reconfigurable PAs thanks to high efficiency LDMOS power devices and low loss RF switches [1]. In this work, a reconfigurable MMPA covering several power modes and frequency bands was designed. Since PA performances are very sensitive to load mismatch, a PA load tuning system based on a low loss tunable output matching network (TOMN) has also been studied. Both solutions were implemented in a 130nm RF SOI technology

Main Results

A two-stage reconfigurable SOI MMPA addressing 2G/3G/4G modes and covering more than 10 frequency bands has been designed and characterized [2]. The circuit shown in Fig.1. occupies an area of 2.9mm². In 2G mode, a saturated output power of 34.6/35.5dBm with a corresponding power added efficiency (PAE) of 61/53% was measured at 800/900MHz. In 3G/4G mode, a linear output power higher than 28/27dBm with a PAE higher than 34/33% while keeping adjacent channel leakage power ratio (ACLR) less than -36/-33dBc was measured with WCDMA and LTE signals respectively in the 700-900MHz frequency range. At 900MHz, up to 39/37% PAE is achieved with WCDMA/LTE signals. Up to 15% boost in PAE was achieved at 700MHz and 900MHz by using reconfigurable matching networks, which validates the usefulness of the proposed reconfigurable PA architecture. Besides, a low loss TOMN using high-Q digitally tunable capacitors has been designed for PA load mismatch correction [3]. Design equations were developed and a prototype has been sent to fabrication. The proposed TOMN is able to recover any impedance mismatch up to 4:1 VSWR with less than 2dB of insertion loss as shown in Fig. 2. When combined with a SOI PA, it allows to maintain optimal performances even under high load mismatch.

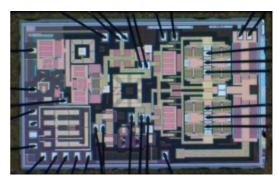


Fig.1. Micro-photograph of the reconfigurable SOI MMPA

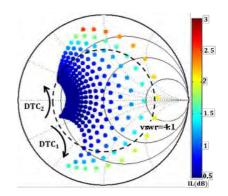


Fig.2. Impedance coverage and insertion loss (IL) of the **SÕI TOMN**

Perspectives

This work demonstrates that RF SOI is capable of delivering PA with competitive performances over conventional GaAs-based cellular PAs. Future work will focus on high efficiency linear PA architectures and design for wideband 5G applications.

RELATED PUBLICATIONS:

[1] A.Giry, "SOI CMOS PA for Mobile Applications," in IEEE MTT-S International Microwave Symposium, Workshop WSA, Tampa, Jun. 2014

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[3] A. Serhan, P. Ferris, A. Giry, "Broadband SOI PA with Tunable Matching Network for Improved LTE Performances under High VSWR", in 23rd IEEE International

Conference on Electronics, Circuits and Systems (ICECS), Monte Carlo, Monaco, December 11-14, 2016



BUILT-IN TEST OF MILLIMETER-WAVE CIRCUITS BASED ON NON-INTRUSIVE SENSORS



RESEARCH TOPIC:

mm-Wave circuit testing, built-in test, nonintrusive sensors, alternate test.

AUTHORS:

E. de Foucauld, A. Siligaris, A. Dimakos (TIMA) H. Stratigopoulos (TIMA) S. Mir (TIMA)

ABSTRACT:

This work addresses the high-volume production test problem for millimeter-wave (mm-Wave) circuits. We propose a built-in test solution that has two important attributes. Firstly, it is based on non-intrusive sensors that are totally transparent to the mm-Wave circuit. They monitor variations in the performances of the mm-Wave circuit indirectly by virtue of offering an "image" of process variations. Secondly, the non-intrusive sensors operate at DC or low-frequency, thus dramatically simplifying the test of the mm-Wave circuit. We demonstrate the concept on a 65nm 60GHz mm-Wave low-noise amplifier (LNA).

SCIENTIFIC COLLABORATIONS: TIMA, Grenoble

Context and Challenges

The design of mm-Wave circuits and systems has several challenges since it requires accurate modeling of active devices, passive components, interconnects, and transmission lines and it suffers largely from process, supply voltage, and temperature variations. Recent efforts focus on increasing the yield of mm-Wave circuits through calibration, adaptive circuit strategies, and self-healing algorithms. The high-volume production test of mm-Wave circuits and systems is a major challenge towards their widespread adoption. In this work, we explore an alternative solution based on non-intrusive built-in sensors that have the comparative advantage of being totally transparent to the mm-Wave circuit without degrading its performance and without requiring any co-design.

Main Results

The non-intrusive sensors are process control monitors integrated on the same die together with the mm-Wave circuit and offer an "image" of process variations. They incur low area overhead, and are tested at DC or low-frequency. The 60GHz mm-Wave LNA and the non-intrusive sensors have been designed in STMicroelectronics 65nm CMOS bulk technology.

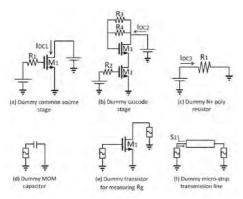


Fig.1: Non-intrusive variation-aware sensors

We used a dummy common source stage composed of transistor M1 and resistor R1, as shown in Fig. 1(a) and (b), a dummy cascode stage composed of transistors M2 and M3 and resistors R2, R3 and R4, as shown in Fig. 1(b), noticing that the second and third stages that use a cascode topology are built from identical components. These dummy analog stages aim at monitoring the process variations that influence the gate and drain transconductances of the transistors of the 60GHz mm-Wave LNA. The prediction error of alternate test is expressed in terms of several error metrics. This methodology gives us the best non-intrusive sensors to get S21, S11, S22, and IIP3 parameters. Fig. 2 shows the layout highlighting the placement of the LNA and of the various non-intrusive sensors on the die.

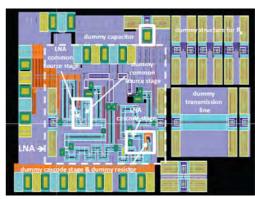


Fig.2: Dummy components in LNA layout

Perspectives

The non-intrusive sensors can be used for enabling a low-cost alternate test approach where the performances of the mm-Wave circuit are inferred implicitly from the outputs of the non-intrusive sensors. The perspective of this work is the possibility of testing a transceiver, receiver and emitter with such methodology. The complementary study will be the correlation of all sensors of each blocks to avoid redondancy.

RELATED PUBLICATIONS:

[1] A Dimakos; H. Stratigopoulos; A. Siligaris; S. Mir; E. De Foucauld, "Built-in test of millimeter-Wave circuits based on non-intrusive sensors", 2016 Design,

[2] A. Dimakos, H. Stratigopoulos, A. Siligaris, S. Mir, E. De Foucauld, Bolintar lest of minimeter-wave circuits based on hori-mutisive seriors, 2010 Design, Automation & Test in Europe Conference & Exhibition (DATE), Pages: 505 – 510
[2] A. Dimakos, H. Stratigopoulos, A. Siligaris, S. Mir, E. De Foucauld, "Parametric Built-In Test for 65nm RF LNA Using Non-Intrusive Variation-Aware Sensors", Journal of Electronic Testing: Theory and Applications, Ed. Springer, Vol. 31, No. 4, pp. 381-394, août 2015
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STUDY AND REDUCTION OF VARIABILITY IN 28 NM FDSOI TECHNOLOGY



RESEARCH TOPIC:

FDSOI, Variability, Back-gate, Auto-biasing,

AUTHORS:

E. de Foucauld, Z. Wei (UNS-EPOC), G. Jacquemod (UNS-

ABSTRACT:

Using FDSOI technology, we propose a new complementary structure based on Back-gate cross-coupled inverters offering a fully symmetrical operation. Monte Carlo (MC) simulations of the complementary outputs crossing point exhibit a mean value of VDD/2=500mV, and the standard deviation is about 2.7mV. Moreover, this topology enables a Voltage Controlled Ring Oscillator (VCRO) with an even number of inverters. This latter feature makes it easy to perform quadrature VCOs (QVCO), which are used in RF receiver architectures for image frequency rejection.

SCIENTIFIC COLLABORATIONS: University of Nice-Sophia Antipolis

Context and Challenges

As the technology scales down into deca-nanometer range the variation of the threshold voltage (VTh) becomes an ever larger problem. We expect a lot of variability between adjacent transistors on the same die and the dopant variation will cause directly a threshold voltage mismatch between adjacent transistors (VTh variability). While the digital blocks continue to shrink, analog one hardly shrinks at all. For example ring oscillators (digital oscillators without passive elements) are known to exhibit high phase noise, but this design will address aggressively the size (only inverters) and power consumption reduction. We use in this work the efficient back-gate biasing offered by the FDSOI MOS transistor to compensate the mismatches between the different inverters of the ring oscillator to decrease jitter and phase noise.

Main Results

Using FDSOI technology, we propose a new complementary structure. The main idea is as follow: the NMOS transistor, the faster one, is going to accelerate the conduction of the slower PMOS transistor, and reciprocally. So, connecting the outputs of each inverter to the back-gate of the other, the faster stage will accelerate the slower one

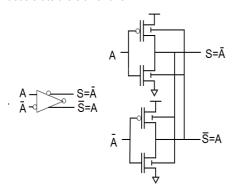


Fig.1: Inverter schematic

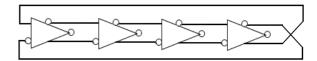


Fig.2: Ring oscillator with even number of inverters

This new topology (complementary inverter) offers two other advantages very important for ring oscillator realization. The first one concerns the duty cycle, which has to be closed to 50%. Secondly, this topology enables an oscillator with an even number of inverters (Fig.2). This latter feature makes it easy to perform a quadrature VCO (QVC0: four identical outputs (same amplitude and same frequency) but with different phases (0°, 90°, 180° and 270°)). This QVCO topology is used in RF receiver architectures with image frequency rejection.

To validate our concept, we have realized a transient simulation of an 8 fully complementary inverters ring oscillator. The measured period is about T = 88 ps, which corresponds to a frequency oscillation of 11.36 GHz. If we compare the different phases at VDD/2, we find a value of 11ps (T/8), corresponding to a phase step of 45°. Then, we have verified this characteristic by estimating the phase between two outputs and the standard deviation using Monte Carlo simulations. The mean value of the phase is 45° (corresponding to T/8) and the standard deviation is σ =0.13° (6 σ #0.8° \Rightarrow 1.8%). We have simulated a standard deviation about σ =230MHz of the oscillation frequency variation

Perspectives

We have demonstrated that such an inverter works like an "ideal" inverter with an infinite gain. This new topology can be used to implement a ring oscillator (or VCO) in order to increase its performances. Nevertheless, a better trade-off between jitter, phase mismatch and power consumption has to be achieved for a given frequency of the oscillator. Moreover, these features will be increased if we decrease the voltage supply (0.8V or less). These simulated results have to be validated on a test-chip. A frequency synthesizer based on a VCRO with Back-gate autobiasing technique will be manufactured.

RELATED PUBLICATIONS:

[1] Z. Wei, G. Jacquemod, P. Lorenzini, F. Hameau, E. de Foucauld & Y. Leduc, "Study and reduction of variability in 28nm Fully Depleted Silicon on Insulator

technology", Journal of Low Power Electronics, Vol 12, N° 1, 2016, pp 64-73 [2] G. Jacquemod; Z. Wei; J. Modad; Y. Leduc; P. Lorenzini; F. Hameau; E. De Foucauld, "Study and reduction of variability in 28 nm FDSOI technology", 2015 International Workshop on CMOS Variability (VARI) Year: 2015 Pages: 19 - 22,

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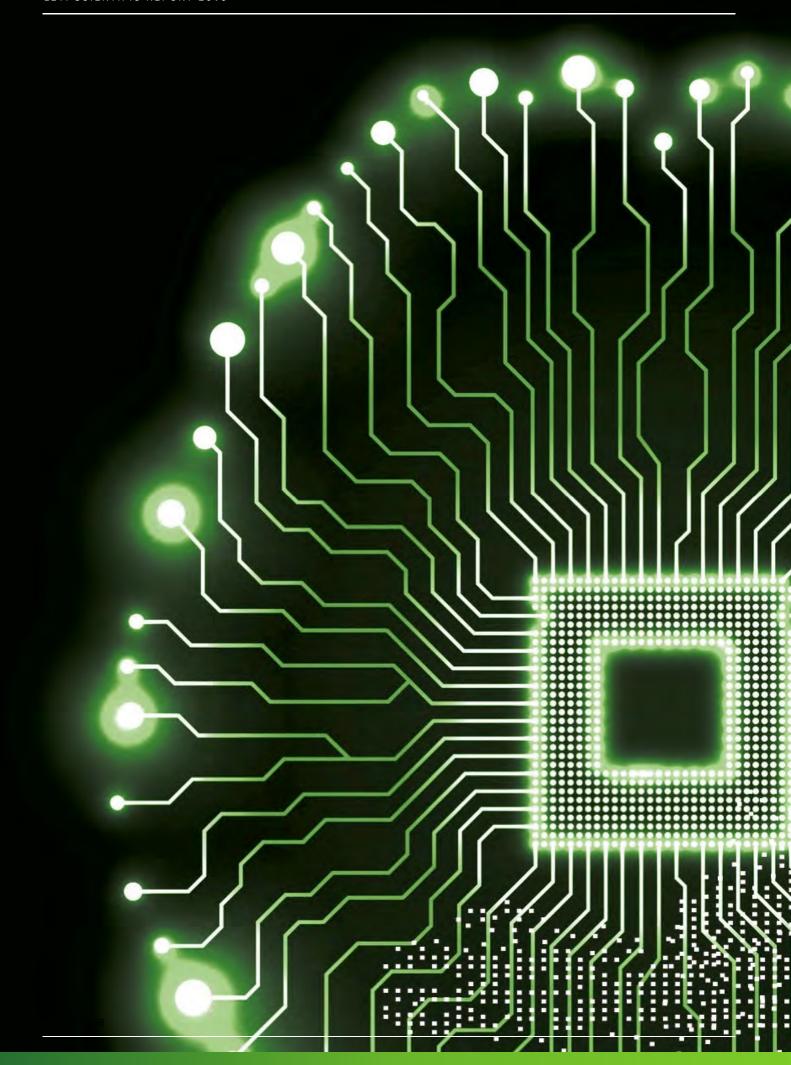
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SENSORS & ENERGY

- Multi-Sensors Fusion & Navigation
- IoT Wake-up Controller
- Sensors
- Imagers
- Power Converter
- Energy Harvesting



LIFELONG EXPLORATORY NAVIGATION INTEGRATING PLANNING, NAVIGATION AND SLAM FOR AUTONOMOUS MOBILE ROBOTS WITH FINITE RESOURCES

RESEARCH TOPIC:

Robot, autonomous, intelligence, learning, SLAM, planning

AUTHORS:

F. Mayran de Chamisso, L. Soulier, M. Aupetit (HBKU, Qatar)

ABSTRACT:

One challenge of robotics is to have robots move autonomously in order to accomplish any mission they are charged with, with time and resource constraints and possibly without prior knowledge of the environment. It requires the robot to maintain an abstract representation of the environment (map), be able to localize itself and navigate within this map, while handling dynamics and avoiding obstacles. The goal of this thesis [1] is to handle all these problems as a whole by developing methods to navigate on partially-known graph-representations of the map and even to voluntarily degrade this representation, in order to release memory and computational constraints, without preventing the robot from performing its mission.

SCIENTIFIC COLLABORATIONS: Hamad Bin Khalifa University, Qatar

Context and Challenges

Autonomous navigation is a canonical problem of robotics that is addressed by an extended literature. Nevertheless, we are thinking that many results cannot scale easily to embedded system (with computational and memory constraints) and unlimited environments.

Main Results

In order to achieve the thesis objectives, several methods have been developed.

First of all, we extended the capacities of graph-based navigation by adding the possibility to explore unknown part of the map, in search of shortcuts. This algorithm, called EDNA* [1] is illustrated in Figure 1.

Then, the graph-map is built by detecting remarkable places. Practically, a range sensor is used to compute a local occupancy grid, whose topology is analysed to extract the nodes of the graph-map [2].

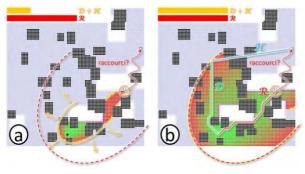


Fig 1 EDNA*: navigating on partially known graph. (a) a potential shortcut is discovered. (b) a shortest path is searched on known-graph until an heuristic decides that the shortcut is worth trying.

While navigating within the graph, position uncertainties are propagated in a way that help to limit the number of hypothesis for loop-closure. Then, disambiguation is performed through active exploration of the local map, leading to valid loop closure

and map correction.

All the above method have been successfully tested on large simulated environment (cf. Figure 2) but also on a real robot, within an office environment.

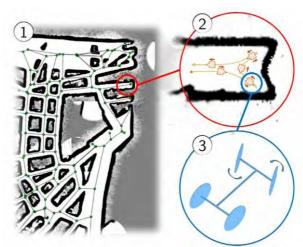


Fig 2 navigating on graph.

- (1) A robot navigate on "large scales", here an entire city, using a graph-map (NB, occupancy grid is displayed only for visualisation purposes).
- (2) It can perform manoeuvres using dense but local information ("medium scales").
- (3) On "smaller scales" it perform local actions.

Eventually, we developed technics to prune the graph-map in a way that allows to adjust graph-size with respect to the acceptable loss of optimality for the navigation cost.

Perspectives

Our robotic platform will be used to demonstrate that this works release resources that will be able to be used to higher level functions (for instance, people or object fetching).

RELATED PUBLICATIONS:

- [1] F. Mayran de Chamisso and M. Aupetit, Michaël, "Lifelong Exploratory Navigation: integrating planning, navigation and SLAM for autonomous mobile robots with finite resources", PhD report, Paris Saclay 2016.
- [2] F. Mayran De Chamisso, L. Soulier and M. Aupetit, "Exploratory Digraph Navigation Using A*" International Joint Conference on Artificial Intelligence (IJCAl'15), 2015.
- [3] F. Mayran de Chamisso, F.; L. Soulier and M. Aupetit, "Robust topological skeleton extraction from occupancy grids for mobile robot navigation", '20ème Congrès Francophone sur la Reconnaissance des Formes et l'Intelligence Artificielle (RFIA 2016), France

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SIGMAFUSION: MULTI-SENSOR FUSION EMBEDDED PERCEPTION



RESEARCH TOPIC:

Multi-Sensor Fusion, Autonomous Drive, ADAS, low power perception,

AUTHORS:

D. Puschini, J. Mottin, T. Rakotovao, C. Laugier (INRIA)

ABSTRACT:

Observing and understanding the environment is a fundamental task of many applications: autonomous navigation, robotics, travel aid to visually impaired people, etc. The variety in nature of the objects, in environmental conditions, stresses the need for the integration of heterogeneous sensor technologies. Radars, Ultrasonic sensors, Lidars, vision systems offer complementary information, which can be possibly noisy and contradictory. To overcome the resulting complexity, Occupancy Grids (OG) have been intensively used. Their major drawback lies in their large computing. SigmaFusion is a novel framework for OG computation that cuts down the implementation cost, while maintaining precision and soundness of the original OG theoretical formulation.

SCIENTIFIC COLLABORATIONS: INRIA

Context and Challenges

Occupancy Grids (OGs) have proposed to solve the challenge of integrating heterogeneous information coming out of imprecise, noisy sensors. It relies on a probabilistic Bayesian formulation that predicts the occupancy probability of a specific region of the environment based on the sensors outputs. When sensors deliver conflicting information, the final probability is mitigated in a procedure called Multi-Sensor Fusion. OGs also offer a common spatial frame to all sensors, and a common discretization to support spatial mapping and computing from sensors data. In state-of-art implementations, OGs are built on expensive parallel platforms with floating point support and/or acceleration.

Main Results

SigmaFusion is a novel arithmetical formulation of the OGs framework, mathematically equivalent, suitable for sequential implementation with integer arithmetic only.

The first main contribution [1] proposes a novel scheme for the discretization of the probability space, suitable for multiple sensor fusion. As a result, it describes how to build a countable closed set of probabilities that solves the challenge of computing Bayesian fusion using integer arithmetic, see Fig. 1.

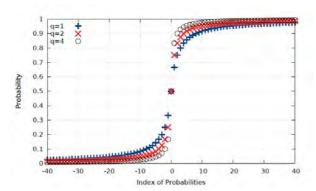


Figure 1 - Countable closed set of probabilities

The main property of such sets is that the fusion of two elements of the set also belongs to the set. From a probability-based computation of fusion using floating point, it is therefore possible to derive an integer based fusion based on the indices of the probabilities. Such indices exists since the set is countable.

The second main result [2] is an integer based procedure that allows to map sensor information in OGs with a user-defined precision. The two contributions have been jointly used in experiments for automotive applications. Automotive ECUs often offer limited computing capabilities, and SigmaFusion offers an opportunity to implement multi-sensor perception in automotive grade platforms, see Fig. 2.

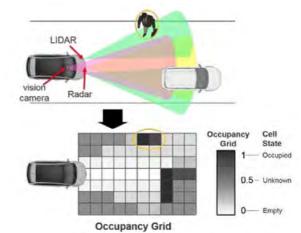


Figure 2 - Automotive implementation of SigmaFusion

Perspectives

With SigmaFusion, highly constrained application domains can now benefit from efficient implementation of multi-sensor fusion. Possible hardware implementations can also help future innovative sensor developments.

RELATED PUBLICATIONS:

[1] Tiana A. Rakotovao, Julien Mottin, Diego Puschini, Christian Laugier: Multi-sensor fusion of occupancy grids based on integer arithmetic. ICRA 2016: 1854-1859

[2] Tiana A. Rakotovao, Julien Mottin, Diego Puschini, Christian Laugier: Integration of multi-sensor occupancy grids into automotive ECUs. DAC 2016: 27:1-27:6.

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ALWAYS RESPONSIVE PLATFORM FOR INTERNET OF THINGS -WAKE UP CONTROLLER

RESEARCH TOPIC:

Internet of Things, wake up controllers, asynchronous processor, automatic sleep mode, event-driven activity

AUTHORS:

J.F. Christmann, F. Berthier, O. Sentieys (INRIA), E. Beigné

ABSTRACT:

This work tackles the development an ultra low power platform for Internet of Things applications. Like any other similar Wireless Sensor Node (WSN), such a platform is constrained by low activity in potential harsh environment. Main targets are thus intrinsic power consumption, whose major contribution comes from leakage, and functional modes management, in order to efficiently switch between processing and sleeping states. On the one hand, we demonstrate promising power consumption performances using UTBB FDSOI 28nm technology. On the other hand, an asynchronous wake up controller is proposed for efficient event-driven implementation of the platform.

SCIENTIFIC COLLABORATIONS: IRISA/INRIA (Rennes)

Context and Challenges

The Internet of Things (IoT) is supposed to encompass billions of connected devices. Wireless Sensor Nodes targeting ultra-low energy applications, such as monitoring and transferring data via RF link, have to cope with new constraints like changing energetic environment, long idle phases, automatic wake up, data backup or even ultra-low voltage operations. In this context, arising challenges concern the use of a low power yet advanced technology process and the development of an architecture which smartly handles typical IoT applications.

Main Results

First, a study of the opportunities offered by UTBB FDSOI 28nm technology process has been realized and shows promising results for IoT systems and applications [1].

High performances can be achieved using UTBB FDSOI 28nm technology process: from 460MHz at 0.4V to 2.6GHz at 1.3V. In addition to those performances, this technology process provides low leakage features but especially exhibits flexibility and performance control thanks to a wide range of back biasing polarization, as illustrated by Fig.1. A factor of magnitude 10 can be reached and allows smart applicative adaptability for ultra-low leakage while in sleeping mode.

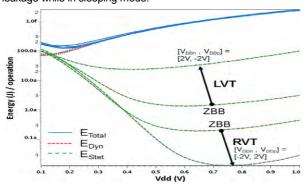


Fig 1 - MEP analysis for RVT and LVT UTBB FDSOI ring oscillator under VBB variations (ZBB = no body biasing applied)

Second, partitioning has been performed on the system architecture to group features related to wake up into an Always Responsive part, which is always powered (Fig. 2). Its job is to detect events in the system environment, such as temperature threshold crossings or incoming communication requests, and to adequately handle the consequent task, on its own or by waking up the main part of the platform, so called On Demand.

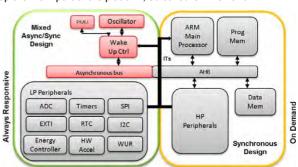


Fig 2 - Internet of Things platform partitioned architecture

In addition to a conventional main processor, staying mostly in sleep mode yet handling the heaviest tasks, the proposed IoT platform thus includes an asynchronous wake up controller [1,2]. Asynchronous QDI logic's robustness to environmental variations and automatic sleep mode are leveraged to allow a sub-10µW low core which keeps on waiting on events, even in extreme conditions.

Perspectives

This work, as a brick in the IoT framework, has huge perspectives, both in terms of IP development and of platform development. Thanks to deep work on the core implementation, we expect to reduce the power consumption under the µW threshold. In addition, essential IPs are to be developed and included in the Always Responsive part of this IoT platform. Among others, we target the integration of a wake up radio, which would be dedicated to wireless wake up and to simple message communication, and energy harvesters combined to an energy controller, whose job is to monitor the energetic environment in order to allow the system to optimally schedule the application.

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[2] Beigné, E., Vivet, P., Thonnart, Y., Christmann, J.-F. and Clermidy, F., "Asynchronous Circuit Designs for the Internet of Everything", Solid-State Circuits Magazine, pp. 39-47, 2016

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FULLY INTEGRATED LOCK-IN AMPLIFIER DEDICATED TO PHOTO-ACOUSTIC GAS SENSING



RESEARCH TOPIC:

Lock-In amplifier - Photo-acoustic gas sensor - sensor readout circuits

AUTHORS:

F. Badets, J-G. Coutard, E.Dina, A. Glière and S. Nicoletti

ABSTRACT:

This work is related to the implementation of a 12-bit Lock-In Amplifier (LIA) based readout circuit dedicated to Photo Acoustic gas sensors. This circuit is one of the very few examples of fully integrated LIA, as it embeds the low pass filter, the clock generation circuit as well as a 12-bit ADC. Its power consumption is 1.3 mW under a 3.3 V supply voltage, while achieving $10nV/\sqrt{Hz}$ input referred noise

Context and Challenges

From Principle...

Photo-acoustic gas detection relies on the excitation of a molecule of interest with a light source emitting at the wavelength of an absorption line of the molecule. The light is modulated at the acoustic resonance frequency of a chamber containing the gas mixture, creating a pressure wave that could be detected by microphones.

...to Miniaturization

Photo-acoustic technique has favorable detection characteristics when the system dimensions are scaled down. A mm size PA is under study in the frame work of the FP7 MIRIFISENS project. Once coupled with Quantum Cascade Lasers (QCL) and an optical multiplexer, it should lead to the miniaturization of multigas sensors [1].

Main Results

In order to keep full advantage of the sensor miniaturization, the full integration of the electronic readout circuit has been considered in this work.

Readout Circuit

Fig 1. Readout Architecture

As the gas concentration information lies on the amplitude of the signal wave at the microphones output, a Lock-In amplifier architecture has been chosen and is depicted in Fig.1 [2]. It consists in the multiplication of the signal with a quadrature clock at exactly the same frequency as the incoming signal, performing thus a synchronous detection. The accurate quadrature is obtained by locking a PLL to four times the signal frequency and dividing its output frequency through a divider by four.

The input referred noise has been measured to 170 nV over a 300 Hz bandwidth at 20 KHz which is in accordance with simulated results. The current consumption is 400µ A under a 3.3V supply voltage.



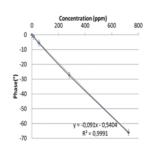


Fig. 2: a) Experimental gas test bench embedding a « mini » PA cell and the fully integrated LIA readout circuit, b) phase difference between the two microphone outputs

A full chain of detection embedding a Quantum Cascade Laser (QCL) emitting in the mid infra-red, a centimeter size PA based on a differential Helmholtz cell resonating at 2 kHz and two readout circuits has been designed as depicted in Fig 2. The readout circuits have been assessed by measuring the phase shift versus gas concentration (here CO2). The obtained characteristic function is linear as expected, and permits sub-ppm detection validating thus the full chain of detection associating the QCL, the miniaturized PA cell and the LIA based readout circuits.

Perspectives

Next steps will consist in optimizing the overall performance of the circuit through the increase of the resolution. The LNA noise should be improved, oversampled ADCs could be efficiently introduced.

RELATED PUBLICATIONS:

[1] J.G.Coutard, J. Rouxel, M. Brun, O; Lartigue, S. Nicoletti, F. Badets and A. Glière "Development of a high Performance Miniaturized Photoacoustic Gas Sensor",

Imaging and Applied Optics 2016, OSA technical Digest, paper LTh3E.6
[2] F. Badets, J.G. Coutard,, P.Ruso, E.Dina,, A.Glière, and Nicoletti, "A 1.3 mW, 12 bit Lock-In Amplifier Based Readout Circuit Dedicated to Photo-Acoustic Gas Sensing," 2016 IEEE Sensors, Orloando, FL, 2016, pp 1-3.

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INTEGRATED CIRCUIT DESIGN TOWARDS GRAVIMETRIC SENSING APPLICATIONS BASED ON LARGE NANO-MECHANICAL RESONATOR ARRAYS

RESEARCH TOPIC:

Nano Electro Mechanical Systems (NEMS), Resonator, Oscillator Gravimetric Sensing, Mass Spectrometry, Resonant Sensor

AUTHORS:

G. Gourlat, G.Billiot, P. Villard, S. Hentz, G. Sicard

ABSTRACT:

The extreme sensitivity of nano electro mechanical system (NEMS) to atomic scale physical variations has led to the breakthrough development of NEMS-based mass spectrometry systems capable of measuring a single molecule. Parallel sensing using thousands of devices will help to circumvent the small effective sensing area while opening new perspectives for applications which require spatial mapping.

Context and Challenges

While development of NEMS CMOS co-integration technology is of paramount importance to achieve high density sensor arrays (>1000 devices) [1], the readout circuitry capable of tracking NEMS resonator frequency shifts is still the limiting factor for the very large scale integration of individually addressed sensors. Moreover, in order to resolve the mass and position of an adsorbed analyte, single particle mass sensing applications require to track simultaneously and in real time at least two modes of the resonators. This requirement adds complexity to the design of the overall system.

Main Results

To respond to the size, power consumption and resolution constraints linked to NEMS array measurement, we propose a compact heterodyne self-oscillator circuit topology which performs simultaneous dual-mode frequency tracking compatible with a NEMS "pixel-based" readout scheme [2].

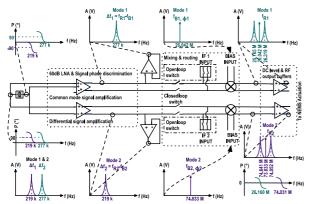


Fig 1. Schematic of the dual-mode heterodyne oscillator tracking simultaneously the first two modes of the resonator

The dual-mode heterodyne self oscillating loop SOL behavior is illustrated in Fig. 1. The mechanical resonator's motion occurring at frequencies (fR1, fR2) is down-mixed by the gauges biasing

signals at (fB1, fB2). The resulting NEMS output signals located at the intermediate frequency range (Δ f1=fR1-fB1, Δ f2=fR2-fB2) are discriminated and amplified by a low noise amplifier (LNA). Finally, the active up-mixer multiplies the intermediate frequency signal with a phase-shifted signal at biasing frequencies (fB1, Φ 1, fB2, Φ 2), thus shifting the signal back to the resonant motion frequency range with the gain and phase Barkhausen conditions fulfilled.

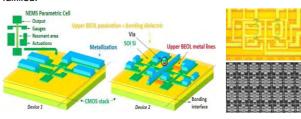


Fig 2. Schematic principle of NEMS resonators connected to CMOS (Back End Offline) BEOL and SEM and optical observations of NEMS arrays above CMOS BEOL.

On the integration side, the 3D sequential co-integration of silicon NEMS above industrial CMOS wafers with the so-called CEA/LETI "CoolCubeTM" promises good integration density. Figure 2 shows NEMS patterned in monocrystalline silicon above industrial CMOS Back-End-of-Line (BEOL) wafers. We successfully demonstrated similar electrical performance of the NEMS devices, whether or not they are routed through CMOS BEOL. We report frequency stability (characterized by the Allan deviation tool) around 10-7 at 100ms integration time.

Finally, the proposed integrated circuit [3] targets NEMS array gravimetric sensing applications that require compact "pixel-based" readout electronics. We report a compact (26 $000\mu m^2$) heterodyne 30-80MHz self-oscillator analog front-end IC which performs fast (1ms) simultaneous dual-mode frequency tracking and achieves 300 zeptogram mass resolution.

Perspectives

Next steps will consist in designing large NEMS array cointegrated with the proposed heterodyne oscillator readout scheme.

RELATED PUBLICATIONS:

[1] Gourlat, M. Sansa, P. Villard, G. Sicard, G. Jourdan, and S.Hentz. "Simultaneous mode tracking for sensing applications with dual- mode heterodyne NEMS oscillator".: IEEE SENSORS 2016 Conference Proceedings. IEEE SENSORS 2016. Orlando, Florida, 29 oct. 2016

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[3] G. Gourlat, M. Sansa, P. Villard, G. Sicard, G. Jourdan, I. Ouerghi, G.Billiot and S. Hentz. "A 30 – 80 MHz simultaneous dual-mode heterodyne oscillator targeting NEMS array gravimetric sensing applications with a 300 zg mass resolution".: 2017 IEEE International Solid-State Circuits Conference (ISSCC). 2017.

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EMBEDDED OMTDR SENSOR FOR SMALL SOFT FAULT LOCATION ON AGING AIRCRAFT WIRING SYSTEMS



RESEARCH TOPIC:

Cable diagnosis, reflectometry, soft defect, smart connector, OMTDR, post-processing, data fusion

AUTHORS:

W. Ben Hassen, M. Gallego Roman, B. Charnier, N. Ravot, A. Dupret, A. Zanchetta, F. Morell

ABSTRACT:

This work introduces the first embedded Smart Connector (SmartCo) which could locate very small soft defects resulting from partial degradation of cables. SmartCo injects a generated OMTDR signal at an extremity of the cable and then listens to the echoes created at each discontinuity of the cable characteristic impedance. Since soft defects result in faint reflected energy, they are hard to distinguish from the noise. Hence, the SmartCo uses an approach based on data fusion to eliminate false alarms and determine the small soft fault position

Context and Challenges

In aircrafts, soft defects represent 45% of wire faults such as chafing, corrosion, and insulation according to NASA. These defects may not lead to catastrophic incident since they do not interrupt energy or information propagation, but can generate hot spots and hard faults (open circuit and short circuit). Hence, the detection and location of small soft defects permit to plan predictive maintenance and avoid system dysfunction (about 150 000 dollars per hour for aircraft on ground [1]). In this context, reflectometry remains the most interesting method for cable diagnosis [2]. It injects a signal at an extremity of the cable and listens at the same port to the echoes created at each discontinuity of the cable characteristic impedance. An embedded wire Health Monitoring System (HMS) is crucial to ensure continuous cable diagnosis. Thus, the miniaturization of Orthogonal Multi-tone Time Domain Reflectometry (OMTDR) systems is necessary to enable their implementations into connectors [3]. Introducing intelligence into the commercial connector, named SmartCo, permits to maximize the diagnosis coverage and increase accuracy. Indeed, the OMTDR technology is chosen for SmartCo thanks to sensor data fusion enabling using the same test signal.

Main Results

The proposed approach includes several steps as illustrated in Fig.1. After reflectograms construction, a difference between healthy and faulty cable reflectograms is performed to eliminate inhomgeneities related to cable manufacturing, installation, etc. After post-treatment method, a windowing is performed to eliminate the peaks related to impedance mismatch. A normalization step is performed with respect to optimum values of remaining samples. Step 7 converts each reflectogram obtained at step 5 into a signal where the amplitude of each sample represents the percentage of satisfied thresholds in step 6. In step 8, the cable length is divided into sections based on predetermined spatial intervals. In step 9, the signal is converted into a measure of the conditional probability of the defect presence in each section according to method m, noted P(D/m). Data fusion of two post-processing methods m_1 and m_2 is calculated as shown below:

 $P(D/m_1,m_2) = P_1P_2/[P_1P_2+(1-P_1)(1-P_2)],$

with $P_1 = P(D/m_1)$ and $P_2 = P(D/m_2)$

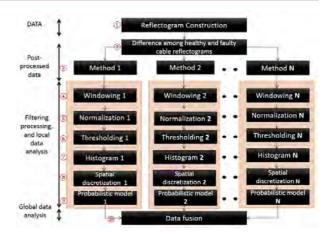


Figure 1. Innovative approach for soft fault location.

In order to evaluate the proposed approach, a shielded twisted pair TWINLINK 50 FA with length 30 m is considered where a -8 mm long, 3 mm wide- shield damage is present at 10.9 m from the injection point. As illustrated in Fig. 2, the proposed algorithm makes possible the detection and accurate location of a soft fault at 10.98 m.

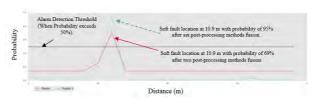


Figure 2. Soft fault detection and location at 10.98 m.

Perspectives

As future works, OMTDR-based sensor fusion will be implemented to maximize the diagnosis coverage

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[1] F. Auzanneau, "Wire troubleshooting and diagnosis: Review and perspectives," Progress in Electromagnetics Research B 49, pp. 253–279, 2013.

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COMPRESSIVE HIGH DYNAMIC RANGE CMOS IMAGE SENSOR WITH DEDICATED RECONSTRUCTION ALGORITHM

RESEARCH TOPIC:

Compressed sensing, High Dynamic Range, Image sensor

AUTHORS:

W. Guicquero, A. Dupret and P. Vandergheynst (EPFL)

ABSTRACT:

Standard imagers feature dynamic range about 60dB while natural scenes may be over 120dB. Sensors that address such High Dynamic Range need specifically designed pixels or perform a multi-capture that unfortunately requires larger memories and longer acquisition time. On the other hand, Compressive Sensing (CS) implementations suffer from these same issues impacting both the pixel and the readout circuitry. This work [1] presents a novel imager design without classical pixel changes enabling HDR CS thanks to a dedicated current readout mode and specific time diagrams of the control signals.

SCIENTIFIC COLLABORATIONS: Pierre Vandergheynst, École Polytechnique Fédérale de Lausanne (EPFL)

Context and Challenges

During the last decade, several architectures of CMOS imagers performing CS have emerged. Regarding this kind of sensor, the CS measurement operator is not implemented after the ADC stage because it would not fully take advantage of the CS paradigm. Analog implementations are generally preferred for both decreasing the amount of the on-chip storage area and reducing the overall power consumption. But major limitations still reside on the complexity inside the pixel and the parallelization of the measurements, namely resulting in larger technological dispersions between the pixels. A recent trend is to minimize the impact on pixel design, performing the CS operation during the readout stage, for instance at the end of column circuits [2].

Main Results

The proposed CS acquisition method is based on acquiring multiple compressed images corresponding to different integration times. It is a direct extension of CS for HDR imaging. The generation of pseudo-random word for CS projection vectors is performed thanks to a dedicated cellular automaton with pseudo-random behavior and reduced expectancy output. This circuit has the advantage of exhibiting a very small footprint, a low power consumption and reducing the need for large memory stored inside the image sensor.

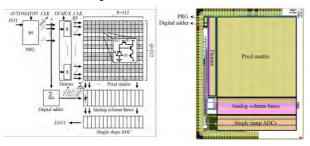


Fig 1. Functional view of the image sensor architecture

An architecture (see Fig. 1) and its dedicated reconstruction algorithm are jointly optimized taking into account the pixel nonlinear behavior in current-mode readout. In addition, this imager can easily be turned into a color image sensor by using a

regular Color Filter Array (CFA). The pixel and the overall architecture can advantageously keep a "conventional" design and the specific readout mode can be switched off. Interestingly, the HDR CS multi-capture also relaxes requirements on the pixel linearity. Indeed, a new class of CS reconstruction algorithms is emerging to make it more robust against nonlinearity, noise and mismatches between the acquisition model and the actual way the information is acquired [3].

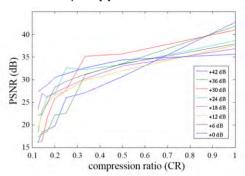


Fig 2. PSNR of reconstructed images depending on the compression ratio and Dynamic Range extension.

Therefore, this proposed approach provides a tradeoff between Dynamic Range, image quality and CS Compression Ratio (see Fig. 2). Typically, a 40dB enhancement of the dynamic range can be reached without increasing the amount of converted data compared to a single integration time uncompressed acquisition. It shows that for a specific adaptive tone-mapping operator, it does not degrade the overall quality of a tone mapped image even if the amount of acquired information is considerably reduced compared to a regular multi-capture acquisition.

Perspectives

This work shows how Compressive Sensing can relax on-chip constraints in the scope of multi-capture based HDR imaging. Our ongoing work aims at developing a new class of image sensor well suited for HDR CS with very few modifications of a conventional design. The acquisition scheme, the set/reset timetable and the readout circuitry slightly differs from common image sensors. which is a trend in recent works on CS

RELATED PUBLICATIONS:

[1] W. Guicquero, A. Dupret and P. Vandergheynst, "An Algorithm Architecture Co-Design for CMOS Compressive High Dynamic Range Imaging," in IEEE

Transactions on Computational Imaging, vol. 2, no. 3, pp. 190-203, Sept. 2016.
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TOWARDS ULTRA LOW NOISE IMAGE SENSOR

RESEARCH TOPIC:

CMOS, CIS, image sensor, low noise

AUTHORS:

Assim Boukhayma, Arnaud Peizerat and Christian Enz (EPFL)

ABSTRACT:

An analytical noise calculation has been carried out to derive the impact of process and design parameters on 1/ f and thermal noise for a low-noise CMOS image sensor (CIS) readout chain, [1]. This approach was then confirmed with a sub-0.5 e⁻ms temporal read noise VGA (640H×480V) CMOS image sensor that has been integrated in a standard 0.18 µm 4PM CIS CMOS process. The low noise performance is achieved exclusively through circuit optimization without any process refinements. The presented imager relies on a 4T pixel of 6.5 µm pitch with a properly sized and biased thin oxide PMOS source follower, [2].

SCIENTIFIC COLLABORATIONS: Christian Enz, Ecole Polytechnique Fédérale de Lausanne (EPFL)

Context and Challenges

During the last few years, many works focused on the reduction of the temporal readout noise (TRN) in CMOS image sensors based on pinned photodiodes in order to enhance their performance under low light conditions. To this purpose, the noise of the whole readout chain has to be minimized, starting with the thermal noise using conventional circuit techniques, e.g. bandwidth control, in-pixel or column-level amplification and correlated multiple sampling (CMS). After thermal noise reduction, the 1/f noise originating from the pixels becomes the dominant noise source. At the circuit level, the correlated double sampling (CDS) and CMS reduce dramatically that 1/f noise, but not enough to reach sub-electron noise performance. Thus, pixellevel optimization is required in order to further reduce the 1/ f noise. The purpose of this work is to exploit the only few degrees of freedom left to the designer, in a standard process, to further reduce the input-referred TRN to sub-0.5-electron level...

Main Results

The chip, Fig. 1, has been fabricated in a CIS standard 1P4M process (digital: 1.8V transistors, analog: 3.3V transistors, pinned photodiode, color filters and microlenses (not used here)).

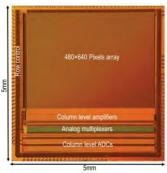


Fig. 1 Chip micrograph and imager main design blocks

In order to assess the pixel conversion gain, the photon transfer curve (PTC) measurement technique is used. A conversion gain of 160µV/e- is obtained. It is measured by estimating the slope

factor in the linear part of the PTC and dividing it by the measured gain of the readout chain.

In order to measure the input-referred noise the output voltage noise is first measured. Then it is referred to the input using the readout chain conversion gain. This operation was applied to 5000 pixels after performing 100 readouts with a CDS of 5 µs and a line (pixel) readout time of 25 μs . The in-pixel SF current bias is set to 1.5 µA and the TX is off. The column-level amplifier gain is set to 64, limiting the bandwidth to about 300 kHz in order to reduce the thermal noise and the noise originating from the next stages. Fig. 2 shows the resulting histogram of the input referred TRN. The maximum of the histogram corresponds to 0.48 erms. The inset of Fig. 2 shows the histogram in a log scale highlighting a minority of pixels featuring an RTS noise of a few e- rms.

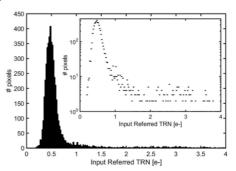


Fig. 2 Input-referred temporal read noise histogram of the image sensor - vertical axis in linear and log scale (inset).

Perspectives

This work provides a full characterization of the VGA imager showing that neither the dynamic range, the imager lag nor the PRNU are compromised with the proposed noise reduction technique. The characterization also shows that the QE of the PPD is not affected by the neighboring PMOS n-wells. Note that the proposed approach can be combined with any known additional noise reduction techniques at system (e.g. CMS), device (e.g. buried channel) and process level (e.g. parasitic capacitance reduction) to further reduce the TRN, [3].

RELATED PUBLICATIONS:

[1] A. Boukhayma, A. Peizerat, C. Enz, "Temporal Readout Noise Analysis and Reduction Techniques for Low Light CMOS Image Sensors", IEEE Transaction on

Electron Devices, Vol. 63, No. 1, January 2016
[2] A. Boukhayma, A. Peizerat, C. Enz, "A Sub-0.5 Electron Read Noise VGA Image Sensor in a Standard CMOS Process", IEEE Journal of Solid-State Circuits, Volume: 51, Issue: 9, Pages: 2180 - 2191, 2016

[3] A.Boukhayma, A. Peizerat, C. Enz, "Noise Reduction Techniques and Scaling Effects towards Photon Counting CMOS Image Sensors". Sensors 2016,

ADC SAMPLING REDUCTION BY AN EFFICIENT IMPLEMENTATION OF QUEUE - APPLICATION TO X-RAY SPECTROMETRY IMAGERS

RESEARCH TOPIC:

ADC, CMOS, queue, random flux, X-Ray, imager, spectrometry

AUTHORS:

J.-P. Rostaing, G. Sicard, A. Dupret, A. Peizerat, P. Villard

ABSTRACT:

In a high-speed digital X-ray imager, each pixel in the matrix needs an analogue-to-digital converter (ADC) in order to assess the energy of the randomly incoming photons. The analogue-to-digital (AD) conversion rate is thus highly dependent on the photon flux parameters. In classic designs, this rate is often set to ten times the maximum photon flux mean, which requires highspeed ADCs. The use of a queue to derandomize the photon flux prior to the AD conversion allows the ADC sampling frequency to be decreased to the maximum photon flux mean instead of ten times that value. An electronic circuit has been designed and the simulations results show a behavior close to the theoretical model: at the cost of an additional queue block, reduced speed can be achieved, leading to a lower consumption and an easier integration.

Context and Challenges

The sampling frequency of analogue-to-digital converters (ADCs) usually derives from a strict respect of Shannon's sampling theorem. When the signal to be converted is composed of sporadic, short lasting events, e.g. pulses, the sampling frequency is chosen so as to comply with the worst case, i.e. the shortest delay between two events. Such a situation can be found in X-ray spectroscopy. In our case, the purpose of the queue is to store the successive randomly occurring events and to release those events at regular time intervals. In other words, the queue turns sporadic events into regularly spaced events that can be processed with fewer resources.

Main Results

The straightforward implementation of a queue would be an analogue shift register. Yet, unless charge transfer processes (e.g. charge coupled device vision sensor) are available, the usual implementation in CMOS technology requires buffers, capacitors and switches. As a result, the signal at the end of the queue is altered by the reset noise and by charge injections that are added at each step of its progress through the queue. Moreover, the buffers require additional silicon area, power and they add noise. Hence, we developed a K cell parallel queue, shown in Fig 1.

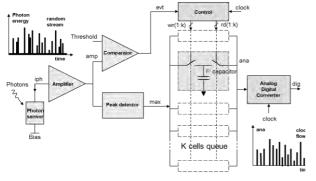


Fig 1. Block diagram of our X-ray pixel using a queue

Several electrical simulations over Ts = 1 ms are performed with the ELDO simulator on the CMOS circuit. Those simulations encompass a large number of events in order to get sufficient statistical accuracy. The writing time in the queue is Tw = 2 ns. The reading period in the queue, equal to the ADC sampling period, is Tck = $1/\mu$ = 80 ns (i.e. μ = 12.5 M samples/s). All written events are read. Proximity is observed in Fig. 2 between the theoretical green curve 'eight-seat queue' and the simulated points, yet tainted with a statistical error. We note that the measures deviate from the curve especially at low traffics due to the electronics implementation imperfection. Even when the expected K = 8 curve is not reached, a significant gain is obtained: a factor of 7 for 1% losses instead of a factor of 8.

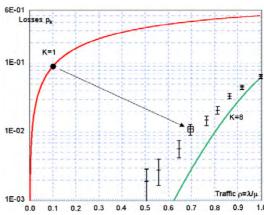


Fig. 2 Losses versus traffic for simulated points and theoretical curves

Perspectives

The implementation of the queue we have described and simulated is compact enough (i.e. about 50 × 150 μ m2 or a quarter of the ADC area on a 130 nm CMOS process) to be easily integrated within an X-ray imager pixel. The functional and electrical simulations confirm the predicted performances.

RELATED PUBLICATIONS:

[1] J-P. Rostaing, G. Sicard, A. Dupret, A. Peizerat and P. Villard, "ADC sampling reduction by an efficient implementation of queue application to X-ray spectrometry imagers," in Electronics Letters, vol. 52, no. 6, pp. 428-430, 2016.

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ISOLATED GATE DRIVER OPTIMIZED FOR GAN-BASED HIGH VOLTAGE POWER CONVERTERS



RESEARCH TOPIC:

Power electronics, Gate driver, Wide bandgap devices, Synchronous converter, Coreless transformer, Signal isolation

AUTHORS:

R. Grezaud, D. Bergogne, Y. Wanderoild, F. Ayel, N. Rouger (Laplace), J.-C. Crebier (G2elab)

ABSTRACT:

An ultimate isolated gate driver optimized for GaN-based high voltage power converters is presented. Signal and power isolation, negative voltage generation, adaptive output impedance and dynamic dead-time control are required functions for a gate driver to be compatible with Wide Band Gap Transistors and high temperature. Specific architectures have been studied and fabricated in CMOS and SOI technologies to implement in a single chip these four key features.

SCIENTIFIC COLLABORATIONS: G2elab (Grenoble), Laplace (Toulouse)

Context and Challenges

In recent years SiC and now GaN power devices have come out on the market and engineers are starting to implement them in promising high frequency, high efficiency power converters especially for high bus voltages requiring breakdown voltages in the 600V to 1200V range. Manufacturers provide Gate Drivers that can be used with some Wide Band Gap Power Transistors. However, these integrated circuits are either single gate drivers without insulation or limited voltage bridge drivers, up to 100V. A specific GaN-FET gate driver must address high peak currents. high speed with high voltage isolation and also take care of Electro-Magnetic-Interferences due to high speed switching. GaN devices also require negative biasing and dynamic short deadtime control in synchronous power converters.

Main Results

Three key functions of a gate driver compatible with Wide Band Gap Transistors and high temperature applications are presented in [1]. A specific negative voltage charge pump has been developed to ensure safe operation during normal conditions by

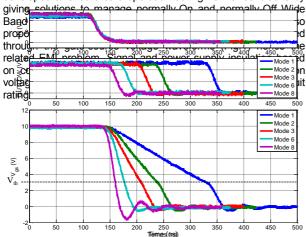


Fig.1 Experimental Vgs turn-off waveforms of the adaptive impedance gate driver to reduce EMI issues

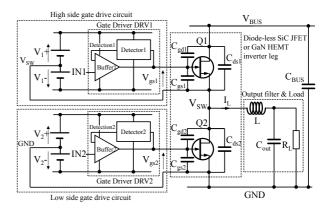


Fig.2 High-efficiency diode-less GaN-based synchronous buck converter driven by the proposed auto-adaptive dead-time gate driver

A specific dead-time management is introduced in [3] to ensure proper operation of a high-voltage synchronous power converter (Fig.2). A controller integrated in each single isolated gate driver secures synchronous switching by detecting the opposite switch turn-off before turn-on. With such a self-switching technique very short but safe non-overlap times can be set. A gate driver has been implemented in a 0.35µm 20V CMOS process. The monolithically integrated controller consumes only 140µA and 0.22mm² of silicon area. The proposed local dead-time management has been validated in two synchronous buck converters without external free-wheeling diodes: a 500W 250V to 55V converter based on SiC JFETs and a 30W 45V to 10V converter based on GaN FETs. In either case, the proposed controller allows a higher efficiency from 10% of the rated load with resulting dead-times as short as 15ns.

Perspectives

Future work targets a single gate driver chip fabricated in a standard HT 10V SOI technology with each key function integrated. Finally even higher performance could be reached with some critical parts monolithically integrated in GaN.

RELATED PUBLICATIONS:

- [1] R. Grezaud, F. Ayel, A. Chapel and D. Bergogne, "Wide Band Gap Power Transistors Gate Driver Cutting Edge Bloc Functions," CIPS 2016; 9th International
- Conference on Integrated Power Electronics Systems, Nuremberg, Germany, 2016, pp. 1-6.
 [2] R. Grezaud, F. Ayel, N. Rouger and J. C. Crebier, "An adaptive output impedance gate drive for safer and more efficient control of Wide Bandgap Devices," The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications, Columbus, OH, 2013, pp. 68-71.
- [3] R. Grezaud, F. Ayel, N. Rouger and J. C. Crebier, "A Gate Driver With Integrated Deadtime Controller," in IEEE Transactions on Power Electronics, vol. 31, no. 12, pp. 8409-8421, Dec. 2016



ENERGY HARVESTING FROM A MICROBIAL FUEL CELL IN AQUATIC ENVIRONMENT FOR SUPPLYING SEAFLOOR SENSORS

RESEARCH TOPIC:

Energy harvesting, Microbial Fuel Cell (MFC), Sensor nodes, Low-power management unit, Flyback converter

AUTHORS:

A. Capitaine, T. Chailloux, O. Ondel (Ampère), B. Allard (Ampère) and G. Pillonnet

ABSTRACT:

The sedimentary microbial fuel cell (SMFC) is a promising alternative to conventional batteries for powering sensors on the seafloors in the long-term. Regarding their performances (around $100~\mu W$ at 0.3~V for cm²-scale electrodes), a power management unit is needed to maximize the harvested energy and boost the voltage to a minimum value required by the conventional electronic used in environmental sensor nodes. Extracting an equivalent model from lab-scale SMFCs, a flyback converter in discontinuous conduction mode is optimized at $90~\mu W$ input power (two decades lower than literature). With an efficiency of 72%, the global harvesting unit allows a sensor measuring and transmitting wirelessly one temperature and acceleration data every 4~s.

SCIENTIFIC COLLABORATIONS: Ampère (INSA Lyon), LGC (Toulouse), CEA/DSV (Cadarache))

Context and Challenges

Microbial fuel cell (MFC) is a promising energy harvester for supplying sensors in seafloors where solar, thermal and vibration sources are inadequate. It exploits the waste materials around the sensor: the catalysis properties of bacteria into a couple of redox reactions convert chemical energy from a large range of carbonate substrates such as seafloor sediment or compost into electrical energy (Fig 1). This energy source production is relatively robust and low-cost but the generated power is around $100\mu W$ for cm-scale electrodes and its DC voltage is not sufficient e.g. up to 0.7V to power continuously low-power sensor nodes. A harvesting interface is required i.e. a DC-DC converter to extract the maximum power from the SMFC and boost its voltage.

Main Results

Lab-scale SMFCs were realized with 20cm² of cheap material electrodes implanted in a 300L aquarium and with experimental conditions close to natural ones (Fig 1) [1-3].

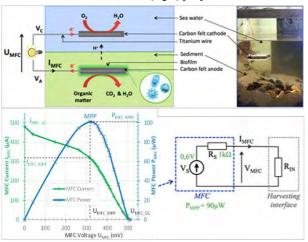


Fig 1. Schematic of a SMFC and the corresponding labscale SMFC in a 300L aquarium. Typical electrical characteristics and equivalent electrical model.

As the SMFC is intended to be used for long-term energy generation, its static performances are evaluated (Fig 1) [1-3]. The maximum power point (MPP) is around 100 μW at 0.3 V. When operating close to MPP the SMFC can be modeled by a Thevenin equivalent model (Fig 1). The extracted power is maximized when the harvesting interface impedance R_{IN} is equal to the SMFC impedance $R_{\text{S}}.$

In [1] we associated the lab-scale SMFC with a commercially-available circuit, designed for other scavenging sources. This PMU requires an external source to set the input voltage to a reference. This configuration was able to supply a sensor node composed of a temperature sensor, an acceleration sensor, a 2.4 GHz Bluetooth Low Energy Chip and an antenna (designed in LETI/DSYS).

In [2,3], we designed a dedicated harvesting interface to maximize the extraction and conversion efficiencies. The flyback in DCM is chosen because its input impedance $R_{\rm IN}$ is independent from its output voltage ie. the MPP tracking and output voltage regulation can be respected simultaneously. Its efficiency is maximized by analyzing the power loss contributions. Indeed, thanks to a proposed flyback model validated experimentally, we underline the predominant impact of the magnetic hysteresis losses in the coupled inductances. By choosing a good tradeoff between the switching frequency and the coupled inductances, a prototype was able to transfer 71% of the 90 μ W maximum power available in the SMFC to the previous sensor with an average output voltage of 2 V (Fig 2).

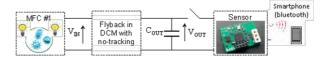


Fig 2. Temperature and acceleration sensor autonomously powered by a SMFC using a flyback in DCM.

Perspectives

Dynamic models of the SMFCs are currently under study. The start-up phase will also be studied in the future to ensure a totally autonomous work of the system *in vivo*.

RELATED PUBLICATIONS:

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[3] A. Capitaine, G. Pillonnet, T. Chailloux, F. Khaled, O. Ondel and B. Allard, Modélisation électrique d'une pile microbienne sédimentaire et extraction de son énergie par un flyback en mode discontinue, Symposium de Génie Electrique (SGE 2016), juin 2016, Grenoble, France.

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ENERGY HARVESTING CIRCUITS USING PIEZOELECTRICITY



RESEARCH TOPIC:

Energy harvesting, Start-up circuit, Multiphysics modeling, Piezoelectricity, Frequency tuning, Low-power management unit.

AUTHORS:

A. Morel, T. Martinez (SATIE), G. Pillonnet, R. Grézaud, P. Gasnier, A. Badel (SYMME), F. Costa (SATIE)

ABSTRACT:

One of the main challenges in energy harvesting from ambient vibrations is to find efficient ways to harvest the energy, not only at the mechanical system resonance, but on a wider frequency band. We propose new ways to tune this resonant frequency based on the electromechanical coupling, and two different interfaces that have been used to harvest about $600\mu W$ over a 20 Hz frequency bandwidth (5 to 6 times more than without any tuning). Finally we present another use of piezoelectric ceramics, not as a harvester but as a transformer in start-up operation of converters for energy harvesting.

SCIENTIFIC COLLABORATIONS: SATIE (Paris-Saclay), SYMME (Annecy)

Context and Challenges

The last decade has seen a growing interest in new sustainable energy sources that could replace batteries and help developing self-powered sensors systems. Mechanical energy harvesting is a good alternative to solar or thermal generators, since energetic vibrations are easier to find in various environments. Piezoelectric elements are of particular interest because of their high energy densities and integration potential (~1mW.cm⁻³.G⁻²).

The main issue with piezoelectric harvesting, is that the resonance frequency of the structure must be matched with the vibrations frequency in order to maximize the harvested energy. One of the principal challenge in this field is to find ways to adapt the resonance frequency of such systems without increasing its size or consuming too much power.

Main Results

Instead of tuning the mechanical part of the harvester, implying bulky solutions not well fit for small devices, we propose to tune the electrical part. An electric field applied on a piezoelectric material results in a counteracting force applied on the mechanical structure. This force can modify the resonant frequency of the system. Hence, the electrical interface can be used to tune dynamically the system's resonant frequency to the vibrations frequency in order to maximize the harvested energy.

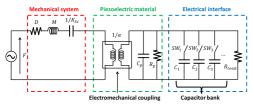


Fig. 1. Piezoelectric model with its electrical interface

We first proposed a solution in [1] based on a capacitive adaptation, as shown in Fig.1. Changing the capacitance of the load allows to tune the phase of the force applied on the mechanical system, leading to a change in its resonant frequency. The main issue of this solution is that it requires a large off-chip capacitive bank that needs to be tuned step by step.

In order to overcome these limitations, we proposed another solution based on a non-linear interface, as explained extensively in [2]. Here, we include some short-circuit times, forcing the electric field at zero, and hence changing the characteristics (magnitude, phase) of the force applied on the mechanical system. This strategy allows the tuning of the frequency on a relatively large bandwidth. The experimental results show that it is possible to harvest about $600~\mu W$ over a 20 Hz frequency bandwidth, which is 5 to 6 times larger than without any tuning, as shown on Fig.2.

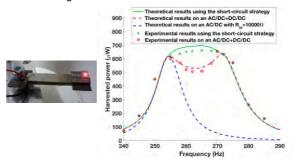


Fig. 2. (a) Highly coupled piezoelectric harvester and (b) Comparison between the theoretical and experimental results of the proposed strategy

Piezoelectric materials may also be used to create transformers that are notably useful in conversion circuits for energy harvesting systems. Their high voltage gain make them particularly suitable for start-up circuits that are used to generate a voltage high enough to supply the active harvesting interfaces circuits. We proposed a new kind of start-up circuit based on a self-resonant oscillator architecture with a piezoelectric transformer that is capable to step-up a voltage with an input voltage as low as 12 mV as explained in [3]. This type of transformer, in comparison with its magnetic equivalent, is expected to have better performances and to present fewer losses when integrated.

Perspectives

New solutions that could improve frequency tuning possibilities based on non-linear electrical interfaces, energy reinjection and pre-biasing are currently studied.

RELATED PUBLICATIONS:

- [1] A. Morel, R. Grézaud, G. Pillonnet, A. Badel, « Piezoelectric generator frequency tuning and output power optimization through the use of an electronic interface », 11th Energy Harvesting Workshop, 2016.
- [2] A. Morel, R. Grézaud, G. Pillonnet, P. Gasnier, G. Despesse, A. Badel, « Active AC/DC control for wideband piezoelectric energy harvesting », PowerMEMS 2016, Journal of Physics: Conference Series, 2016.
- [3] T. Martinez, G. Pillonnet, F. Costa, « A 12 mV start-up converter using piezoelectric transformer for energy harvesting applications », PowerMEMS 2016, Journal of Physics: Conference Series, 2016.

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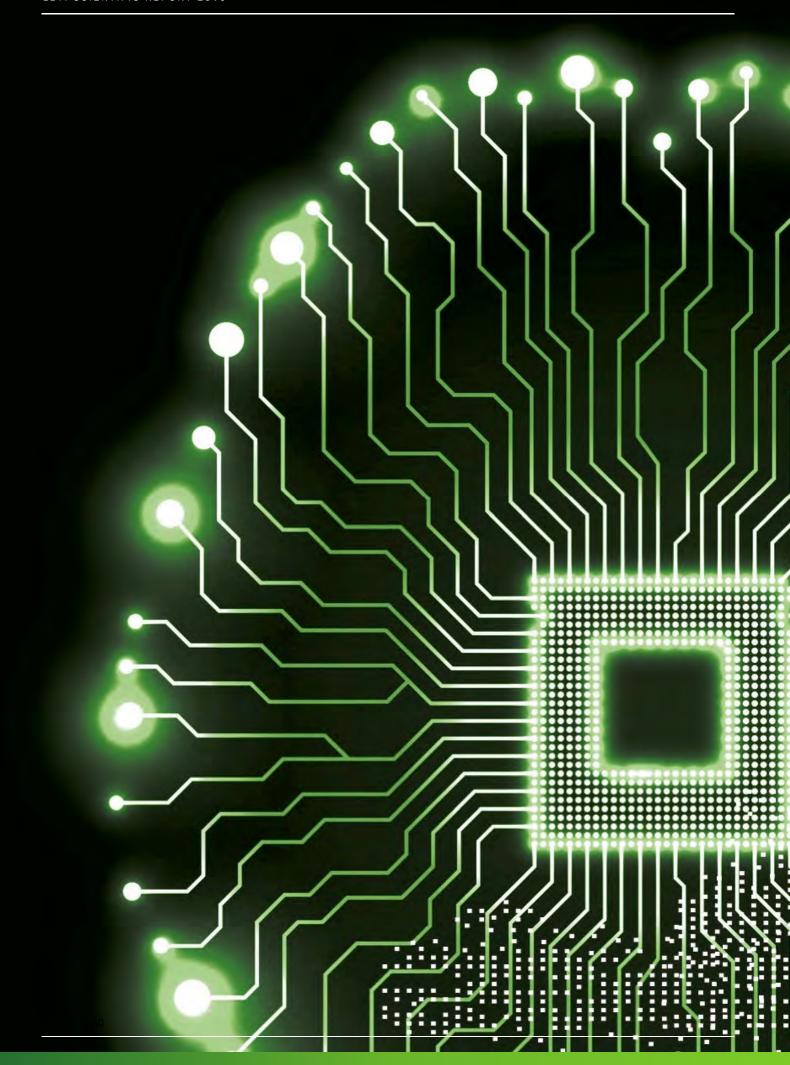
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5.

RELIABLE SYSTEMS

- Aging
- HW & SW for Security & Privacy
- Reliable Coordination Platform

ANALYSIS OF THE FACTORS INVOLVED IN THE DEGRADATION OF DIGITAL CIRCUITS FOR EARLY ESTIMATION OF AGING



Aging of integrated circuits, NBTI

AUTHORS:

C. Sandionigi, O. Heron

ABSTRACT:

One of the research activities currently ongoing at CEA-LIST has the ambitious goal of estimating the impact of aging on digital circuits without the need of degradation-aware technological libraries or aging models. A programmable hardware module, object of CEA-LIST patent and currently under development, allows reaching the goal by observing the impact of aging directly on the paths of the circuit on a selected technology. The work presented in [1] and described here constitutes a preliminary study for the design of the module. The factors involved in the degradation of digital circuits have been analyzed in order to define the methodology behind the module.

Context and Challenges

Current technologies are more and more subject to aging, which introduces delay along the paths of the circuits over time and may induce their failure. The estimation of aging at design time becomes mandatory to guarantee performance and lifetime of the circuits. The approach commonly adopted for the estimation is based on timing analysis. It requires the adoption of degradation-aware technological libraries or accurate aging models including degradation-aware technological parameters. The availability of degradation-aware technological libraries or parameters is actually an issue since the information are confidential or they have not been obtained for the required aging conditions.

The challenge taken up at CEA-LIST consists in estimating aging at design time without degradation-aware technological libraries or parameters. A Programmable Hardware Module (PHM) which allows reaching this goal is currently under development. Fig. 1 shows a comparative view of the proposed approach and the classical ones. A preliminary study, described in the following, has been conducted to identify the main factors involved in aging and the minimal structure for the configuration of the PHM. It is at the base of the methodology implemented by the module.

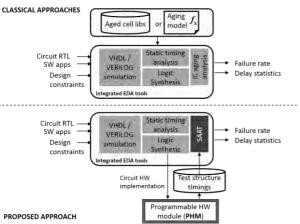


Fig. 1 Classical approaches vs. proposed approach for the estimation of aging at design time

Main Results

The study considered the impact of Negative Bias Temperature Instability (NBTI) on the paths of digital circuits. It analyzed different logic gates and their interconnections with other gates or registers and varied the key parameters involved in aging (operating time, supply voltage, temperature and activity) to estimate their impact. To identify the minimum granularity at which aging must be analyzed, each type of gate has been studied alone (located between two registers) and connected to other gates.

The following conclusions have been drawn:

- most of the degradation of the gates occurs at the beginning of the lifetime, as shown in Fig. 2;
- the increase of the supply voltage attenuates the delay;
- the delay increases as the activity increases on single gates;
- the gate's degradation is impacted by its immediate neighbors.

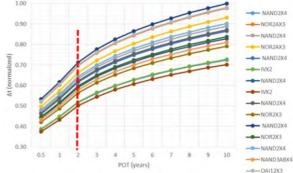


Fig. 2 Impact of power-on time on delay for various logic gates

Perspectives

The PHM, defined on the basis of the study described here and currently under development, is a collection of standard cells organized in test structures. The study of the minimum granularity allowed the definition of the structures and the analysis of the aging-related factors helped in the specification of the protocol to apply the aging conditions.

RELATED PUBLICATIONS:

[1] B. Ouattara, O. Heron, C. Sandionigi, "Fine-grain analysis of the parameters involved in aging of digital circuits", IEEE International On-Line Testing Symposium, 2016, pp. 51-53

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TRACKING BTI AND HCI EFFECTS AT CIRCUIT-LEVEL IN ADAPTIVE SYSTEMS



RESEARCH TOPIC:

Reliability, aging, BTI, HCI

AUTHORS:

M. Altieri, S. Lesecq, E. Beigné, O. Heron, D. Puschini

ABSTRACT:

Miniaturization of the transistor size provides gains in performance and power for today processors. However, aging has become a major issue in CMOS circuits due to the reduction of the thickness of the gate dielectric. The aging increase of the threshold voltage of the transistor reduces its switching speed. In this work, we propose a simple method to measure aging degradation of an Adaptive Frequency Scaling system by tracking both the maximal clock frequency for a fault-free operation and temperature evolutions over time. The technique uses sensors present in any adaptive architecture and does not requires additional structures.

Context and Challenges

Two aging phenomena, namely Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI), consist in carriers that get inside the dielectric, increasing the threshold voltage of the transistor and, thus, reducing its switching speed. Safe margins must be added to the circuit design in order to avoid timing faults. This means that either a lower frequency than the maximum allowed or a larger voltage than the minimum necessary has to be applied. All these margins lead to energy efficiency losses.

Many in-situ delay monitors have been proposed to mitigate not only Process-Voltage-Temperature variations but also aging effects. They are inserted in the circuit critical paths and raise warning when the path delay is close to the clock period. Canary structures such as ring oscillators have been proposed to evaluate aging. Basically, two identical structures are integrated, one being stressed while the other one is not. It is possible then to obtain an information about aging by comparing both oscillating frequencies. However, the degradation experienced by canary structures is not necessarily the one experienced by the circuit itself because aging effects depend on signal probability that cannot be emulated by ring oscillators.

Main Results

The proposed method for estimating aging is based on an Adaptive Frequency Scaling (AFS) system with in-situ delay monitors and local temperature sensors, e.g. an AFS system with a closed-loop control that increases or reduces the clock frequency until the number of warnings generated by the delay monitors is equal to a given value. This value is chosen in such a way that the occurrence of timing faults is zero or less than an accepted boundary. Therefore, the clock frequency is always equal to the maximum $f_{\it max}$ allowed. This latter depends on 4 variables, namely, process, supply voltage, temperature and aging variations. The process is considered static (i.e. constant over time). The temperature (T) can be dynamically measured through the embedded sensors. The supply voltage V_{dd} is assumed to be constant here, but it could be also measured through embedded sensors. Thus, it is possible to know the circuit degradation over time by tracking $f_{\it max}$ evolution along with T and V_{dd} variations. By applying a data fusion technique, the

circuit performance shift due exclusively to aging (A) is computed, i.e. $f_{max}(A)$ is extracted from $f_{max}(T,V_{dd},A)$. Therefore, the main contribution of this work is to estimate the real degradation suffered by the circuit independently from supply voltage and temperature variations. The workload also impacts the occurrence of warnings since it determines which paths are or are not activated. Here, a test subroutine is used to stimulate all monitored critical paths, the circuit activity being the same for each test.

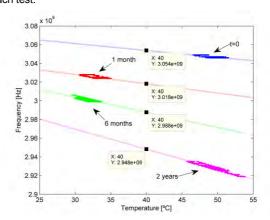


Figure 1. Results at $V_{dd}=1.2V$ for 4 different stress times (1000 tests each).

Fig. 1 shows tests performed at $V_{dd}=1.2V$ for 4 different stress times and given temperature ranges. The different lines, obtained using mean squares, correspond to $f_{max}(T)$ for the different stress times. As a consequence, for a given temperature T, the frequency shift due solely to aging A can be evaluated. Also, by monitoring f_{max} and T, one can evaluate the circuit aging.

Perspectives

The case when V_{dd} is not constant will be studied in future works. It may correspond to large voltage drops as well as when Dynamic Voltage and Frequency Scaling strategies are applied.

RELATED PUBLICATIONS:

[1] Altieri, M.; Lesecq, S.; Beigne, E.; Heron, O. & Puschini, D., "Tracking BTI and HCI effects at circuit-level in adaptive systems", Proceedings of the 14th IEEE International NEWCAS Conference, NEWCAS 2016, 26-29 June 2016.

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LEVERAGING COMPILATION: SOFTWARE COUNTERMEASURES AGAINST PHYSICAL ATTACKS

RESEARCH TOPIC:

Software countermeasures, physical attacks, side-channel attacks, fault attacks.

AUTHORS:

D. Couroussé, B. Robisson, T. Barry, H. Le Bouder (INRIA), J.L. Lanet (INRIA), P. Jaillon (EMSE), O. Potin (EMSE).

ABSTRACT:

Physical attacks represent the strongest security threat against embedded systems. A secured system usually integrates protection mechanisms at several levels: attack detection mechanisms in the hardware, dedicated cryptographic IPs, and hardened software components. We provide code generation tools to automatically apply software protection schemes against both side channel attacks and fault attacks (1) using traditional static compilation techniques, and (2) in a new paradigm shift: code polymorphism, which involves runtime code generation.

SCIENTIFIC COLLABORATIONS: LHS - INRIA Rennes, École Nationale Supérieure des Mines de Saint-Étienne

Context and Challenges

Physical attacks represent an effective mean to break the security protections of a computing system. They are mostly used against embedded systems, where the device under attack is literally in the hands of the attacker, but these attacks are also effective against other computing systems such as general purpose computers and servers. Side-channel attacks are passive, observation-based attacks; fault attacks are active, perturbation-based attacks. Secured components must be protected against all these attack paths. Usually, the protection schemes are ad hoc; they are added iteratively to the design, and nowadays the industry still misses tools in order to automatically apply these protection schemes. Our research works focus on the ability to apply automatically countermeasures on legacy, unprotected software components, by leveraging compilation.

Main Results

We define polymorphism as the capability to change the behaviour of a secured component at runtime without altering its functional properties. Polymorphism was shown to effectively increase the difficulty to perform side-channel attacks [2]

Side-channel and fault attacks mostly target cryptographic components because cryptography is considered secure against cryptanalysis. However, taking into account some knowledge about its implementation (hardware or software), it is possible to break these security assumptions. Outside of cryptography, authentication procedures (e.g. verifyPin) are also targeted by these attacks [3]. Polymorphism is a generic countermeasure that is applicable to any component: cryptography, authentication procedures or other ones such as system or applicative generalpurpose components.

We developed a secured compiler based on the industry-grade compilation framework LLVM [1]. The compiler is able to automatically apply a protection scheme against fault attacks, on a portion of the source code selected by the software developer. The protection scheme consists in duplicating every instruction in the protected section of the program, so that it is not possible to attack the program with an instruction skip fault model. The protection scheme has been formally verified for the ARM thumb instruction set.



Figure 1. Test bench of fault injection.

Figure 2 provides a performance comparison of the same protection scheme applied by our work and by Moro et al (cf [1]), where the protection scheme was applied semi-manually after the compilation step. Figure 2 illustrates the fact that in our case the cost of the protection is mitigated by the performance optimisations applied by the compiler on the protected code.



Figure 2. Security overheads in terms of execution time and code size for two implementations of AES [1].

Perspectives

Automatic compilation and of software verification countermeasures against physical attacks. Project PROSECCO (ANR 2015)

RELATED PUBLICATIONS:

[1] Barry, T.; Couroussé, D. & Robisson, B. (2016), "Compilation of a Countermeasure Against Instruction-Skip Fault Attacks" In CS2 - Third Workshop on

Cryptography and Security in Computing Systems. ACM, Vienna.

[2] Couroussé, D.; Barry, T.; Robisson, B.; Jaillon, P.; Potin, O. & Lanet, J.-L. (2016), "Runtime Code Polymorphism as a Protection against Side Channel Attacks" In WISTP. International Conference on Information Security Theory and Practice', Springer, Grece.

[3] Le Bouder, H.; Barry, T.; Couroussé, D. & Lanet J.L. (2016), "A template attack against VERIFY PIN algorithms", SECRYPT, Portugal.

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ULTRA LOW-POWER AND LOW-ENERGY 32-BIT DATAPATH AES ARCHITECTURE FOR IOT APPLICATIONS



RESEARCH TOPIC:

Advanced Encryption Standards (AES); Low-Power; Low-Energy; Internet-of-Things (IoT)

AUTHORS:

D.-H. Bui, D. Puschini, S. Bacles-Min, E. Beigné, X.-T. Tran (VNU-UET)

ABSTRACT:

Security and power/energy consumption are some of the main enablers for IoT. In this work, we propose a novel Advanced Encryption Standard (AES) microarchitecture with 32-bit datapath optimized for low-power and low-energy consumption targeting securing IoT applications. The implementation results in TSMC 65nm technology show that our design saves 20% of area or 20% of energy per bit at the same area when compared with the current 32-bit datapath designs. Our architecture provides medium throughput (28Mbps@10MHz@1.3V@120µW) with the core area equivalent to 8-bit designs for RFID and IoT applications.

SCIENTIFIC COLLABORATIONS: VNU UNiv. of Eng. & Tech., Vietnam National University (Hanoi)

Context and Challenges

The development of the Internet-of-Things (IoT) raises the concerns about the security. It used to be an additional feature for integrated systems but it is, nowadays, crucial in many applications. However, security functions not only reduce the system throughput but also increase power/energy consumption which is important for IoT applications. One way to optimize the throughput and power consumption is to implement the security algorithms in hardware with the trade-offs among security, area, throughput, power consumption and energy consumption. In this work, we focused on optimizations for hardware implementation of AES, one of the main algorithms used in the current IoT proposals such as IEEE 802.15.4, LoraWan, Sigfox...

Main Results

Our proposed architecture contains two parts: encryption path and key expansion as shown in Fig. 1. The encryption path includes four parts: a 128-bit state register, 4 substitution boxes (S-boxes), a *MixColumns*, and a 3×32-bit output/temporary register while the key expansion contains a 128-bit register, 4 S-boxes.

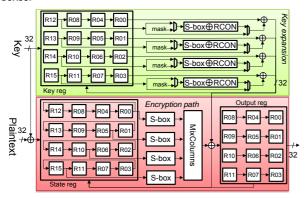


Fig. 1. Proposed AES 32-bit datapath architecture

Area and power consumption are saved by reorganizing the datapath to remove *ShiftRows* step, minimizing control logics by using shift registers; and by doing key expansion on the fly.

Power consumption is optimized further by applying a clock gating strategy to shift registers; gating the input of S-boxes in key expansion; and choosing a low-power S-box implementation. Throughput is maximized by doing key expansion and encryption in parallel using 8 S-boxes (44 cycles/128-bit encryption).

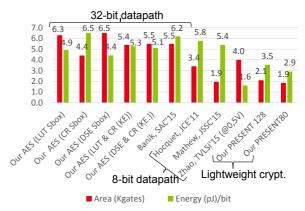


Fig. 2. Estimated results in TSMC 65nm Technology.

Our estimated results with different S-box implementations are presented with in Fig. 2. Comparing with state of the art architecture, our design saves up-to 30% energy consumption with Decode-Switch-Encode (DSE) S-boxes, 20% energy consumption with the same gate counts in case of the deployment of the mixed style of S-boxes, or 20% smaller in area with Canright (CR) S-boxes with nearly the same energy/bit. In comparison with other 8-bit designs, our design with DSE S-boxes is the second best in energy/bit.

Perspectives

Our proposed architecture shows a good trade-off among area, power/energy consumption and throughput which is suitable for future IoT applications. In the future, we would like to apply more advanced low-power techniques such as back-biasing with subthreshold voltage to fully evaluate the capabilities of the proposed architecture in terms of power/energy consumptions and to evaluate its security features under different attacks.

RELATED PUBLICATIONS:

[1] D.-H. Bui, D. Puschini, S. Bacles-Min, E. Beigne and X.-T. Tran, "Ultra low-power and low-energy 32-bit datapath AES architecture for IoT applications," in Proceedings of the 2016 IEEE International Conference on IC Design and Technology, ICICDT 2016.

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DYNAMIC EXECUTION OF SECURE QUERIES OVER HOMOMORPHIC ENCRYPTED DATABASES

RESEARCH TOPIC:

Cryptography, Security and Privacy, Database

AUTHORS:

S. Oana, S. Carpov, R. Sirdey

ABSTRACT:

In this work, we propose and analyze two different methods in which client requests are dynamically executed on homomorphically encrypted data. Dynamic compilation of the requests allows to take advantage of the different optimizations performed during an off-line step on an intermediate code representation, taking the form of Boolean circuits, and, moreover, to specialize the execution using runtime information. We assess the complexity and the efficiency of the protocols proposed in the literature in terms of execution time, accuracy and communication overhead.

Context and Challenges

The emergence of cloud storage and computing platforms allows users (individuals or businesses) to outsource their data and their computation in the cloud and therefore, have access to software, platforms and infrastructures sold as a service, through the Internet. A major drawback for the large-scale adoption of the cloud for storing data and its processing lies in the related security issues. A possible solution for the widespread of data outsourcing can be to use homomorphic encryption allowing encrypted data storage and computations on the server's side.

Main Results

The two possible methods presented in this work are to be applied in the general client-server paradigm, with only some small changes in the data to be transmitted between the client and the server.

Method 1 - The overall architecture is shown on figure 1. A preliminary transaction (Steps 0.1 and 0.2) consists in the transmission to the service provider of the data to be stored along with public key pk and relinearization key evk, generated by the client and needed for encryption, respectively for evaluating operations involving multiplications on encrypted data. Also, the user sends the overall Boolean circuit (Step 0.3), defined in function of the type of requests the system can support, to the database manager system (DBMS) which stores it for the dynamic compilation of the query.

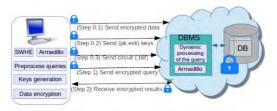


Figure 1 - Method 1 architecture overview

Method 2 is shown on figure 2 - The only difference with regards to the first method, visible at this level, consists in sending the

binary of the source code instead of the boolean circuit (Step 0.3). As before, during the preliminary transactions (Steps 0.1 and 0.2) the keys and the encrypted data to be stored are send to the database server and step 1 consists in sending the encrypted attribute values and the encrypted requested values.

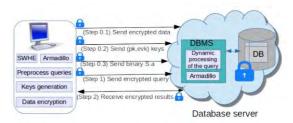


Figure 2 - Method 2 architecture overview

In Table 1 we show the execution times of a selection query obtained when varying the number of records (N) and the number of selected attributes (K). As expected, the execution time and the size of the results increases with K and with N, but it is independent of parameter m (the number of columns). For both methods, most of the time is consumed by the dynamic interpreter of the request with similar time (column "Interpreter") since at the end they execute the same Boolean circuit. We remark however that the overall time of the first method is slightly superior to the one obtained with the second method (column "Total"), mainly due to the transformation into BLIF file.

N	K	1st method				2nd method				Size (kb)
14		Transform BLIF	2nd ABC opt	Interpreter	Total	Obtain BLIF	ABC opt	Interpreter	Total	Size (KD)
.5	1	0,49	0,05	1,7393	2,2793	0,0053	0,03	1,633	1,6683	244
	4	0,45	0,06	11,754	12,264	0,0153	0.06	12,09	12,1653	524
10	1.	0,86	0,08	3,166	4,106	0,009	0,04	3,17	3,219	244
	4	0,82	0,1	24,2	25,12	0,034	0,09	23,387	23,511	1126,4
100	1	7,35	0,64	31,31	39,3	0,08	0,3	30,84	31,22	4812,8
	4	8,45	-1,1	240,03	249,58	0,282	0.9	245,29	246,472	11264

Table 1 - Execution time for the two methods

Perspectives

In this work, we described two possible methods for dynamic compilation and we showed that it is possible to directly evaluate queries using homomorphic primitives. We believe that the performances will be improved in the years to come through the development of more efficient encryption schemes, circuit optimizations and the exploration of the parallelism offered by modern computing systems.

RELATED PUBLICATIONS:

[1] O. Stan, S. Carpov, R. Sirdey "Dynamic Execution of Secure Queries over Homomorphic Encrypted Databases", Proceedings of the 4th ACM International Workshop on Security in Cloud Computing, 2016.

[2] S. Carpov, P. Dubrulle, and R. Sirdey. "Armadillo: A compilation chain for privacy preserving applications", Proceedings of the 3rd International Workshop on Security in Cloud Computing, SCC '15, pages 13–19, New York, NY, USA, 2015. ACM

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INDUSTRIAL IOT APPLICATION DEVELOPMENT WITH A RELIABLE COORDINATION PLATFORM



RESEARCH TOPIC:

Coordination, distributed system, reliability

AUTHORS:

O. Antoni, L.F. Ducreux, M. Louvel, F. Pacull (Bag-Era), A. Ndeye Sylla, M.I. Vergara-Gallego

ABSTRACT:

The Internet of Things (IoT) includes sensors, actuators, but also independent products and different networks. This raises several challenges to developers. They must handle heterogeneous and independent systems, unreliable systems and communications. In addition, it is required to include advanced user interfaces and to reduce product development time. In this work, we rely on LINC, a coordination environment developed at CEA, to answer these challenges. LINC relies on distributed transactions that ensure the consistency of the whole system by guarantying that in a transaction, either all the actions are done successfully or none.

Context and Challenges

The Internet of Things (IoT) has become more and more popular in the last decade. Emerging technologies have allowed to connect anything from a tiny sensor to a cloud algorithm or a full factory. This raises new challenges for applications' and systems' developers. First, they have to integrate independent systems to build new applications, systems and products. Second, user interfaces are expected to be used by any web device (smart phone, tablet or PC) and to include physical components of the real system. Finally, the IoT is by definition unreliable; to meet industrial requirements, it is mandatory to provide a reliable environment to developers and during the system execution.

Main Results

This work relies on LINC, a coordination environment developed at CEA. LINC provides a rule based language to observe the system and distributed transactions engines to update it. LINC is based on tuple spaces which provide time and space decoupling between data producers and data consumers.

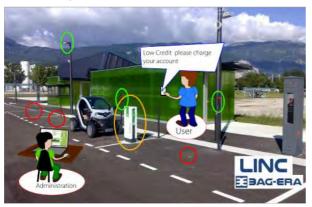


Fig. 1: Smart parking demonstration

In [1] we use LINC for rapid prototyping of IoT applications including several independent systems and advanced user interfaces. Fig. 1 shows the smart parking case study whose application was built in just a few weeks.

In [2] we provide a graphical design tool for building automation. This allows to design building rules across several Building Management Systems and including any devices.

In [3] we explain how we can increase the reliability of IoT applications with LINC transactional guaranties. A part of the LINC protocol is embedded in the sensors and actuators. The consistency of the system is then enforced by the transactions which guaranty that either all the actions are correctly done at once or none of them. Fig. 2 shows a ball and plate demonstrator ensuring that even with unreliable microcontrollers and unreliable wireless communications, the ball never falls [3, 4]. From the developers' point of view only 6 lines of codes are required.

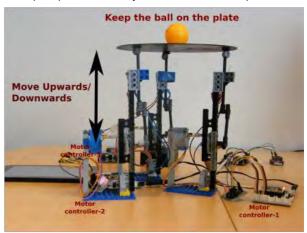


Fig. 2: Reliable distributed control demonstration.

Finally in [5] we show how LINC is used to enforce the correct execution of a distributed control system. The control system is designed by control engineers that benefit directly from LINC to abstract from the complexity of the IoT.

Perspectives

Future work will focus on extending our collaborations with control engineers and discrete control technics to provide robust, autonomous and self-evolving distributed systems.

RELATED PUBLICATIONS:

- [1] Ducreux, L-F, et al. "Rapid prototyping of complete systems, the case study of a smart parking." Rapid System Prototyping 2015 International Symposium on. IEEE,
- [2] Louvel M, Pacull F, Vergara-Gallego M.I. "Coordination Scheme Editor for building management systems." IECON-42nd Annual Conference IEEE, 2016.
 [3] Louvel M, Pacull F, Vergara-Gallego M.I. "Reliable Control through Wireless Networks." IECON-42nd Annual Conference IEEE, 2016.
 [4] Louvel M, Pacull F, Vergara-Gallego M.I. "Demo: Ball and Plate Wireless Control" Int. Conf. Embedded Wireless Systems and Networks. Junction Publishing, 2016
- 5] Vergara-Gallego, M.I., et al. "Implementation of an Energy Management Control Strategy for WSNs using the LINC Middleware." Proceedings of the 2016 Int. Conf. Embedded Wireless Systems and Networks, Junction Publishing, 2016

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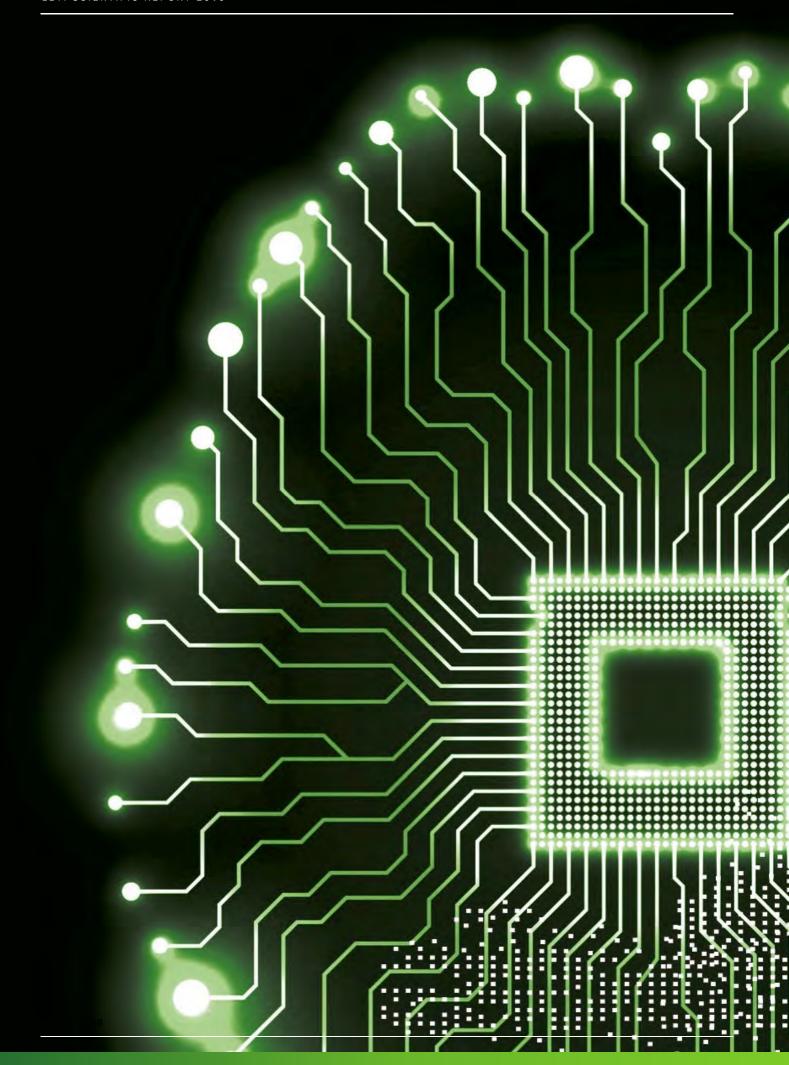
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6.

EMERGING TECHNOLOGIES & PARADIGMS

- Quantum Electronic
- Monolithic 3D
- TFETs and RRAM Memories
- Photonic Interposers
- Chaos Time DomainReflectometry
- Spiking Neural Networks for

Mathematical Operations

TOWARDS SILICON-BASED QUANTUM ELECTRONIC: CRYOGENIC OPERATION OF SOI ELECTRON PUMPS AND RING OSCILLATORS



Quantum bits, cryogenic CMOS operation

AUTHORS:

P. Clapera, X. Jehl, L. Hutin, S. Barraud, A. Valentian, S. De Franceschi, M. Sanguer, M. Vinet

ABSTRACT:

Breakthroughs in silicon spin quantum bits have been made recently, with the demonstration of the first full CMOS realization of a spin quantum bit on SOI. This motivates the need to develop interface circuits between the classical CMOS world and the silicon spin quantum bits. Thus, interface circuits has to be designed and tailored to operate at cryogenic temperature to provide low-noise and very low-thermal budget control signals. Work done demonstrates the operation of a ring-oscillator based circuit designed to generate RF signals on chip, as well as new electron pumps fabricated using only optical lithography. Design, cryogenic operation and performances are discussed.

SCIENTIFIC COLLABORATIONS: INAC (Grenoble)

Context and Challenges

Silicon spin quantum bits (qubits) became, in a few years only, a solid candidate for a practical implementation of a scalable quantum computer. Very recently a full CMOS realization of a spin quantum bit on SOI has been unveiled. It makes possible, for the first time, the design of a scalable hybrid quantum/classical CMOS circuit, bringing the best of both worlds.

CMOS-based interface functions must therefore be designed to scale up to several qubits, and meet the stringent requirements of very low temperature experiments. Oscillators and high precision low current sources are among the needed functions.

Main Results

The FDSOI technology used at LETI enables to co-integrate classical Field Effect Transistors (FET) and Single Electron Transistors (SET). The difference between the two is that width of a SET is much narrower (45nm). The SET/FET co-integration enables to implement qubits and its control logic on the same chip, which is obviously scalable in terms of number of qubits.

However, operation in the SET regime is only possible at very low temperatures, i.e. several Kelvins. The difficulty with low-temperature circuit design lies in the very small thermal power budget available, to cool the circuit when it is operating. The control circuitry must therefore be ultra-low power.

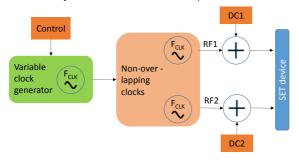


Fig. 1 - Schematic of the ring-oscillator-based circuit to generate two phase-shifted RF signals

The first control circuit considered is dedicated to generate RF signals for controlling the two gates of a SET device [1]. Those gates need to be open in opposite phases for enabling a single electron to enter the device (Coulomb blockage principle). This can then be used as an electron pump in order to generate a very well controlled reference current, whose value is only function of the pumping frequency (times the electron charge).

The RF signals generator is first composed of a Voltage-Controled Oscillator (Green box of Fig. 1): it is a 20-stage ring oscillator. The obtained clock is then decomposed into two non-overlapping clocks of same frequency. The amplitude of those signals is then downscaled to below 1mV thanks to a capacitive divider. A DC voltage, up to several volts, is finally added using a 1MOhm resistor.

The RF signals generator has been measured down to a temperature of 4.2K. As can be seen in Fig. 2, the lower the temperature, the steeper the clock frequency dependency on the control voltage: this is explained by the steeper subthreshold slope of the FDSOI technology at low temperature.

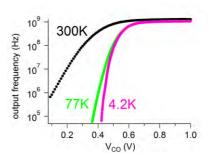


Fig. 2 - Output clock frequency as function of the control voltage $% \left(1\right) =\left(1\right) \left(1\right)$

Perspectives

One direct outcome of this work is the possibility to redefine the Ampere standard using high frequency electron pumps. A longer term perspective is the design of quantum circuit using multiple qubits.

RELATED PUBLICATIONS:

[1] P. Clapera, X. Jehl, L. Hutin, S. Barraud, A. Valentian, S. De Franceschi, M. Sanquer and M. Vinet, "Cryogenic operation of SOI electron pumps and ring oscillators," IEEE Silicon Nanoelectronics Workshop, Honolulu, USA, June 2016

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IMPACT OF INTERMEDIATE BACK-END OF LINE ON **BOTTOM TIER STANDARD CELLS CHARACTERISTICS FOR** 3D SEQUENTIAL INTEGRATION



RESEARCH TOPIC:

Coolcube™, Monolithic 3D, Place&Route, Back-End of Line

AUTHORS:

O. Billoint, M. Brocard, S. Thuries, G. Berhault, S.K. Lim (GTCAD)

ABSTRACT:

In the 3D sequential process development context, design strategies are investigated and performances need to be predicted. This process enables fabrication of stacked layers of transistors but conductors/dielectrics for intermediate Back-End Of Line (iBEOL) need to be adapted for thermal budget and contamination risk reasons. Standard cells electrical characteristics will be thus impacted so a study was performed for various iBEOL material options. Timing degradation can be up to 20% in the worst case.

SCIENTIFIC COLLABORATIONS: Georgia Tech University (Atlanta, USA))

Context and Challenges

3D monolithic integration is a breakthrough technology raising great interest in the semiconductor industry for its promising performances in numerous applications. Also called 3D Sequential technology, this process enables the fabrication of circuits using multiple stacked layers of devices connected at the transistor scale with vertical inter-tier via (Fig. 1). It enables higher transistors density, reduced footprint and shorter routing wire length for a given technology node compared to 3D TSV-based technology. The different tier connection is enabled by etching a via which can be as small as 50nm wide and 150nm tall with a 100nm pitch, in 14nm technology. Yet, 3D sequential is a disruptive technology which leads to a lot of technological and design challenges to lay ahead. In designer's field, numerous studies on two-tiers 3D monolithic designs predict noticeable performance improvements.

Main Results

Power and timing characteristics of standard cells integrated on the bottom tier of a 3D sequential circuit have been simulated. In order to have a high-volume production iBEOL bottom tier metallization thermal stability, standard cells are routed using materials with higher permittivity and resistivity compared to conventional 2D integration. RC parasitic netlists were extracted from representative standard cells from their layout views, using a commercial parasitic extraction tool for a high electrical analysis accuracy.

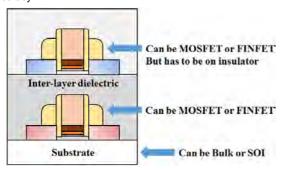


Fig. 1: sequential 3D process description

We performed a sensitivity analysis (two cases presented Fig. 2) to separate resistive effect from dielectric one's in order to provide relevant guidelines for designers to achieve 3D sequential circuits with the same performances on the top and bottom tier (less than 5 % difference) and take full advantage of the sequential technology.

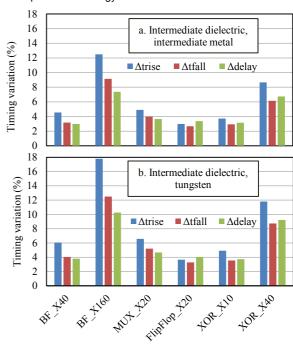


Fig. 2: timing variation for different standard cells depending on BEOL process option.

Perspectives

Future work should focus on using modified characteristics standard cells for bottom tier and evaluate cell-on-cell 3D physical implementation when commercial tools will be available.

RELATED PUBLICATIONS:

[1] M. Brocard, G. Berhault, S. Thuries, F. Clermidy, P. Batude, C. Fenouillet-Beranger, L. Brunet, F. Andrieu, F. Deprat, J. Lacord, O. Rozeau, G. Cibrario, O. Billoint, "Impact of intermediate BEOL technology on standard cell performances of 3D VLSI", ESSDERC 2016.
[2] M. Brocard, R. Boumchedda, J. P. Noel, K. C. Akyel, B. Giraud, E. Beigne, D. Turgis, S. Thuries, G. Berhault, O. Billoint, "High density SRAM bitcell architecture in 3D sequential CoolCube™ 14nm technology", S3S 2016.

[3] F. Clermidy, O. Billoint, H. Sarhan, S. Thuries; "Technology scaling: the CoolCubeTM paradigm", S3S 2015.

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TFET NEGATIVE-DIFFERENTIAL-RESISTANCE-BASED MEMORY AND FLIP-FLOP DESIGN FOR LOW-VOLTAGE AND LOW-POWER APPLICATIONS

RESEARCH TOPIC:

SRAM, TFET, Flip-Flop, Sense Amplifier

AUTHORS:

N. Gupta (ISEP), A. Makosiej, A. Vladimirescu (ISEP), A. Amara (ISEP), C. Anghel (ISEP)

ABSTRACT:

In this work the application of TFET and its Negative Differential Resistance property, and hybrid CMOS/TFET design was investigated, focusing on the SRAM and flip-flop design. Proposed 3T-TFET SRAM cell supports aggressive voltage scaling without impacting data stability and allows performance boosting techniques without impacting cell leakage. 0.35 fA/bit leakage current is obtained. The proposed flip-flop works for supply voltages from 0.3V to 0.6V. Leakage is improved by 3 to 7 decades in comparison to state-of-the-art TFET, FinFET and MOSFET designs.

SCIENTIFIC COLLABORATIONS: ISEP (Paris)

Context and Challenges

The relevance of power optimization is increasing with growing demand of energy efficient devices for portable applications, like Internet of Things (IoT), wireless sensor nodes and implantable medical devices. As these systems typically exhibit long inactivity periods, the reduction of the standby leakage of the system should be focused in order to improve the battery life time. The Tunnel FET emerges as a promising device for such applications due to a much lower leakage than the standard CMOS devices. Moreover due to the unidirectional behavior and presence of Negative Differential Resistance (NDR) under reverse voltage bias, new circuit architectures can be envisaged.

Main Results

Fig.1b depicts the principle of operation of the NDR latch formed by 2 reverse oriented devices as in Fig.1a (M₀,M₁). The reverse biased TFET exhibits a gate voltage controlled current hump near 0. As the reverse voltage increases the current drops up to a point where it increases without the control of the gate (in our device this occurs past 0.6V). By biasing the device to take advantage of the reverse region where only either the hump or minimum current is present a behavior with only 2 stable points as in Fig.1b can be obtained. In such configuration the logical '1' and '0' are maintained by the "hump" of either Mo or Mi device, while the current of the other device is minimum.

Using this latch as a base various novel circuits can be envisaged. Fig.1a depicts a 3T TFET bitcell [1,2]. The memory latch is programmed via VDD and VSS while read is done via the M₃ device. Single device is sufficient for the read port as long as the voltage range is within controlled zone under reverse bias.

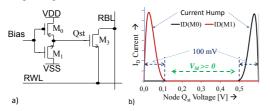


Figure 1 (a) current characteristics of the 2T TFET latch using NDR, and (b) 3T SRAM cell

In order to further improve the performance of the 3T bitcell where the read is single ended a novel NDR skewed inverter based sensing method was developed [3] allowing sensing at a reduced voltage drop on the read bitline and hence improving the memory access time

Application of the 2T NDR latch in the flop-flop design allowed obtaining a competitive novel architecture [4] while limiting the number of used devices to only 14 as compared to 18-27 in the state-of-the-art approaches. The proposed flip-flop operates with ultra-low leakage current (< 3fA) and operates for voltages from 0.3V to 0.6V. Comparison of the performance of the new TFET flip-flop was made with CMOS and FinFET (LSTP and HP) standard Master-Slave flip-flop implementations (Fig.2). Reduction of 4 to 7 decades and 3 to 5 decades in comparison to MOSFET and FinFET implementations was achieved for leakage and dynamic power, respectively.

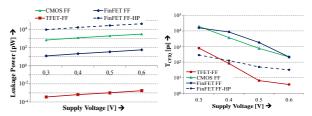


Figure 2 Leakage power and Clock-to-Q in function of supply voltage for new TFET flip-flop architecture and standard master-slave flip-flop implemented with CMOS and FinFFT devices

Perspectives

The unique properties of the TFET device, i.e. unidirectionality and negative differential resistance, call for reconsideration and/or re-optimization of existing circuit and memory architectures to adapt them to the device behavior. As demonstrated on the SRAM and flip-flop examples, the exploitation of the TFET features allows the design of compact low-voltage and low-power circuits while maintaining high performance. Given the alignment of TFET performance with emerging IoT market demands, further work on the TFET-customized architectures can be expected.

RELATED PUBLICATIONS:

- [1] N. Gupta, A. Makosiej, A. Vladimirescu, A. Amara, C. Anghel, "3T-TFET bitcell based TFET-CMOS hybrid SRAM design for Ultra-Low Power applications", DATE 2016
- [2] N. Gupta, A. Makosiej, A. Vladimirescu, A. Amara, C. Anghel, "Ultra-compact SRAM design using TFETs for low power low voltage applications", ISCAS 2016 [3] N. Gupta, A. Makosiej, A. Vladimirescu, A. Amara, S. Cotofana, C. Anghel, "TFET NDR skewed inverter based sensing method", NANOARCH 2016
- N. Gupta, A. Makosiej, A. Vladimirescu, A. Amara, C. Anghel, "Ultra-Low-Power compact TFET Flip-Flop design for high-performance low-voltage applications." **ISQED 2016**

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CAPACITOR BASED SNEAKPATH COMPENSATION CIRCUIT FOR TRANSISTOR-LESS RERAM ARCHITECTURES



RESEARCH TOPIC:

Crosspoint, Non-Volatile Memory, RRAM, SneakPath, Compensation circuit

AUTHORS:

A. Levisse, B. Giraud, J.P. Noël, M. Moreau (IM2NP), J.M. Portal (IM2NP)

ABSTRACT:

Transistor-Less Resistive memory architectures using 1Selector-1resistance bitcells suffer from performances loss due to sneaking current through unselected bitcells. Beyond the back end of line selector design, circuit design solutions have to be pushed in order to improve precision during programming steps. In this work we propose a novel capacitor based 2-steps SneakPath (SP) compensation circuit for transistor-less architectures of resistive memories. Compared to standard SneakPath compensation circuits, it ensures up to 20x of area improvement and more than 3x reduction of the variability effects for a 28nm CMOS node.

SCIENTIFIC COLLABORATIONS: IM2NP (Marseille)

Context and Challenges

In Crosspoint memory arrays, a Back-End-of-Line (BEoL) selector is integrated in series in the bitcell in order to provide a high density bitcell (4F²). However, BEoL selectors suffers of high leakage varying with the process, the RRAM state or the temperature. Thus, cycle-to-cycle and device-to-device variability impacts a lot the SP and thus, the RRAM programming conditions.

Main Results

In this work we introduce an innovative 2-steps sneaking current (Sneakpath - SP) compensation circuit for crosspoint arrays. This architecture complete previously published one-step .SP compensation circuit [1]. Sample and Compensate 2-steps SP compensation circuits consists first in a calibration step that measures the SP current in the selected line. Then, the programming pulse is applied and the measured SP current is added to the RRAM programming current.

The proposed analog-based SP compensation circuit [2] uses a capacitor instead of a digital circuit to sample and compensate the SP. This enables a huge reduction of the occupied area as shown Fig. 1.

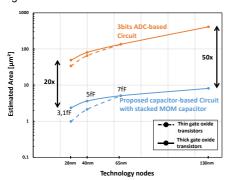


Figure 1: Occupied area estimation for 3bits ADC and capacitor based SP compensation circuits for several technology nodes. Stacked MIM capacitor without area increase provides 20x area improvement.

The area estimation takes into account the use of thicker oxide transistors mandatory to manage the high voltages needed to program 1S1R bitcells.

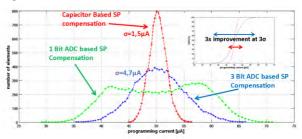


Figure 2: Probability density function of programming currents for different SP compensation architectures. 1bit ADC (green curve), 3bit ADC (blue curve) and capacitor based (red curve). Architectures are compared with 10.000 Monte-Carlo simulations with CMOS, selector VT and non-selected resistances variations.

Fig. 2 shows the distributions of programming current in the selected resistance considering CMOS variability in 28nm FDSOI technology node, Selector variability and random non selected resistance states with 10.000 Monte Carlo simulations. For capacitor based writing circuit, the programming current distribution (red) is reduced compared to ADC based approach (blue and green). In terms of CMOS variability, the proposed capacitor approach uses the same transistor as the current measurement and current limiter for SP. This approach eliminates the mismatch between measure transistors and limit transistors which exists in the digital approach. It also eliminates the quantization error while storing the analog value in a capacitor. The proposed capacitor based SP compensation approach provides 3x narrower distribution than 3bits ADC based digital approach due to simpler circuitry and CMOS variability resistant design.

Perspectives

Programming current control improvements increase the RRAM endurance and reduce its variability. With the lowering of programming currents, accurate SP compensation circuits such as [1] and [2] appears to be mandatory.

RELATED PUBLICATIONS:

[1] A. Levisse, B. Giraud, J-P. Noel, M. Moreau, J-M. Portal, "SneakPath Compensation Circuit for Programming and Read Operations in RRAM-based CrossPoint Architectures", NVMTS 2015.

[2] A. Levisse, B. Giraud, J-P. Noel, M. Moreau, J-M. Portal, "Capacitor based SneakPath compensation circuit for transistor-less ReRAM architectures", Nanoarch 2016.





SILICON PHOTONICS DRIVERS AND ARCHITECTURES FOR INTERCHIP/INTRACHIP OPTICAL COMMUNICATIONS USING PHOTONIC INTERPOSERS

RESEARCH TOPIC:

Silicon photonics, Optical Networks on Chip

AUTHORS:

Y. Thonnart, J.L. Gonzalez Jimenez, G. Waltener

ABSTRACT:

Silicon photonics is a tremendous opportunity for more efficient communication for high-performance computing. In these works, we investigate the potential benefits of short-distance interchip/intrachip optical communication, leveraging on possible 3D integration of CMOS chiplets on silicon photonic interposers. This goal is taken from both technological and system-level ends. We develop and characterize the optical devices and their CMOS drivers, while leading studies at architectural level to optimize the system efficiency using a sparing co-design of the devices, links, architectures and protocols suited to ultra-short-distance communication.

SCIENTIFIC COLLABORATIONS: Columbia U. (USA), HKUST (Hong-Kong), INL (France), IEF (France)

Context and Challenges

With the scaling-down of CMOS transistor dimensions, highperformance integrated circuits are now facing an increasing problem of on-chip communication density and latency. Global communication routing across the die area can now hardly be achieved within tens of clock cycles, while suffering costly bandwidth/consumption tradeoffs. Besides, diminishing process yield on larger chips advocates for cost-reduction thanks to slicing of these chips on smaller chiplets to be assembled on interposers. In these works, we investigate the use of silicon photonics to develop dense communication and routing on optical interposers for future high-performance computing chips.

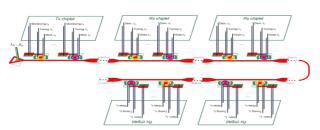


Fig. 1. WDM Optical links on interposer between chiplets using silicon photonic microring modulators and filters

The major challenges for this technology to emerge is the integration density of many optical functions and the associated power budget. The static consumption related to the control of resonant optical devices may be mitigated by wavelength-division multiplexing of the waveguides and factoring of the transmitters and receivers within the topology. Nevertheless, the associated losses and crosstalk between channels must be analyzed and constrained to a minimal level.

Main Results

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In papers [1-2], we investigate the different tradeoffs for the design of efficient electro-optical links. We show that a minimum energy point exists for intermediate link datarates between 8 and 16 Gbps depending on the driver technology node, where the serialization and driver costs can be kept moderate with efficient and compact implementation. Paper [3] extends the point to point

link concept to optical network on chip topologies, and shows the need for sufficient wavelength spacing in complex topologies to limit SNR degradation due to crosstalk between channels.

Paper [4] focuses on the optimization and characterization of optical waveguides and microring resonators to take benefit of the silicon photonic platform for optical interposers. As waveguide length may reach about 10 cm in 4-8 cm² interposers, 0.2 dB/cm low-loss waveguides and high-Q optical modulators have been developed. Papers [5-6] show a 65nm CMOS implementation of efficient Tx and Rx drivers at 10 Gbps for these optical devices.

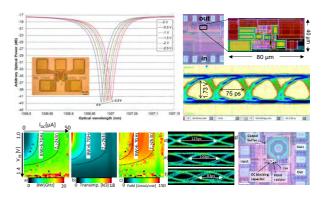


Fig. 2. Characterization results of elementary building blocks for optical modulators and associated CMOS driver (top), and for photodiodes and associated TIA (bottom).

Perspectives

Based on the photonic and CMOS building blocks and the system analyses presented here, complete prototypes of silicon photonic links and optical network on chips architectures are under development. These demonstrators should open the way to industrial adoption of silicon photonics for high-performance processor architectures.

RELATED PUBLICATIONS:

- [1] Polster, R., et al., "Efficiency Optimization of Silicon Photonic Links in 65-nm CMOS and 28-nm FDSOI Technology Nodes", IEEE TVLSI, 24 (12).
- [2] Bahadori, M., et al., "Energy-bandwidth design exploration of silicon photonic interconnects in 65nm CMOS", 5th IEEE Optical Interconnects Conference, OI 2016. [3] Duong, L.H.K., et al., "Coherent and Incoherent Crosstalk Noise Analyses in Interchip/Intrachip Optical Interconnection Networks", IEEE TVLSI, 24 (7). [4] Reboud, V., et al., "Experimental study of silicon ring resonators and ultra-low losses waveguides for efficient silicon optical interposers", Proc. SPIE Vol. 9753.

- Gonzalez, J.L., et al., "10 Gbps, 560 fJ/b TIA and modulator driver for optical networks-on-chip in CMOS 65nm", IEEE NEWCAS 2016.
- [6] Bernabe, S., et al., "On-board silicon photonics-based transceivers with 1-Tb/s capacity", IEEE TCPMT, 6 (7).

CHAOS TIME DOMAIN REFLECTOMETRY FOR DIAGNOSIS OF COMPLEX TOPOLOGY WIRED NETWORKS



RESEARCH TOPIC:

Defects, cables, reflectometry, chaos

AUTHORS:

F. Auzanneau, N. Ravott

ABSTRACT:

A new reflectometry-based wire diagnosis method, called Chaos Time-Domain Reflectometry (CTDR), using chaotic signals is investigated. It shows excellent potential for the diagnosis of live wires (i.e. during their operational usage) and complex topology networks. Chaotic signals, having very low auto-correlation sidelobes, have high performances in very noisy environments: the detection and location of defects are possible, even if several reflectometers inject their signals concurrently with the diagnosis and the normal operation of the cable. This enables the use of CTDR for distributed diagnosis of complex topology networks.

SCIENTIFIC COLLABORATIONS:

Context and Challenges

In many application domains, wire faults can have dramatic consequences. Live wire diagnosis is often required to ensure permanent monitoring of the health of embedded cables. Reflectometry methods are among the best methods for this purpose. Similarly to Radar, reflectometry injects a signal at one end of the network under test. This signal propagates along the cables and each impedance discontinuity (junction or defect) sends a part of its energy back to the injection port. The analysis of the measured signal provides information on the presence, the location and the type of these discontinuities. But these methods have limited performances in the case of noisy and branched networks. Chaotic signals present a very good potential for an improved diagnosis of noisy complex networks.

Main Results

Chaos theory describes systems whose behavior is highly dependent on initial conditions, and becomes very difficult to predict in time. Chaotic signals show very good auto-correlation and cross-correlation characteristics and the capacity of generating virtually an infinite number of orthogonal signals. This feature is exploited for the distributed diagnosis of complex topology networks.

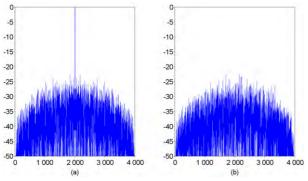


Fig. 1. Auto- and cross-correlation of 2 chaotic signals.

In CTDR, chaotic signals are generated with the joint use of the logistic and Bernoulli maps.

In a complex reflectogram, it is not easy to precisely locate a defect in the branches of the network: a single sensor cannot tell a defect from symmetric branches. To provide unambiguous defect location, one must add other sensors at other ends of the network (distributed diagnosis). However, to prevent a signal from one sensor from triggering a false alarm in another sensor, the signals from all the reflectometers must have cross-correlation levels lower than or similar to the noise level (Fig. 1).

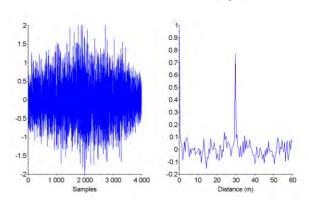


Fig. 2. Chaotic signal acquired and computed reflectogram in a very noisy network (SNR= -18dB)

Fig.2 shows that CTDR can detect and locate a defect 30 meters away from the reflectometer (right) in the case of a noisy network, where 10 other reflectometers inject their signals, although the defect's signal is 8 times lower than the measured one and cannot be recognized in the measurement (left). Experiments have confirmed the simulation results.

Perspectives

CTDR's capacity of increasing the number of possible reflectometry systems in the same network is a great advantage for Smart Grid application. A high number of sensors can be used without any interference, allowing unambiguous defect location even for a very complex branched topology.

RELATED PUBLICATIONS:

[1] F. Auzanneau, "Chaos time domain reflectometry for distributed diagnosis of complex topology wired networks," Electronics Letters., vol. 52, no. 4, pp. 280-281, 2016.

[3] F. Auzanneau, L. Incarbone, and N. Ravot, "Chaos time domain reflectometry for distributed diagnosis of complex topology wired networks," in IEEE Sensors Journal, vol. 16, no. 22, pp. 8027-8034, 2016.





MATHEMATICAL OPERATORS IMPLEMENTED USING SPIKING NEURAL NETWORKS – IMPACT OF SPIKE PROPAGATION ON RESULTS ACCURACY

RESEARCH TOPIC:

Signal processing, Spiking neural network

AUTHORS:

T. Mesquida, A. Valentian, D. Bol (Université Catholique de Louvain), E. Beigne

ABSTRACT:

Spiking neural networks are the third generation of neural networks. They are more biologically inspired than classical formal coding networks and are more computationally powerful as well as more power efficient. For fully exploiting spike coding at a system level, one may need to process signal from a sensor that generates spikes. That is why work is done on implementing a Signal Processing engine in a neural network. Spikes in a neural network are propagated thanks to an Address Event Representation (AER) scheme. The work presented here shows the impact of AER on mathematical operations accuracy.

SCIENTIFIC COLLABORATIONS: Université Catholique de Louvain, (Belgium)

Context and Challenges

Spiking neural networks are very promising for reducing the power dissipation of inference as well as learning tasks, compared to Formal Coding classical networks. This is due to the fact that a spike can convey more information (temporal coding), and induces less power consumption when processed (simple accumulation).

However, for truly taking benefit from spike coding, spikes must be considered at system-level: spikes must propagate all the way from the sensor to eventually the actuator. In that context, some preprocessing may be necessary at sensor level, before inference tasks. Thus mathematical operators must be implemented in spiking neural networks [1].

Main Results

The way spikes are propagated in a neural network is using an Address Event Representation (AER) scheme. Spikes are not propagated on single wires, but are time-multiplexed on a bus: the biological-scale connectivity is replaced by the serialization of events. As shown in Fig. 1, an AER event is based on the handshake asynchronous protocol and consists in sending the address of a spike.

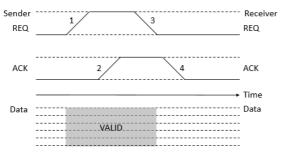


Fig. 1 - Illustration of the AER mechanism

However, a bus bandwidth is not infinite and collisions may occur between events. In such a case, a spike may arrive later than

expected. For estimating the impact on the calculation accuracy, several AER models have been considered. The two main models used in literature are M/M/1 and M/D/1: the first letter gives information on the inter-arrival time, the second one on the service time, and the last one is the number of servers. M/M/1 queues have Poisson process as input, i.e. inter-arrival time following an exponential distribution, and a service time following an exponential distribution. It is found that the output is still a Poisson distribution, so there is no impact for that model.

However, since the 4-phases AER handshake cannot be processed instantaneously, an M/D/1 queue is more representative. It has been found that an error occurs and is function of the occupancy rate and the integration time of spikes (see Fig. 2): it can increase up to 3.8% in the worst case.

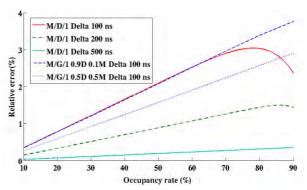


Fig. 2 - Error as function of the network occupancy rate

It means that attention must be paid when (1) spike coding strategies involve time constants close to network's mean service time and (2) the network is busy. This is obviously less of a problem for low power applications, for which the spike rate would be low.

Perspectives

This work lays down the foundations for a neuromorphic signal processing engine, dedicated to IOT application.

RELATED PUBLICATIONS:

[1] Thomas MESQUIDA, Alexandre VALENTIAN, David BOL, Edith BEIGNE, "Impact of the AER-Induced Timing Distortion on Spiking Neural Networks Implementing DSP," PRIME Conference, Lisbon, Portugal, June 2016

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7.

PHD DEGREES
AWARDED IN 2016



ASSIM BOUKHAYMA ULTRA LOW NOISE CMOS IMAGE SENSORS EPFL (Switzerland)

CMOS Image Sensors (CIS) overtook the charge coupled devices (CCDs) in low noise performance. Photoelectron counting capability is the next step for CIS for ultimate low light performance and new imaging paradigms. This work presents a review of CMOS image sensors based on pinned photo diodes (PPDs). The physical mechanisms behind the random fluctuations affecting the signal at different levels of conventional CIS readout chains are reviewed and clarified. This thesis dedicates a particular focus to the readout circuit noise given that it precludes photoelectron counting in conventional CIS. A detailed analytical calculation of the temporal read noise (TRN) in conventional CIS readout chain is presented. The latter suggests different noise reduction techniques at process and circuit design level. Among them, the increase of the oxide capacitance by using a thin oxide in-pixel amplifying transistor, for low 1/f noise, is

suggested for the first time. A test chip was designed in a 180 nm CIS process and embedding optimized readout chains exploiting the new pixels together with state-of-the-art 4T pixels. A mean input-referred noise of 0.4 e-rms has been measured. Compared with the stateof-the-art pixels, also present onto the test chip, the mean RMS noise is divided by more than 2. Next, a full VGA imager has been integrated in a standard CIS process. It relies on a 4T pixel of 6.5 µm pitch with a properly sized and biased thin oxide PMOS source follower. The sensor chip features an input-referred noise histogram from 0.25 e-rms to a few e-rms peaking at 0.48 e-rms. This sub-0.5 electron noise performance is obtained with a full well capacity of 6400 eand a frame rate that can go up to 80 fps. The VGA imager also features a fixed pattern noise as low as 0.77%, a lag of 0.1% and a dark current of 5.6 e-/s.



MATTHIEU VERDY

DEVELOPMENT OF TEST STRATEGIES FOR MILLIMETER-WAVE COMMUNICATIONS SYSTEMS

Université Grenoble Alpes (France)

The thesis' goal is to develop global test strategy in order to reduce test cost and ensure cover. OFDM communications will be a point of interest in this thesis. The investigation has to reach the circuit BIST implementation to release constraint over test environment. The test environment contains ATE and test interface. Our approach consists in using a standard ATE and implementing few components on test interface. BIST specification and modules of test interface must be precise and realistic in order to ensure the physical implementation. To reach these goal, we will first rely on models of different blocks and appropriate simulations to identify relevant test parameters. Secondly, we will produce test solution that ensure the measure of each relevant parameters. Relevant test parameters are parameters that allow to test the system quickly, with maximal test cover. These parameters can be computed using both functional model and structural model. Functional model is used to detect catastrophic faults, and structural model determines each blocks performance to improve efficiency. Dealing with structural test, individual block performances can be determined using BIST, or computing correlation between local blocks parameters and global system parameters (ie. EVM, or any relevant parameter).

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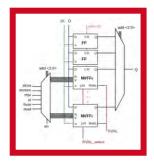
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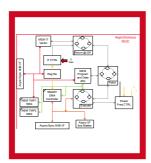
NATALIJA JOVANOVIC

ROBUST AND RELIABLE RERAM-BASED NON-VOLATILE SEQUENTIAL LOGIC CIRCUITS IN DEEPLY SCALED CMOS TECHNOLOGIES

Telecom ParisTech (France)

Non-volatile memories and flip-flops can improve the energy efficiency in batteryoperated devices by eliminating the sleep-mode consumption, while maintaining the system state. Among emerging embedded NVM technologies, ReRAM has a fast programming time, a simple CMOS-compatible structure and a good scalability. Previously proposed ReRAM based non-volatile flip-flops (NVFF) have been implemented in 90nm or older CMOS nodes and suffer from CMOS reliability issues in scaled nodes due to high programming and forming voltages. This thesis makes the analysis of robust and reliable non-volatile design in 28nm CMOS node and below. It presents two novel thin gate oxide CMOS design solutions for the programming of ReRAM devices. The programming circuits are applied in dual-voltage NVFF architecture which employs two ReRAM devices (2R). Alternative 1R NVFF architecture is proposed in order to

improve the area overhead and reduce the consumption. With regard to the existing ReRAM technologies, the proposed NVFF solutions are optimized for ReRAM programming conditions which improve endurance and minimize programming power. Statistical analysis of the FF core and its optimization was performed to evaluate the best restore operation architectures meeting digital CMOS circuit design yield requirements. The NVFFs are implemented in 28nm CMOS FDSOI and benchmarked against a master slave flipflop from a standard library and a data-retention flip-flop. Finally, non-volatile register file (NVRF) based on the 1R NVFF solution is proposed, for the design of NV MCU.



FLORENT BERTHIER

DESIGN OF AN ULTRA LOW POWER PROCESSOR FOR WIRELESS SENSOR NODES

Université de Rennes I (France)

This PhD work focuses on the reduction of energy consumption and wake up time reduction of a WSN node microcontroller through innovations at architectural, circuit and power management level. This work proposes a partitioned microcontroller architecture between a programmable wake up processor, named Wake-Up Controller on which this work is focused, and a main processor. The first deals with the common tasks of a wireless sensor node while the second manages the irregular tasks.

The Wake-Up Controller proposed in this work is a 16-bit RISC processor whose instruction set has been adapted to handle regular tasks of a sensor node. It only executes code on interruptions. It is implemented in asynchronous / synchronous mixed logic to improve wake up time and energy. A circuit was fabricated in a 28nm UTBB FDSOI technology integrating the Wake-Up Controller. The core reaches 11,9

MIPS for 125 μ W average power consumption in active phase and wakes up from sleep mode in 55ns from eight possible interruption sources. The static power consumption is around 4μ W for the asynchronous logic core at 0.6V without power gating and 500nW when gated.



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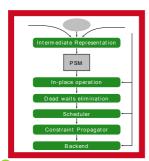
THIAGO RAUPP DA ROSA

COMMUNICATION SUPPORT IN MULTI-CORE
ARCHITECTURES THROUGH HARDWARE MECHANISMS
AND STANDARDIZED PROGRAMMING INTERFACES

Université Grenoble Alpes (France)

Developing embedded applications is becoming a key challenge, since applications workload will continue to grow and the software technologies are not evolving as fast as hardware architectures, leaving a gap in the full system design. Indeed, the increased programming complexity can be associated to the lack of software standards that supports heterogeneity, frequently leading to custom solutions. On the other hand, implementing a standard software solution for embedded systems might induce significant performance and memory usage overheads. Therefore, this Thesis focus on decreasing this gap by implementing hardware mechanisms in co-design with a standard programming interface for embedded systems. The main objectives are to increase programmability through the implementation of a standardized communication application programming interface (MCAPI), and decrease the overheads imposed by the software implementation through the use of the developed hardware mechanisms.

The contributions of the Thesis comprise the implementation of MCAPI for a generic multicore platform and dedicated hardware mechanisms to improve communication connection phase and overall performance of data transfer phase. It is demonstrated that the proposed mechanisms can be exploited by the software implementation without increasing software complexity. Furthermore, performance estimations obtained using a SystemC/TLM simulation model for the reference multi-core that architecture show the proposed mechanisms provide significant gains in terms of latency (up to 97%), throughput (40x increase) and network traffic (up to 68%) while reducing processor workload for both characterization test-cases and real application benchmarks.



IVAN LLOPARD

PROGRAMMING EMBEDDED MANYCORE: REFINEMENT AND OPTIMIZING COMPILATION OF A PARALLEL ACTION LANGUAGE FOR HIERARCHICAL STATE MACHINES

Université de Paris VI (France)

languages propose convenient Modeling abstractions and transformations to handle the complexity of today's embedded system design and implementation. Based on the formalism of Hierarchical State Machines, widely known as Statecharts, they enable the expression of control parallelism. However, they face two important challenges when it comes to model data-intensive applications on modern parallel architectures: no unified approach that also accounts for (data) parallel actions; and no effective model optimization and code generation flows. We propose a modeling language extended with parallel action semantics and indexed state machines suitable for computationally intensive applications. Together with its formal semantics, we present an optimizing model compiler aiming for the generation of efficient data-parallel implementations. Following the model-driven methodology, the compilation flow has been

successfully applied to many-core architectures such as GPGPU platforms.

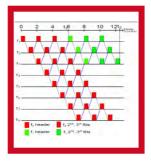
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LAURE ABDALLAH

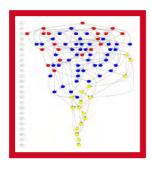
WORST-CASE DELAY ANALYSIS OF CORE-TO-IO FLOWS OVER MANY-CORES ARCHITECTURES

Université de Toulouse(France)

Many-core architectures are more promising than multicore for designing real-time systems as they should allow for an easier integration of a higher count of tasks with various level of criticalities. In embedded real-time systems, these architectures will generally be networked through Ethernet links. Thus, a number of applications of different level of criticalities could be allocated on the Network-on-Chip (NoC) and required to communicate with sensors and actuators. However, the worst case behavior of a NoC for both inter-core and core-to-Input/Output(I/O) communications is generally over estimated.

In this thesis, we show that the habitual pessimism of the existing Worst-Case Traversal Time (WCTT) computing methods and the existing mapping strategies lead to drop Ethernet frames due to an internal congestion in the NoC. Thus, we demonstrate properties of such NoC-based wormhole networks to reduce

the pessimism when modeling flows in contentions. We then propose a mapping strategy that minimizes the contention of coreto-I/O critical flows in order to solve this problem. We show that the pessimism can be reduced up to 50% compared to current stateof-the-art real-time packet schedulability analysis. These results are due to the modeling of the real impact of the flows in contention in our proposed computing method. Besides, experimental results on real avionics applications show significant improvements of core-to-I/O flows transmission delays, up to without significantly impacting 94% transmission delays of core-to-core flows. These improvements are due to our mapping strategy that allocates the applications in such a way to reduce the impact of non-critical flows on critical flows. These reductions on the WCTT of the core-to-I/O flows avoid the drop of Ethernet frames.



DANG PHUONG NGUYEN

IMPROVED COMPACT FORMULATIONS FOR A WIDE CLASS OF GRAPH PARTITIONING PROBLEMS IN SPARSE GRAPH

Université Paris 6 (France)

The graph partitioning problem is a fundamental problem in combinatorial optimization. The problem refers to partitioning the set of nodes of an edge weighted graph in several disjoint node subsets (or clusters), so that the sum of the weights of the edges whose end-nodes are in different clusters is minimized. In this thesis, we study the graph partitioning problem on graph with (non negative) node weights with additional set constraints on the clusters (GPP-SC) specifying that the total capacity (e.g. the total node weight, the total capacity over the edges having at least one end-node in the cluster) of each cluster should not exceed a specified limit (called capacity limit). This differs from the variants of graph partitioning problem most commonly addressed in the literature in that: 1) The number of clusters is not imposed (and is part of the solution), 2) The weights of the nodes are not homogeneous.

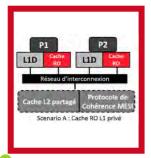
The subject of the present work is motivated by the task allocation problem in multicore structures.

The goal is to find a feasible placement of all tasks to processors while respecting their computing capacity and minimizing the total volume of inter-processor communication. This problem can be formulated as a graph partitioning problem under knapsack constraints (GPKC) on sparse graphs, a special case of GPP-SC. Moreover, in such applications, the case of uncertain node weights (weights correspond for example to task durations) has to be taken into account.

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GREGORY VAUMOURIN

HYBRID MEMORY HIERARCHY AND DYNAMIC DATA HANDLING IN EMBEDDED PARALLEL ARCHITECTURES

Université de Bordeaux (France)

The energy consumption of the memory system in modern architectures is a major issue for both embedded systems limited by their battery capacity and high performance computers limited by their Thermal Design Power specifications.

By introducing a classification information in the memory system we allow for a heterogeneous management of data specific to each kind of data During this thesis, we focused on the specific management of read-only data into the memory system through a compilation/architecture codesign.

This approach allows to explore new potentials in terms of data locality, scalability of the system or cache designs.

Evaluated by simulation with a multi-core architecture, the proposed solution offers a significant energy consumption reduction while keeping the performance stable



FABRICE MAYRAN DE CHAMISSO

LIFELONG EXPLORATORY NAVIGATION: INTEGRATING PLANNING, NAVIGATION AND SLAM FOR AUTONOMOUS MOBILE ROBOTS WITH FINITE RESOURCES

Université Paris-Saclay (France)

One of the yet unresolved canonical problems of robotics is to have robots move completely autonomously in order to accomplish any mission they are charged with, with time and resource constraints and without prior knowledge of the environment.

Reaching a goal requires the robot to perform at least four tasks: maintaining an abstract representation of the environment (map), being able to localize itself within this representation, using the representation to plan paths and navigating on the planned paths while handling dynamics of the environment and avoiding obstacles.

Each of these problems has been studied extensively by the robotics community. However, the four components are usually studied separately, and as a result are mostly incompatible with each other. Additionally, since humans as well as robots have to operate with finite memory and computing resources, long

running planning, navigation and SLAM algorithms may have to operate on incomplete or compressed data while guaranteeing that the goal(s) can still be reached.

In this thesis, planning, navigation and SLAM in arbitrarily large environments with finite computing resources and memory are considered as one single problem, for a new bio-inspired paradigm which we call Lifelong Exploratory Navigation.

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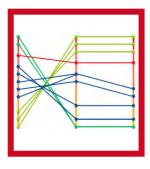
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XUAN KHANH DO

A MODEL OF PROGRAMMING LANGUAGES FOR DYNAMIC REAL-TIME STREAMING APPLICATIONS

Université Paris 6 (France)

There is an increasing interest in developing applications on homo- and heterogeneous multiprocessor platforms due to their broad availability and the appearance of many-core chips. Given the scale of these new massively parallel systems, programming languages based on the dataflow model of computation have strong assets in the race for productivity and scalability, meeting the requirements in terms of parallelism, functional determinism, temporal and spatial data reuse in these systems. However, new complex signal and media processing applications often display several major challenges that do not fit the classical static restrictions.

To tackle those restrictions, we propose and evaluate an analytical scheduling framework that bridges classical dataflow models of computation and real-time task models. In this framework, we introduce a new scheduling policy noted Self-Timed Periodic (STP), which is

an execution model combining Self-Timed scheduling (STS), considered as the most appropriate for streaming applications modeled as data-flow graphs, with periodic scheduling: STS improves the performance metrics of the programs, while the periodic model captures the timing aspects. We evaluate the performance of our scheduling policy for a set of 10 real-life streaming applications and find that in most of the cases, our approach gives a significant improvement in latency compared to the Strictly Periodic Schedule (SPS), and competes well with STS. Our experiments also show that, for more than 90% of the benchmarks.

We also introduce a new dynamic Model of Computation called Transaction Parameterized Dataflow (TPDF). We demonstrate that TPDF can be used to accurately model task timing requirements in a great variety of situations and can easily be mapped to massively parallel embedded platforms.

ACKNOWLEDGEMENTS

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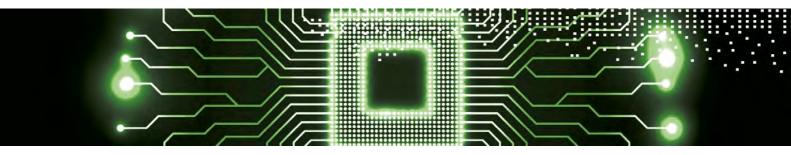
Thierry Collette

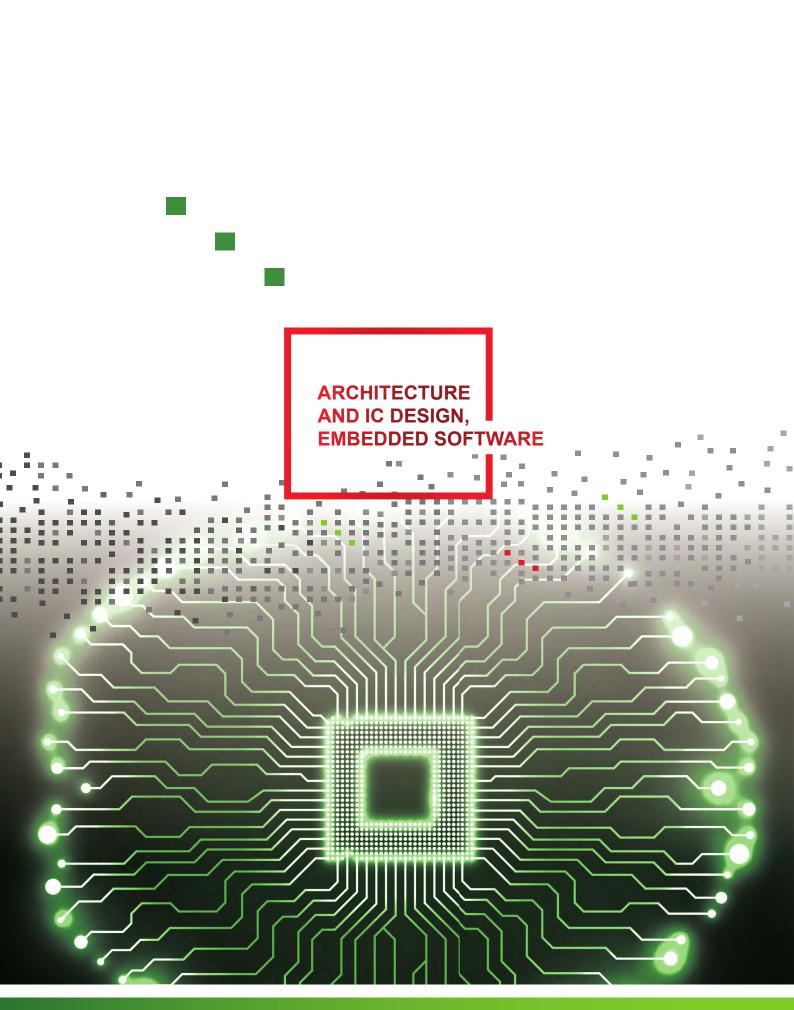
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