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TECHNOLOGY
RESEARCH
INSTITUTE

OPTICS
AND PHOTONICS

TECHNOLOGY RESEARCH INSTITUTE

LETI AT A GLANCE

Founded in **1967**

Based in **France** (Grenoble) with offices in **USA** (Silicon Valley) and **Japan** (Tokyo)

330 industrial partners

1,900 researchers

Committed to innovation, Leti's teams create **differentiating solutions in miniaturization and energy-efficient technologies** for its industrial partners.

Leti is a technology research institute at CEA Tech and a recognized global leader focused on miniaturization technologies enabling energy-efficient and secure IoT. Leti delivers solid expertise throughout the entire IoT chain, from sensors to data processing and computing solutions. Leti pioneered FDSOI low power platform for IoT, M&NEMS technology for low cost multisensors solutions, CoolCube™ integration for highly connected and cost effective devices.

Leti's mission is to pioneer new technologies, enabling innovative solutions to ensure Leti's industrial partners competitiveness while creating a better future. It tackles most current global issues such as the future of industry, clean and safe energies, health and wellness, sustainable transport, information and communication technologies, space exploration and safety & security.

For 50 years, the institute has built long-term relationships with its partners: global industrial companies, SMEs and startups. It tailors innovative and differentiating solutions that strengthen their competitiveness and contribute to creating new jobs. Leti and its partners work together through bilateral projects, joint laboratories and collaborative research programs. Leti actively contributes to the creation of startups through its startup program.

Leti has signed partnerships with major research technology organizations and academic institutions. It is a member of the Carnot Institutes network*.

*Carnot Institutes network: French network of 34 institutes serving innovation in industry.

2,760 patents in portfolio

60 startups created

€315 million budget

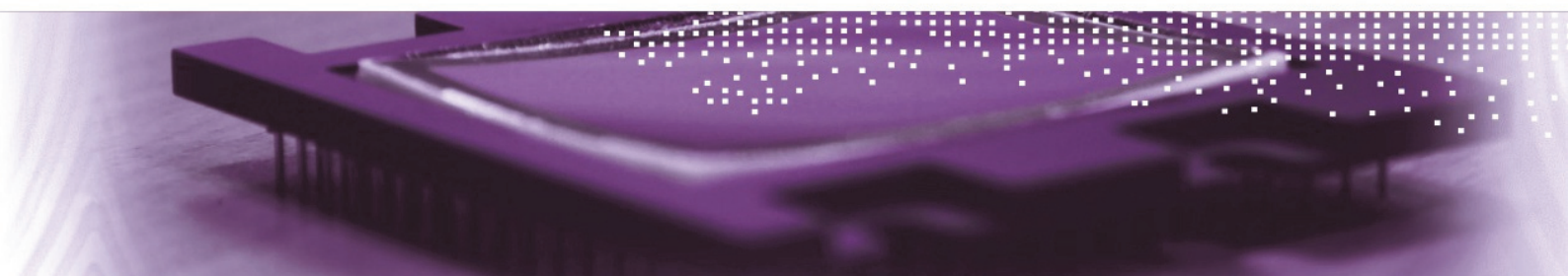**700** publications each year

ISO 9001 certified since 2000

Within CEA Tech and Leti, Optics and Photonics activities are focused principally on big industrial markets of photonics: all-wavelength imaging (visible, infrared, THz), information displays, solid state lighting, optical data communications, optical environmental sensors.

The R&D projects are performed with industrial and academic partners. The industrial partners of the Optics and Photonics division range from SME to large international companies. The projects are merging fundamental aspects with advanced technological and industrial developments; nanosciences are connected with material sciences, optics, electronics and micro & nano-fabrication.
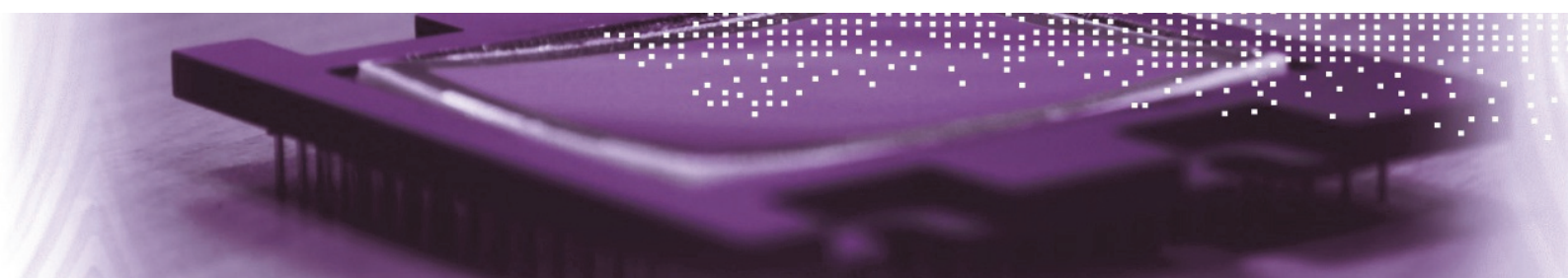
OPTICS AND PHOTONICS

Picture on the cover page: prototype of a visible image sensor (30x37x0.1mm) with a spherical radius of curvature of 150mm

CONTENTS

EDITO

Ludovic POUPINET
HEAD OF OPTICS AND PHOTONICS DIVISION

Optics and Photonics Division (DOPT) of Leti fosters employment in France and Europe by developing innovative photonic components. We see miniaturization and integration as the main driving factors to reach this target. We help our industrial partners to decrease the cost, to improve the performances and to diversify the functionalities of their products.

DOPT is focused on various topics such as visible, infrared and THz imaging sensors as well as integrated photonic components, optical gas sensors and light emitting arrays both for displays and smart lighting. In each area, DOPT, with its 300 staff members, concentrates long-term expertise, up-to-date clean rooms and equipment and dedicated characterization benches. 90% of our funding is obtained through one-to-one or collaborative projects, both with academic and industrial partners. The high quality of our partners is also our strength.

To stay at the leading edge of applied photonic research requires a deep understanding of product and application needs in terms of performance, cost and functions, as well as an ability to introduce new concepts in our process flows. Infrared high performance avalanche photodiodes, metamodeling, topological insulators, THz imaging toolbox, GeSn integrated lasers, large-scale photonic circuits and ultra-high resolute GaN micro-displays are among the exciting topics detailed in this report.

I hope that reading this report will make you want to know more about us, meet us during conferences, professional forums or Leti events, join us as a researcher, a PhD or a post-doctoral fellow and, of course, build fruitful collaborations on exciting research topics tackling the microscopic behavior of photons using state-of-the-art industry compatible facilities.
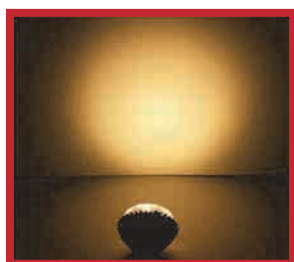
Happy reading!

Ludovic Poupinet
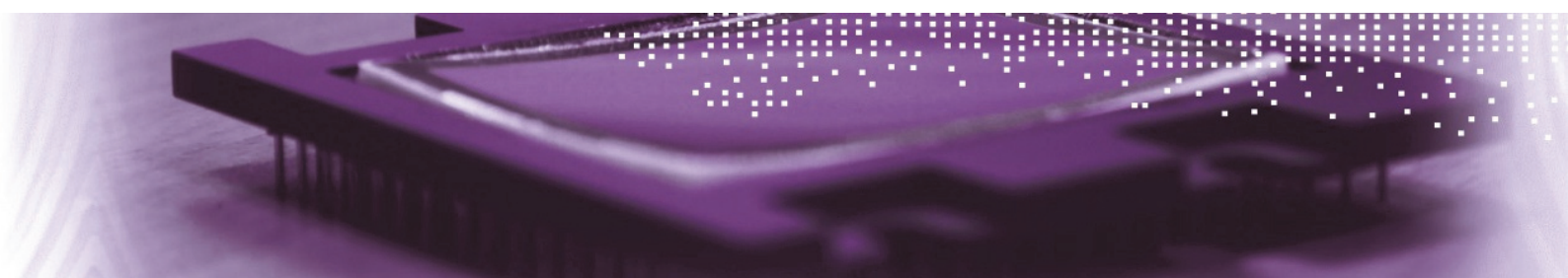
KEY FIGURES

210 permanent researchers
30 PhD students and Post-docs
45 CEA experts: with 4 directors of research
and 2 international experts

160 publications in 2016 including 55 papers in peer reviewed journals

75 patents filed in 2016
450 patents portfolio with about
20% under license

Dedicated clean rooms for III-V and II-VI materials on versatile substrate geometries up to 150 mm
Access to Leti clean rooms in 200 and 300 mm through numerous photonic processes and technology modules
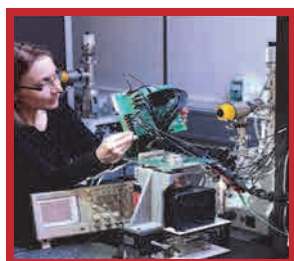
Optics and opto-electronics characterization facilities

Advanced means of modeling and simulation
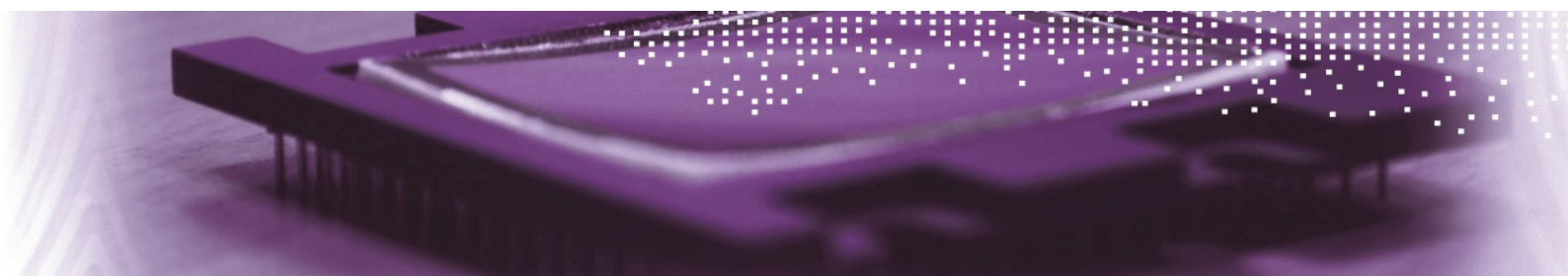
SCIENTIFIC ACTIVITY

Awards

François TEMPLIER received a "best paper award" at the International Display Workshops IDW'2016, for a new approach for fabricating high-rightness GaN LED microdisplays with very small pixel-pitch

François OLIVIER received a "best poster award" at the Euro MRS 2016 conference for the study of the influence of size-reduction on the performances of GaN-based micro-LEDs display

Candice THOMAS received a "best student paper award" at the 19th Int. Conf. on Molecular Beam Epitaxy (MBE'2016) for "Revealing Dirac fermions in strained three‐dimensional HgTe topological insulators via Quantum Hall spectroscopy".

Olivier CASTANY received a "best paper award" at 6th Electronics System-Integration Technology Conference (IEEE, ESTC - 2016) for the packaging of high speed 100 Gbps silicon photonic photoreceiver module

Conference and workshop organization

Pierre CASTELEIN at the conference OPTRO 2016 (Paris, France)

Tony MAINDRON at the RAFALD workshop on "Atomic Layer Deposition (ALD) techniques" (Chatou, France)

Sylvie MENEZO at two Silicon Photonics conferences: "Optical Fiber Communication" (OFC-Los Angeles, USA) and the "European Conference on Optical Communication" (ECOC - Düsseldorf, Germany)

Book

François TEMPLIER : chapter of the book "La lumière en lumière" published by EDP Sciences

1.
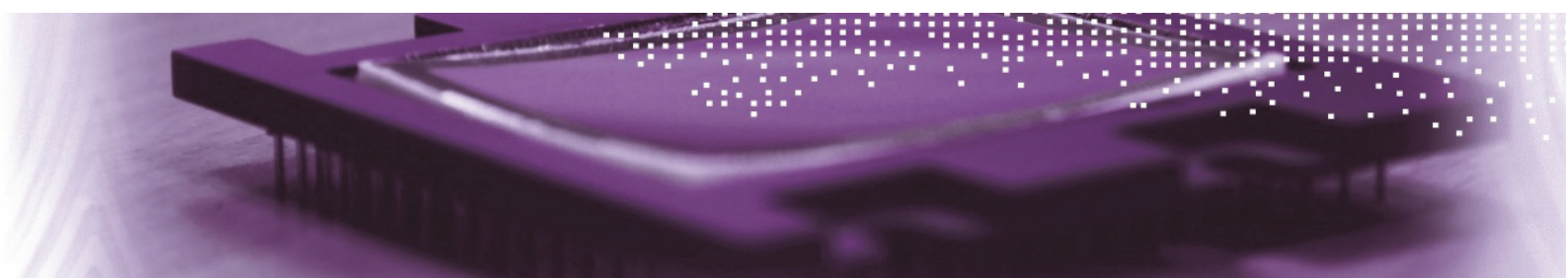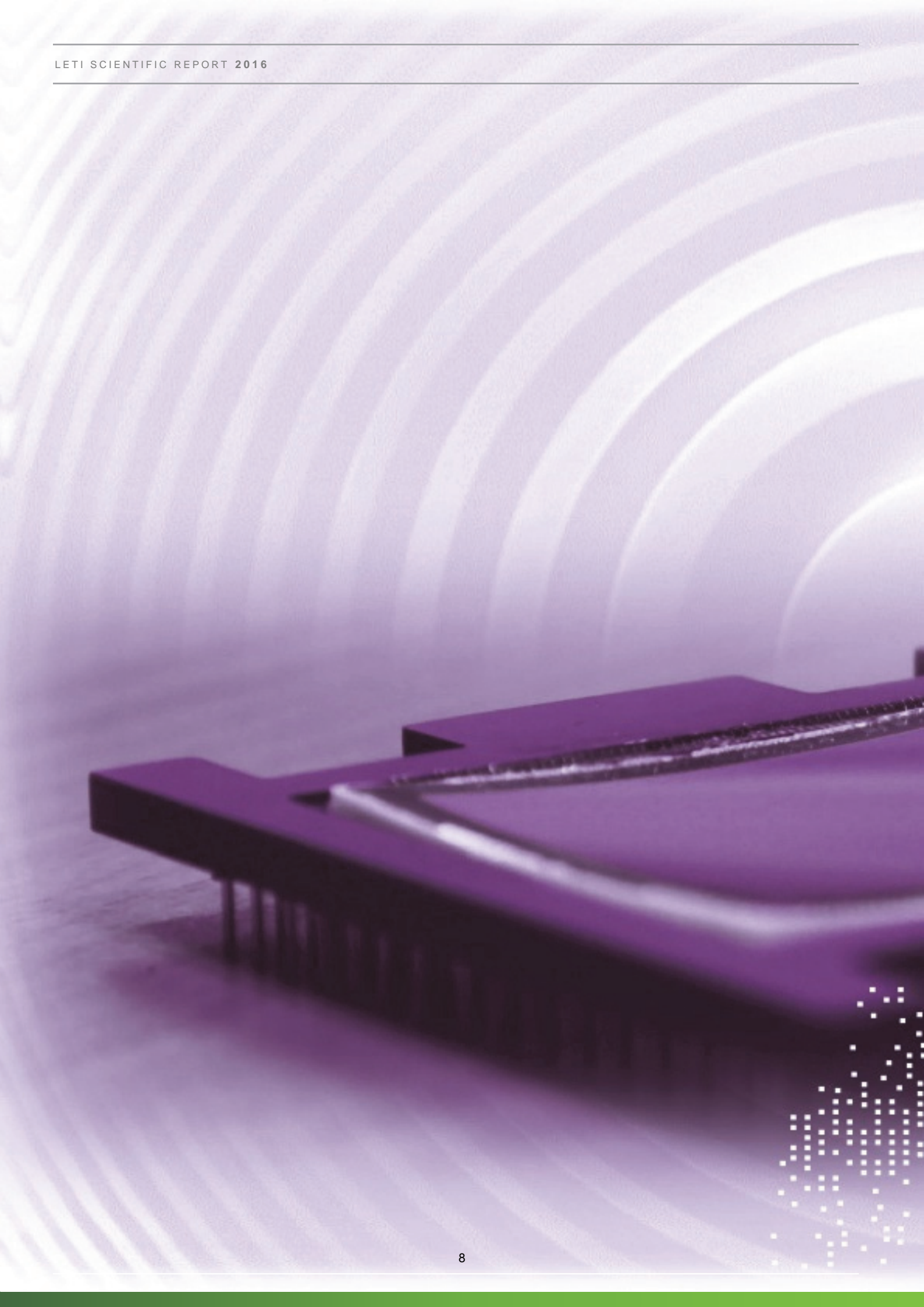
INFRARED IMAGING
COOLED HgCdTe DETECTORS

- Space and science imaging
- Low dark current detectors
- Avalanche HgCdTe photodiodes (APD)
- Frequency selective surfaces
- Multi-color infrared imaging
- Small pitch, hybridization

HgCdTe DETECTORS FOR SPACE AND SCIENCE IMAGING

AUTHORS:
O GRAVRAND, C CERVERA, J ROTHMAN, N BAIER, E DE BORNIOL, C LOBRE, J L SANTAILLER, G BADANO

ABSTRACT:
HgCdTe (MCT) has always been a material of choice for IR imaging from space. For several decades, LETI has been at the cutting edge of such technologies. For instance, the Cassini probe, today orbiting Saturn makes use of a LW MCT detector fabricated at LETI in the late 90's. Later, first VLWIR MCT arrays (20µm cutoff) has been demonstrated at LETI, giving rise to the MTG program where all MCT arrays are delivered by Sofradir (former spinoff from LETI). During the last few years, a strong effort has been dedicated to the optimization of such arrays for ultimate performances. Thanks to ESA and CNES funding, various cutoff wavelengths has been investigated, from VLWIR (15µm co) for meteorology, to LW and MW low flux arrays for exoplanet exploration and SWIR large arrays for general astrophysics needs. The focus was the assessment of very low dark currents and high quantum efficiencies.

SCIENTIFIC COLLABORATIONS: CEA-IRFU, GIF SUR YVETTTE, FRANCE, IPAG (CNRS/Université Grenoble Alpes, France, Centre National d'Etudes Spatiales (CNES) and the European Space Agency (ESA)

Large SWIR Arrays for astronomy

Astronomy observations require very large arrays (at least 2k x 2k with 15µm pitch) with ultra-low dark currents (below 0.1 e/s/pixel) and high quantum efficiencies (QE>80%). Since 2011, a strong effort has been dedicated to the demonstration of such devices at LETI and IRFU [1]. Fig 1 shows a gathering of measured dark currents on 15µm pitch low flux ROIC. Different configurations have been investigated, including different material growth (MBE or LPE), different diode structures (n/p, p/n, APD) or different doping levels. At the end, sub e/s/pixel has been demonstrated at temperatures below 150K, while keeping QE higher than 80% [2] [4]. Measurements are now limited by ROIC glow (electroluminescence from the Si ROIC, usually around 1e/s/px) and further work about this subject is ongoing within a large ESA program aiming at producing the first 2k x 2k european array for astronomy needs.
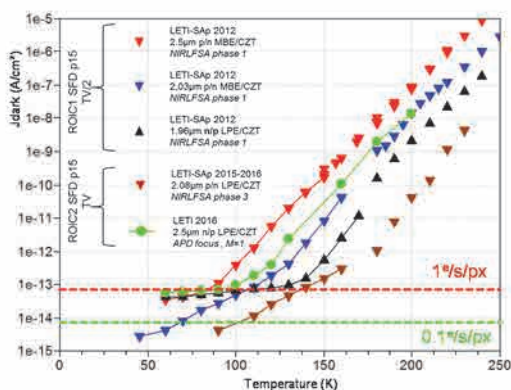

Figure 1: Dark current data for SWIR p/n and n/p arrays (2.08 data is corrected from ROIC glow)

Recently, further work has been carried out at LETI in order to investigate the use of MCT APDs for astronomy needs. [3]. We demonstrated that APDs (Green dots on fig1) may be suitable for low flux imaging at low temperature. The use of avalanche gain may however slightly degrade the dark current by typically one order of magnitude.

MW-LW-VLW arrays for exoplanet or earth observation

Going to longer cutoff arrays leads to much smaller gap absorbing material. As a consequence, dark currents are usually much higher due to diffusion from the absorbing layer, but also depletion related dark current and last but not least surface leakage currents. Once again, different configurations in terms of diode polarity and technological parameters have been investigated [2] [4] using 30µm pitch CTIA ROIC. 100 e/s/pixel has thus been demonstrated for LW p/n arrays (green dots for 12.3 µm co at 40K). Other investigated n/p devices showed a 1000 e/s/pixel limitation, independent from the cut-off. This effect is not yet understood but may be attributed to a potential experimental limitation.

Last but not least, VLWIR p/n arrays have been also investigated, up to 17.1 µm cutoff at 80K. Dark current remained diffusion limited down to 50 to 45K, with close to perfect noise histograms [2].
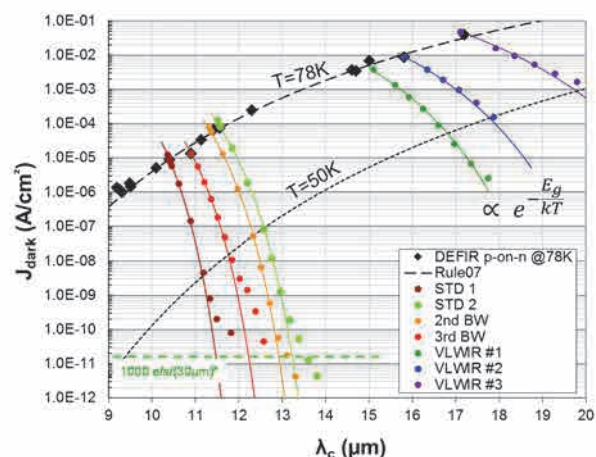
Figure 2: LW p/n dark currents measured for different temperatures and cutoffs.

RELATED PUBLICATIONS:
[1] O. Gravrand, L. Mollard, O. Boulade, V. Moreau, E. Sanson, and G. Destefanis, "Ultralow-Dark-Current CdHgTe FPAs in the SWIR Range at CEA and Sofradir," J. Electron. Mater., vol. 41, no. 10, pp. 2686–2693, Aug. 2012.
[2] O. Gravrand, J. Rothman, C. Cervera, N. Baier, C. Lobre, J. P. Zanatta, O. Boulade, V. Moreau, and B. Fieque, "HgCdTe Detectors for Space and Science Imaging : General Issues and Latest Achievements," J. Electron. Mater., vol. 45, no. 9, pp. 4532–4541, 2016.191W, 2016.
[3] [1] J. Rothman, E. de Borniol, O. Gravrand, P. Kern, P. Feautrier, J.-B. Le Bouquin, and O. Boulade, "MCT APD focal plane arrays for astronomy at CEA-LETI," SPIE, vol. 9915, p. 99150B, 2016.
[4] O. Boulade, V. Moreau, P. Mulet, O. Gravrand, C. Cervera, J.-P. Zanatta, P. Castelein, F. Guellec, B. Fièque, P. Chorier, and J. Roumegoux, "Development activities on NIR large format MCT detectors for astrophysics and space science at CEA and SOFRADIR," SPIE, vol. 9915, no. 0, p. 99150C, 2016.

DARK CURRENT LIMITATIONS IN HGCDTE APDS FOR ASTRONOMY AND SPACE APPLICATIONS

AUTHORS:

J. ROTHMAN, E. DE BORNIOL, C LARGERON, S GOUT, L MATHIEU and O. BOULADE[1]

ABSTRACT:

The dark-current limitations in HgCdTe avalanche photo diodes (APDs) with different Cd compositions and cut-off wavelengths have been characterized using read-out integrated circuits (ROICs) adapted for low flux and low photon number detection. The measurements showed that the dark current in the APDs follows a general trend when reported as a function of an effective temperature $\lambda_c T$. Dark currents at the level of the experimental limit, down to 1 e/s, and compatible with most low flux application is observed at low effective temperature, although additional cooling is required to compensate a 10 fold increase in dark current generation at high avalanche gains. At high temperatures, the dark current is independent on gain and compatible with ambient operating temperature in application with short observation times, such a free space telecommunications.

SCIENTIFIC COLLABORATIONS: [1] CEA-IRFU, GIF SUR YVETTTE, FRANCE, IPAG (CNRS/Université Grenoble Alpes,

HgCdTe APDs offers a unique means to detect a low number of photons that arrives on a photodetector during a time of observation. This enables to improve the sensitivity, down to single photon detection limit, in a wide range of applications ranging from high speed telecommunications to low flux astrophysical observation. In all applications it is ultimately the dark current that limits the sensitive of the detectors. To enable the highest possible gain, the dark current needs to be considerably lower than the lowest flux expected in each application. Extensive characterization of this limitation have been made in HgCdTe APDs with variable Cd composition and cut-off wavelengths (λ_c), hybridized on ROICs designed for low flux and low photon number detection in astronomy. The aim of the measurements were to explore the current limitations in dark current and prospective use of the HgCdTe APDs made at CEA/Leti and to identify paths for improvements through a deeper insight into the limiting phenomena.

The dark current was measured on HgCdTe APDs with cut-off wavelengths ranging from λ_c=2.54 to 3.7 µm hybridized onto two ROICs with low read-out noise, designed to detect a low number of photon during each integration time [1]. The ROIC termed RAPID was designed at Sofradir for fast frame rate applications such as wave front correction and fringe tracking and is characterized by a noise of 40 electrons rms at unity gain. The CL103 ROIC was designed at LETI for low flux imagery and is characterized by a noise of 11 electrons using double correlated sampling (CDS). The lowest dark current that could be detected were limited by the photoemission from the ROIC at a level of 1 e/s and 60 e/s for the CL103 and RAPID ROICs, respectively.

Figure 1 reports the dark current density as a function of inverse cut-off wavelength normalized temperature ($1/T\lambda_c$) with and without gain. In both cases, the variation of the dark current density is found to follow an approximate phenomenological law independently of the cut off wavelength. At a low effective temperature, below 2 (K.mm)-1, the dark current is found to be a factor 10 larger than the one for unity gain. In this regime, the dark current is limited by generation in the multiplication layer and the observed increase corresponds to an enhanced generation due to a reduced lifetime and/or the inclusion of new defects into the multiplication layer due to the extension of the space charge region at high reverse bias.

At the low effective temperatures, the reduction in dark current saturates at the level of the ROIC glow. This indicates that the dark current in HgCdTe APDs should be compatible with low flux applications that require a dark current below 1 electrons/s. However, the operating temperature to obtain this level need to be lower than the one in detectors with unity gain.

In the high temperature region, the dark current is limited by the amplified diffusion current and the dark current with or without gain is equal. In this regime, the measurement shows that the dark current at 300 K in a 15 µm diameter APD with λ_c=2.8 µm should be below 10 nA. Such an APD can be used in applications with high temporal resolution such as free space telecommunication at 10 Gb/s at gains in excess of 100.

Finally, the dark current measurement have been used to refine the calibration of a model, see figure 1, that is used to predict the dark current limited sensitivity in APD detectors as a function of operating temperature, size and Cd composition.
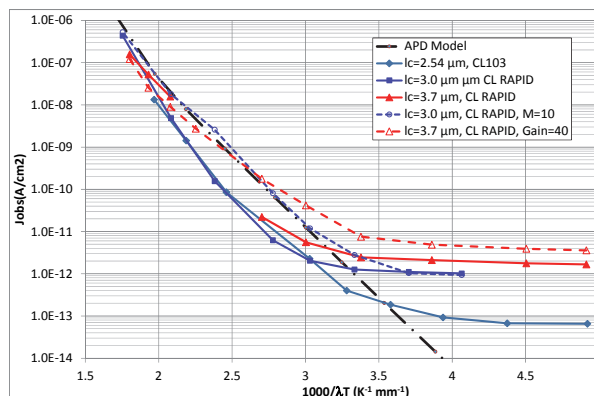

Figure 1: Measured and modelled dark current densities in HgCdTe APDs as a function of inverse normalized temperature [1].

The results shows on the potential use of HgCdTe APDs for low flux application at low operating temperatures with a read-out noise that will be close single photon sensitivity. An increase in operating temperature can be obtained from a reduction of defects in the multiplication layer and/or their contribution to the dark current. Such development should be associated with a further development of ROICs to reduce the glow and to increase reverse bias and gain of the APDs. In addition, an optimization of the APD bandwidth to 10 GHz will enable telecom applications at ambient operating temperature.

RELATED PUBLICATIONS:

1] J. Rothman, E. De Borniol, O. Gravrand, P. Kern, P. Feautrier, , J.-B. Lebouquin and O. Boulade, "MCT APD focal plane arrays for astronomy at CEA-LETI", Proc. SPIE, vol.9915, pp. 99150B

MICRO-DIFFRACTION INVESTIGATION OF LOCALIZED STRAIN IN MESA-ETCHED HGCDTE PHOTODIODES

AUTHORS:
A. TUAZ, P. BALLET, X. BIQUARD[1], and F. RIEUTORD[1]

ABSTRACT:
We present an X-ray micro-diffraction investigation of localized strain and lattice disorientation in HgCdTe layers with a submicronic resolution using a synchrotron white beam in Laue configuration. Diffraction peak displacement mapping evidences bending of the crystal planes around mesa-etched photodiodes, with strong dependence upon the processing steps. It is shown that the passivation step leads to sufficient strain for plastic deformation to occur at the lateral edges of the etching.

SCIENTIFIC COLLABORATIONS:[1] CEA-INAC: Institute for Nanosciences and Cryogenics, Grenoble, France

Context and Challenges

Within the general goal of reaching high operating temperatures while maintaining strong requirements on infrared photodetector performance, the pressure on HgCdTe material quality is increasingly growing. In particular, careful attention is now being paid to strain and strain relaxation within HgCdTe photodiodes. While recent studies [1] have focused on the lattice mismatch induced strain over areas of sizes of the order of the wafer, no experimental investigation has been able to resolve the strain at the pixel level, i.e. with a sub-micrometer spatial resolution. In particular, the effects of the main processing steps such as trench etching and surface passivation, on strain generation and lattice relaxation need to be investigated.

Main Results

The typical millimetric spatial resolution limit of standard diffraction can be overtaken using a focused synchrotron X-ray white beam. Indeed, by performing submicronic Laue diffraction measurements, we can map with a sub-micrometer resolution both the local deviatoric strain and the local lattice orientation. We have conducted Laue experiments with a 300nm diameter white beam probe using the micro-diffraction setup of the French CRG beamline BM32 at the European Synchrotron Radiation Facility (ESRF), see fig.1.
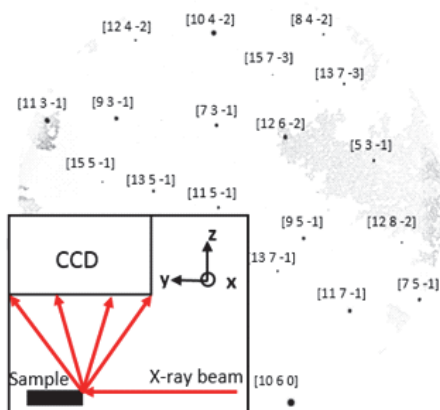

Figure 1: Cross-section Laue diffraction image of the HgCdTe layer, with corresponding [hkl] peak indexing. The inset represents the scheme of the measurement geometry

Samples consist in an Hg1-xCdxTe layer, with 30% cadmium fraction, deposited on a (111)B CdZnTe substrate by liquid phase epitaxy. Trenches were etched while adjusting depth to keep a 2.5µm thick layer under the etched area. To perform complete mesh scan around trench, we successively record 0.5µm horizontally spaced vertical lines from the surface of the layer, down to a few microns in the substrate with a 0.5µm spacing (see Fig. 2.a). As seen in Fig. 2.b, a sample without passivation does not show any evidence of peak displacement.

Thus, the etching process by itself does not induce any deformation field inside the material. On the contrary, the study of the peak displacement after the passivation process (Fig. 2.c-d) reveals the same pattern for all samples: the edges of the trenches are tilted.
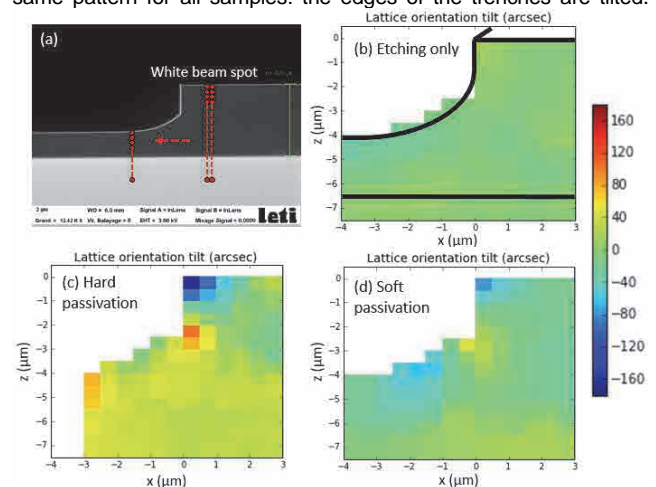

Figure 2: Sample X-section mapping showing the average lateral displacement of all diffraction peaks, as equivalent to lattice orientation tilt. Associated strain is clearly visible and localized all around the etching. The samples have undergone different processes: no passivation (b), hard and soft passivation (c) and (d). A SEM image of the mapping measurement is shown on (a).

The samples of Fig. 2.c-d represent two variations in the passivation deposition parameters to a hard (Fig. 2.c) and a soft (Fig. 2.d) passivation. There is a clear decrease in the overall tilt in the soft passivation case compared to the hard one, by approximately a factor of 2. This evidences the crucial role of the passivation process parameters on the deformation of the material and the ability of this micro-diffraction technique to resolve strain at a submicronic level thus revealing localized strain fields associated to photodetector fabrication [2]. Furthermore, a careful analysis of the diffraction peak shape at the trench corner (at maximum deformation) reveals that the material locally undergo plastic relaxation in the case of the hard passivated sample.

Perspectives

Clearly, the study on the peak displacement has highlighted the local lattice orientation tilt induced by the combination of etching and passivation. To go beyond, we need to quantitatively link this local tilt to the local strain inside the layer. As strain determination implies measurement of the relative peak movement one from another - not an average displacement -, and because expected strain value are below 5.10^{-4}, the evolution of the relative position of each peaks must be measured very accurately and any drifts must be precisely accounted for. Other important IR-detector fabrication steps would be included in this analysis such as annealing, ion implantation and metallization which are likely to induce localized strain fields inside the HgCdTe photodiodes.

RELATED PUBLICATIONS:
[1] P. Ballet, X. Baudry, B. Polge, D. Brellier, J. Merlin, and P. Gergaud, "Strain Determination in Quasi-Lattice-Matched LWIR HgCdTe/CdZnTe Layers" J. Electron. Mater. 42, 3133 (2013)
[2] A. Tuaz, P. Ballet, X. Biquard, and F. Rieutord, "Micro-diffraction investigation of localized strain in mesa-etched HgCdTe photodiodes" To appear in J. Electron. Mater. 2017.

THIN FILM CHALLENGES FOR HIGH PERFORMANCE IR PLASMON ENHANCED PHOTODIODES

AUTHORS:

F. BOULARD, O. GRAVRAND, L. ADELMINI, D. FOWLER, G. BADANO, P. BALLET, M. DUPERRON, S. BOUTAMI, and R. ESPIAU DE LAMAESTRE

ABSTRACT:

For several decades, Surface Plasmons (SP) have been increasingly studied for applications in many fields from chemistry, biology, to materials science. The IR sensor community has long recognized the interest of SPs to concentrate and channel light to increase sensitivity or modify spectral response. However, the incorporation of metallic nanostructures in technologically mature components is challenging. We report on the design and integration of a sub-wavelength photonic structure to add spectral functionalities to mid wave infrared HgCdTe photodiodes. Based on simulation and experimental results, tradeoffs to reach the full potential of SP enhancement are discussed.

Context and Challenges

The next generation of cooled infrared (IR) Focal Plane Arrays (FPA) will operate at higher temperature and provide spectral sensitivity [1]. While III-V materials exhibit promising properties, II-VI alloy such as HgCdTe is still the material of choice due to its large absorption coefficient leading to high quantum efficiency, very long minority carrier lifetime offering state-of-the art dark-current density, and tunable bandgap providing spectral agility. Metal/dielectric nano-patterning allows incident light to couple to surface plasmons. It offers an opportunity to spatially and spectrally concentrate the electric field. Embedded in an IR photodiode, it could offer a technological breakthrough to answer next generation needs. It was shown by numerical simulation that a well suited resonator design makes multicolor detection achievable [2]. In this paper, we discuss challenges to integrate such plasmonic resonator into the HgCdTe photodiode [3].

Main Results

An HgCdTe absorber layer is typically 3 to 10 μm thick. Thanks to the strong electric field enhancement allowed by plasmonic confinement, an ultrathin HgCdTe layer can be used to decrease the dark current while maintaining high quantum efficiency. The HgCdTe bandgap strongly depends on the Cd alloy fraction. Figure 1 (a) shows 3 SIMS Cd composition depth profiles, measured on 60 nm thick HgCdTe layers. In order to reach the Cd fraction of 0.3 needed to address MWIR detection in ultrathin layers, original growth strategy were developed, such as growing layers of shifted alloy composition (to compensate for Cd diffusion) and recalibrating the annealing temperatures and profiles. The thinness of the absorber leads to a surface-to-volume ratio close to that of a sheet of paper. However, no reduction of the minority carrier diffusion length have been measured compared to standard devices, illustrating the quality of surface passivation. Low-loss metals such as gold, copper or silver are suitable to excite plasmonic resonances in the IR. However, these elements act as acceptors in HgCdTe. So, their integration in the immediate vicinity of the absorber layer is forbidden. To solve that issue, a diffusion barrier layer has been implemented. Figure 1 (b) shows the measured quantum efficiency of two MWIR devices functionalized with four-color plasmonic resonators.
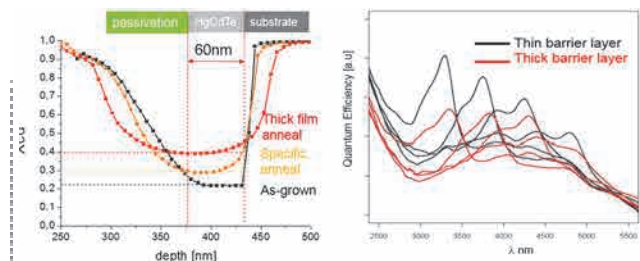

Figure 1: Cd fraction SIMS depth profile on as-grown and annealed ultrathin HgCdTe layers (a); Spectral response of 4 colors MWIR HgCdTe plasmon enhanced photodiode (b)

Resonance wavelength and shape depend mainly on resonator design and dimensions. Figure 1 measurements illustrate the impact of the diffusion barrier layer thickness on the peak intensity. Such dependence, correctly predicted by simulation (not shown), proves the strong impact of that parameter on electro-optical performances. These technological results have been successfully integrated on a 4 color 60 μm pixel pitch FPA [4].
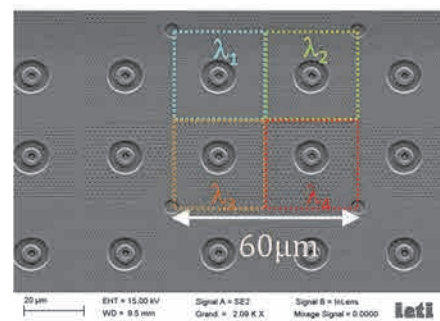

Figure 2: SEM image of 4 colors plasmon resonators embedded in HgCdTe photodiodes.

Perspectives

A sub-wavelength photonic structure was successfully processed on HgCdTe, a technologically very demanding material, proving LETI's know-how and technical maturity. The implementation of optical functions directly on HgCdTe becomes a concrete possibility.

RELATED PUBLICATIONS:

[1] O. Gravand, G.Destefanis, S. Bisotto, N. Baier, J. Rothman, L. Mollard, D. Brellier, L. Rubaldo, A. Kerlain, V. Destefanis, and M. Vuillermet, " Issues in HgCdTe research and expected progress in infrared detector fabrication," J. Electron. Mater., 42 (11), 3349-58, 2013

[2] D. Fowler, S. Boutami, M. Duperron, G. Moille, G. Badano, F. Boulard, J. Rothman, O. Gravrand, and R. Espiau de Lamaestre, "Partially localized hybrid surface plasmon mode for thin-film semiconductor infrared photodetection," Optics Letters, 38(3), 254-6, 2013.

[3] F. Boulard, O. Gravrand, L. Adelmini, D. Fowler, G. Badano, P. Ballet, M. Duperron, S. Boutami, and R. Espiau de Lamaestre, " Thin film challenges for hih performances IR plasmon enhanced photodiodes: from simulation to FPA integration and characterization," 63rd American Vacuum Society, invited talk, 2016.

[4] F. Boulard, O. Gravrand, L. Adelmini, D. Fowler, G. Badano, P. Ballet, M. Duperron, R. Esppiau de Lamaestre, " Sub-wavelength photonic structure to add spectral capabilites to MWIR HgCdTe photodiode, " Optics and Photonics Annual Research Report, 2014.

FREQUENCY SELECTIVE SURFACES FOR MULTICOLOR INFRARED IMAGING

AUTHORS:
E. LESMANNE, G. BADANO, F. BOULARD, O. GRAVRAND, S. BISOTTO, C GRANGIER

ABSTRACT:
LETI realized for the first time pixel-level infrared filters based on frequency-selective surfaces that operate in the infrared range (2 to 6 µm) and can be easily integrated in the device fabrication process. A complete understanding of the role of metal absorption was acquired, to elucidate the ability of those filters to address the different wavelength bands and obtain the desired lineshape.

Context and Challenges

The classic method to obtain colored infrared images relies on filter wheels, which are inexpensive, flexible and can house a variety of optical elements. They are ideal for astronomy, satellite observation or applications that need high spectral resolution. In recent years though, imaging applications are emerging where measurement in 4 wavelength bands is sufficient. Exempli gratia, the concentration of certain gases can be recognized based on the detection of a few absorption lines, provided that their nature is known a priori. Two-color detectors are used to discriminate friends from foes in tactical contexts, or to spot decoys. For some of these applications, synchronous multiband detection is required at speeds that cannot be achieved with a filter wheel.

The infrared industry has invested heavily into researching and developing imagers with this type of capabilities, but no standard solution has yet emerged, in spite of efforts. For starters, high-end infrared detector development is mostly military driven. It has historically focused on high-performance device designs which proved expensive to realize and technologically complicated. Second, industry has been reluctant to develop entirely new production lines, facing uncertain marketability.

A viable alternative solution is to functionalize each pixel with a filter, like in visible sensors that integrate arrays of Bayer filters. From the standpoint of performance, such integration would reduce quantum efficiency (because of filtering) and produce images with slightly different registration for each color. However, the benefits of adapting the existing infrared detectors to a variety of novel applications overshadows the disadvantages.

The difficulty people have faced so far is that, in the infrared realm, we have no colored dyes to use as filters. The most obvious solution represented by multilayer dielectric stacks, is suboptimal. At CEA, we have turned our attention to pixel-level frequency selective metasurfaces, composed metal-dielectric resonators tuned to a specific wavelength by their geometry. Their main advantage is that adjacent pixels can be tuned to a different wavelength without impacting the complexity of fabrication. monolithic arrays for new applications.

Main Results

We demonstrated bandpass frequency selective metasurfaces, made of at least one layer of metal pierced with periodic resonant apertures. Frequency-selective surfaces have been used for decades in the microwave and radiofrequency domains and recent attempts have been made to adapt them to infrared and visible frequencies, with limited success. Past work lacked a general understanding of the effect of loss on the lineshape,

hence the transmission. We have formulated an analytical model for the filter based on the temporal coupled-mode theory and showed that the lineshape is fundamentally Lorentzian; its linewidth Δλ is linked to the resonant frequency and the transmission efficiency via the metal properties ,

This enabled us to realize FSS filters operating in the 2-5 µm range, using ion beam lithography on the backside of a commercial infrared detector (Figure 1), which was subsequently characterized to determine the spectral lineshape of each pixel. We have also realized FSS on a standard Si foundry, which allows for much higher resolutions in the definition of the resonant cavities. EO characterization showed good agreement with the simulations. In summary, we were able to design and produce the first functional FSS in the infrared domain, both standalone and directly on the backside of a HgCdTe focal plane array.
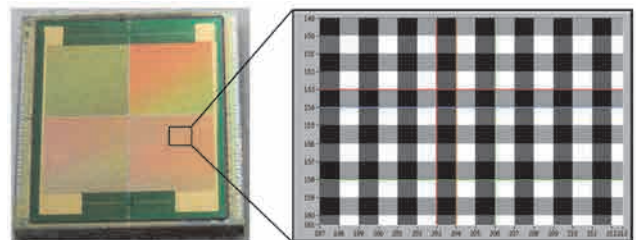

Figure 1: Experimental realization of an infrared frequency-selective metasurface made of apertures in metal.

Perspectives

This work opens the way to a variety of multispectral imaging applications in the infrared domain.

RELATED PUBLICATIONS:
1] F. Simoens and J. Meilhan, "Terahertz real-time imaging uncooled array based on antenna- and cavity-coupled bolometers," Philosophical Transactions of the Royal Society of London, vol. 372, pp. 20130111, Mar., 2014.
[2]. F. Simoens, J. Meilhan, and J.A. Nicolas, "Terahertz Real-Time Imaging Uncooled Arrays Based on Antenna-Coupled Bolometers or FET Developed at CEA-Leti,", J. of Infrared, Millimeter, and Terahertz Waves, Vol. 36, Issue 10, pp 961-985, 2015.
[3] M. Perenzoni et al., 'A monolithic visible, infrared and terahertz 2D detector', IRMMW-THz2010
[4] J Meilhan, Oden, J., Ouvrier-Buffet, J.L., Hamelin, A., Delplanque, B., Simoens, F, . Uncooled terahertz video micro-bolometer camera: Toolbox to optimize the sensitivity by tuning antennas and cavity, IRMMW-THz 2016

UNDERSTANDING THE BEHAVIOR OF SnAg BUMPS AT 10 µm PITCH AND BELOW FOR IMAGING AND MICRODISPLAY APPLICATIONS

AUTHORS:

D. TANEJA, M. VOLPERT, G. LASFARGUES, T. CATELAIN, D. HENRY and F. HODAJ[1]

ABSTRACT:

The finer pitch of 10 µm and below is currently explored by Microdisplays and Imaging industries. There are many contenders for achieving assembly at this pitch e.g. Cu-diffusion, Microtubes, Indium Bumps and SnAg bumps. Among the contenders, SnAg bumps are used for larger bumps but their capabilities for the finer pitch is yet to be explored. In this paper, behavior of SnAg for smaller bumps for the finer pitch is studied and compared to the larger bumps. Different reflow conditions such as environment, different type of flux, temperature profile are examined. During this study, some particular bumps were observed, which we called as hedgehog bumps and their behavior is discussed in this paper. The conclusions drew from the reflow studies have been used to achieve assembly. The behavior of SnAg alloy during the assembly is also explored.

SCIENTIFIC COLLABORATIONS: **[1]** Univ. Grenoble Alpes, SIMAP, Grenoble INP, France

Context and Challenges

As the density of pixels for Imaging and Microdisplays is vigorously increasing, the pitch for interconnections needs to be decreased proportionately. In some industrial roadmaps of IR sensors and Microdisplays, the pitch is approaching 10 to 5 µm with bumps of diameter 2 to 3 µm. One of the promising materials for the pitch of 10 µm or less are copper pillar, Ni diffusion barrier layer and SnAg solder alloy. They are well studied for larger pitch assembly but they are yet to be investigated for finer pitch. In this study, Cu/Ni/SnAg Pillars are investigated for the first step of assembly process, i.e. reflow. We anticipate that by decreasing the size, we may see some different behaviors which were suppressed/neglected in larger diameter bumps due to their big size. Here we are going to discuss about the change of behavior of solder from larger bumps to smaller bumps.

Main Results

Reflow is done by heating Cu/Ni/SnAg pillars above the melting point of Tin, forming a spherical cap. In practice whenever the solder is heated above its melting point it melts, however not always does it takes a spherical shape. This might be because of various reasons such as Sn oxide layer, wettability issues or improper reflow conditions.

To remove the native oxide, flux (weak acids) are used. The Cu/Ni/SnAg pillars are converted into bumps only when this flux is used in the inert atmosphere (figure 1), which is surprising because larger diameter Cu pillars doesn't show this behavior.
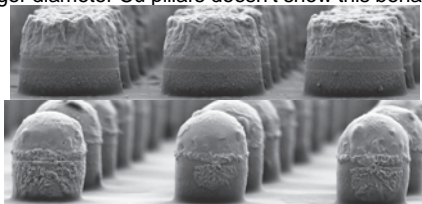

Figure 1: General view of 4 µm bumps after reflow with flux (a) in air and (b) in nitrogen

During our study, we observed in general a good spherical shape of bumps accompanied with various other formations such as scallops and crown formation, spilling of solder on the pillar and surface asperities on the top of the bump. (Shown in figure 2) These formations increase with increase in strength and type (acid content) of the flux.
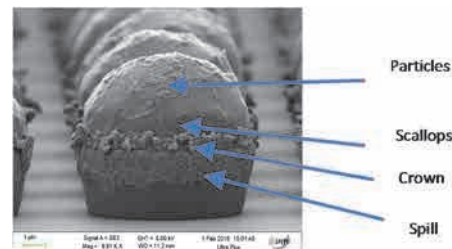

Figure 2: SEM Image of a bump after reflow in Nitrogen with liquid flux

The IMCS scallops and crown are observed for all the diameters, however due to their size, their effect becomes more substantial for smaller bumps as compared to larger bumps.

Surprisingly, the solder can be reflowed under nitrogen atmosphere (spherical shape obtained) without reducing the native oxide by a flux. During the reflow, the diffusion of Ni and Sn forms around 1µm of Intermetallics.

Finally, assembly at 10 µm pitch was successfully achieved with the shear strength of 110MPa. In the assembly process, no flux was used and no prior reflow was done. The achieved interconnect joint has almost no solder left therefore the properties of joint is almost like SLID joint. (Solid-liquid Interdiffusion).

This achieved assembly process is particularly surprising, as for the larger pitch (>50 µm), a prior reflow before the assembly is usually done, for better yield in bonding as reflow uniforms the height of the bumps and guaranties a good and even contact with the upper pad. Therefore it is logical to think that this prior reflow is mandatory for smaller bumps where uniformity is a challenge. However, in our study, we found this not to be true.
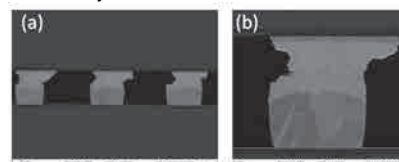

Figure 3: (a) Assembly at pitch of 10 µm. (b) Bonded 5 µm bump

Perspectives

The assembly at pitch of 10 micron was successfully achieved; but is approaching towards the SLID (Solid-Liquid Inter-Diffusion) process. Therefore it is important to study in the future the properties and the stability of the SLID joint Interconnect.

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[1] J. D. Reed, M. Lueck, C. Gregory, A. Huffman, J. M. Lannon,, D. Temple, "High Density Interconnect at 10µm Pitch with Mechanically Keyed Cu/Sn-Cu and Cu Cu Bonding for 3-D Integration", Proc. 60th Electronic Components and Technology Conf, 2010, p 846-852, Doi: 10.1109/ECTC.2010.5490704.

[2] J. Bertheau, P. Bleuet, F. Hodaj, P. Cloetens, N. Martin, J. Charbonnier, N. Hotellier, "Reflow processes in micro-bumps studied by synchrotron X-ray projection nanotomography", Microelec. Engin., vol. 113, pp. 123-129, 2014, doi: 10.1016/j.mee.2013.07.013.

[3] J. Derakhshandeh, "Relfow process optimization for micro-bumps applications in 3D technology", Proc. Electronics System-Integration Technology Conference (ESTC), 2014, pp. 1-5, Doi:10.1109/ESTC.2014.6962837.

[4] Taneja, D., Lasfargues G. / Volpert M. / Catelain T. / Henry D. / Hodaj F," Understanding The Behavior of SnAg Bumps at 10 µm Pitch and Below for Imaging and Microdisplay Application", Electronic Components and Technology 2016 Conference (ECTC)
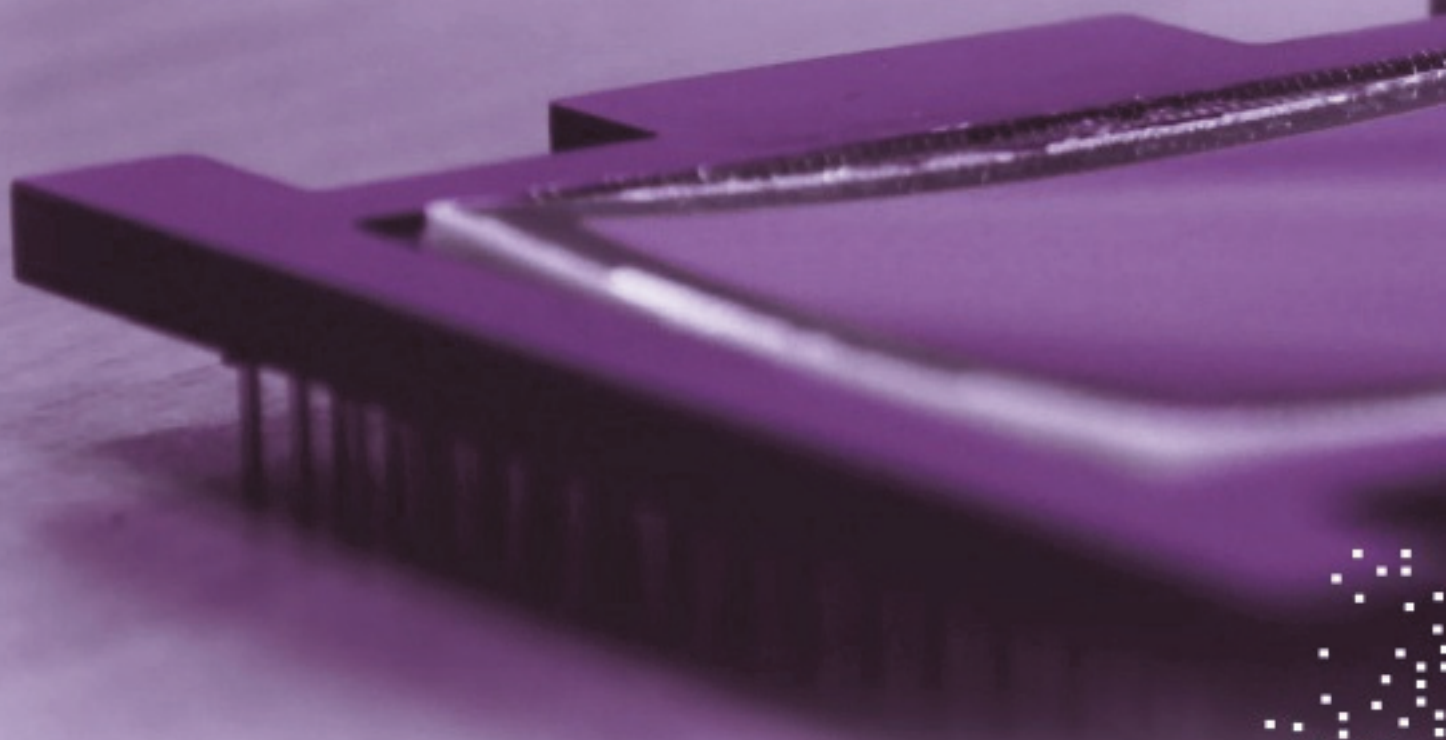
2.

INFRARED IMAGING:
Room temperature IR detectors

- **Multi-spectral IR**

- **THz camera**

- **Nano-electromechanical resonators**

A MULTISPECTRAL UNCOOLED INFRARED IMAGER FOR PASSIVE REMOTE GAS DETECTION AND IDENTIFICATION

AUTHORS:
DELPLANQUE B., BECKER S., BOUTAMI S., GOUDON V., HAMELIN A., MARTIN S., OUVRIER BUFFET J. L., POCAS S., RABAUD W., VIALLE C, YON J. J.

ABSTRACT:

The ability to detect and identify a gas by a standoff system is of particular interest for industrial and security applications. A well-known method is to use passive Long Wave InfraRed (LWIR) imaging where some form of spectral discrimination is implemented at the system level. In this work the spectral discrimination is brought to microscale and built directly at the sensor level. This is done by adding plasmonic structures on top of regular microbolometers. By tuning the geometrical properties of these structures the LWIR has been split into 4 bands. The manufactured chip is based on a 17 μm pitch 640*480 Focal Plane Array (FPA) on which spatial resolution is traded for spectral discrimination: the FPA provides 4 simultaneous 320*240 interdigitated subframes at 25 Hz.

Context and Challenges

With the advent of plug-in modules for smartphones, infrared imaging made its debuts in the consumer market. Whereas both LETI and industry's efforts have mainly been on performance and cost [1], a further way of standing out against the competition is to explore new functionalities.

Multispectral imaging is one of such new functionality that has an immediate application: toxic gas cloud imaging and identification [2]. LETI took on the challenge and created an uncooled multispectral infrared imager using plasmonic structures on top of microbolometers.

Main Results

Regular microbolometers have a broad absorption spectrum from at least 8 to 12 μm. This spectrum is defined mainly by the quarter-wavelength optical cavity created by the microbolometer membrane and a reflector.
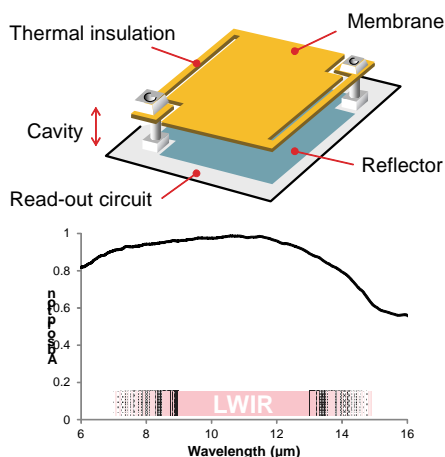

Figure 1: Schematic view of a μbolometer and absorption spectrum typically obtained with such geometry.

In this work, the spectral absorptivity is further adjusted by creating arrays of MIM (Metal Insulator Metal) structures on top of regular microbolometers. Tuning the lateral MIM patch dimensions and periodicity enables to adjust the absorption spectrum. In order to address the gas cloud imaging application four types of spectral responses have been designed, each with a distinct peak between 7 and 14 μm. These have been implemented as four types of pixels interdigitated on a 640*480 array of 17 μm microbolometers. In analogy to visible imagers, the manufactured chip can be described as a 320*240 array with four "coloured" subpixels. Performance of these spectrally selective microbolometers is only affected by the modification of the absorption spectrum: there is no degradation of the noise figure by the plasmonic structures.
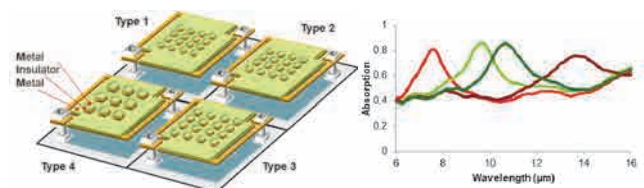

Figure 2: Schematic view of μbolometers with four sets of plasmonic structures and the resulting absorption spectrum

Finally a camera built with this imager has shown its ability to distinguish contents based on their spectral signatures, from demonstration filters to gases such as ammonia and sarin. In contrast to other solutions, the bolometer array itself provides the multispectral capability.
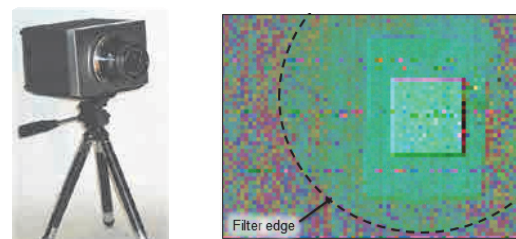

Figure 3: Camera and multispectral view of a scene comprising a selective filter - the filter area is rendered, arbitrarily, green depicting a spectral signature different from that of a blackbody.

Perspectives

LETI has demonstrated the use of plasmonic structures to engineer the spectral response of microbolometers. All the steps from simulation to manufacturing of functional imaging chips have been addressed. The focus is now on a tighter integration with industrial production schemes as well as capitalization with other existing assets of LETI in infrared and microbolometer technology.

RELATED PUBLICATIONS:

[1] Yon J.J., Dumont G., Goudon V., Becker S., Arnaud A., Cortial S., Tisse C.L., "Latest improvements in microbolometer thin film packaging: Paving the way for low-cost consumer applications", Proc. SPIE 9070, Infrared Technology and Applications XL, 90701N (June 24, 2014); doi:10.1117/12.2050378.

[2] B. Delplanque, S. Becker, S. Boutami, V. Goudon, A. Hamelin, S. Martin, J. L. Ouvrier Buffet, S. Pocas, W. Rabaud, C. Vialle, J. J. Yon, "A multispectral uncooled infrared imager for passive remote gas detection and identification", poster at the 12th Int. Symp. on Protection against Chemical and Biological Warfare Agents, Sweden, 2016.

UNCOOLED TERAHERTZ VIDEO MICRO-BOLOMETER CAMERA: TOOLBOX TO OPTIMIZE THE SENSITIVITY BY TUNING ANTENNAS AND CAVITY

AUTHORS:

J. MEILHAN, J. ODEN, J.L. OUVRIER-BUFFET, A. HAMELIN, B. DELPLANQUE, and F. SIMOENS

ABSTRACT:

THz uncooled bolometer imaging arrays developed at CEA-LETI provide flexibility both in frequency tuning and in specific features like polarimetry or multispectral detection. A complete design toolbox has been developed in order to optimize the performance and customize the pixel design for new applications. This paper describes this toolbox and validation modelling and experimental tests..

SCIENTIFIC COLLABORATIONS:

Context and Challenges

THz uncooled bolometer imaging arrays developed at CEA-LETI are based on two-storey cross-antenna pixel architectures that enable absorption at any polarization and frequency [1]. The antenna structures are built over a thick dielectric layer terminated by a ground plane -that we first introduced in this bolometer technology- in order to achieve an optimized resonant cavity for high absorption in the THz range, typ. 80-90% [2]. These imagers present state-of-the-art performance with a Minimum Detectable Power (MDP) of tens of pW measured while the array integrated in a camera is operated at a 25 Hz frame rate.

The intrinsic design of these pixels provide the ability to both tune the spectral sensitivity and integrate features that can be required for real-life applications, like polarimetry sensitivity, multispectral monolithic imaging (demonstrated in the FP7 Mutivis project [3]). Such tunability is eased by a modeling toolbox that we developed and validated to specify and design monolithic arrays for new applications.
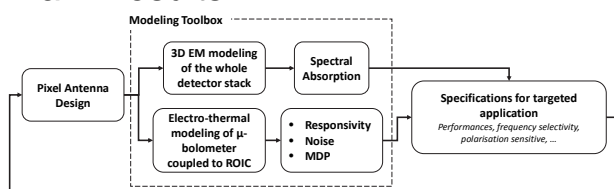
Main Results

Figure 1: Optimization scheme of antenna-coupled bolometer design

This design modeling tools combines 3D electromagnetic (EM) simulations of the complete detector (antennas-cavity-bolometer & CMOS Read-Out Integrated Circuit upper layers) and proprietary numerical models that predict accurately the dynamic electro-thermal behavior of bolometers coupled to the ROIC. These models [3] have been successfully validated by experimental measurements and can be used as a toolbox (Fig. 1.) to optimize the performance or to customize the pixel design for new applications.

In particular, thanks to signal and noise analysis of the μ-bolometer bridge we managed to point out the elements that degrade the performance of the prototyped 320x240 array. Considering the current response of the device, estimated at 0.79 A/W, and an equal noise contribution of the skimming bolometers, the MDP achieved prior to the read-out chain is close to 10 pW (Fig. 2.).

	Noise RMS Integrated on $[10^{-4} - 10^{4}]$ Hz	Injection Efficiency
Active Bolometer	6 pA	
Active Injection Transistor	31.8 pA	0.976
Total Noise	5.7 pA	

Figure 2: Modeled noise of the active branch of μ-bolometer bridge

This number has to be compared to the 32 pW measured at the ROIC output at 2.5 THz, with 80% of the incident radiation collected. This modeled MDP reveals that significant improvement can be expected if ROIC and pixel are better matched to achieve detector noise limited performances.

In terms of experimental tests, the spectral characterization of existing 2D sensors has been extended in the sub-THz range. The setup relies on reflective optics that guide the solid-sate source beam towards the array or a calibrated power-meter. The whole optical path is dried with N2 and translation stages move the detectors to take into account stationary wave effects. As previously shown by 3D EM simulations, the array presents a resonance at 850 GHz with a MDP of 100 pW, while the MDP increases at lower frequencies (Fig. 3).
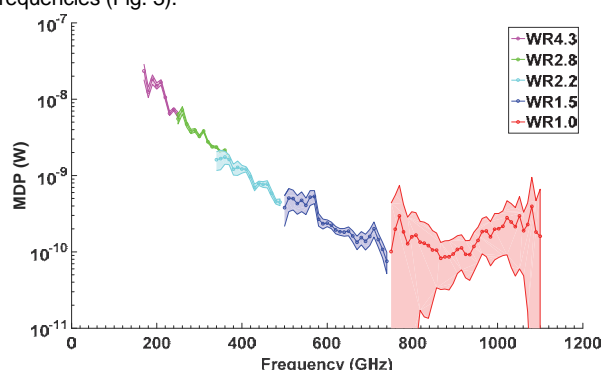
Figure 3: Measured MDP of current array between 0.1 and 1.1 THz For future sensors, introduction of AMC (artificial magnetic conductor) within the dielectric cavity will enable efficient detection at lower frequencies without significant changes of pixel design [4].

Perspectives

Development of a design toolbox allows us to tune the antenna-coupled bolometer array with respect to performance or specific feature specifications. This design chain has been validated by experimental results that have extended in the sub-THz range.

RELATED PUBLICATIONS:

[1] F. Simoens and J. Meilhan, "Terahertz real-time imaging uncooled array based on antenna- and cavity-coupled bolometers," Philosophical Transactions of the Royal Society of London, vol. 372, pp. 20130111, Mar., 2014.
[2]. F. Simoens, J. Meilhan, and J.A. Nicolas, "Terahertz Real-Time Imaging Uncooled Arrays Based on Antenna-Coupled Bolometers or FET Developed at CEA-Leti,", J. of Infrared, Millimeter, and Terahertz Waves, Vol. 36, Issue 10, pp 961-985, 2015.
[3] M. Perenzoni et al., 'A monolithic visible, infrared and terahertz 2D detector', IRMMW-THz2010
[4] J Meilhan, Oden, J., Ouvrier-Buffet, J.L., Hamelin, A., Delplanque, B., Simoens, F, . Uncooled terahertz video micro-bolometer camera: Toolbox to optimize the sensitivity by tuning antennas and cavity, IRMMW-THz 2016

12µM-PITCH NANOELECTROMECHANICAL RESONATOR FOR THERMAL SENSING

AUTHORS:

L. LAURENT, J.-J. YON, J.-S. MOULET, M.-L. ROUKES[1] and L. DURAFFOURG

ABSTRACT:

We provide here the demonstration of 12 µm pitch nanoelectromechanical resonant infrared sensor with fully integrated capacitive transduction. Low temperature fabrication process has been used to manufacture torsional resonator array. H-shape pixel with long nano rods 9µm-long and 250nmx30nm-cross section have been designed to provide high thermal response 1024Hz/nW and unprecedented Allan deviation of σ_A=3×10^{-7} at room temperature and 50Hz-bandwidth (σ_A =1.5×10^{-7} over 100ms, mechanical dynamic range of over 113dB). These features have allowed to reach resolution to 8-12 µm radiation of 27 pW/$\sqrt{}$Hz leading to a noise equivalent power (NEP) of 190pW at 50Hz (NEP=140pW at 100ms) and sub-millisecond response time. Style:

SCIENTIFIC COLLABORATIONS:[1] Kavli Nanoscience Institute, California Institute of Technology

Context and Challenges

Over the last 20 years microbolometer has become the most prominent uncooled infrared technology. Microbolometers operate by converting the radiation-induced heating of a thin membrane in a variation of electrical resistance. Thus, the sensitive part of a microbolometer pixel acts as a thermistor. Such thermistors are commonly made of a thin film of semiconductor, using mostly Vanadium Oxide (VOX) or amorphous silicon (α-Si). The induced heating effect is advantageously enhanced by achieving a high thermal insulation between the sensor and the substrate (2x10^8 K.W^{-1} have been reported for microbolometers with 12µm-pixel pitch). Today such devices have exhibited 50mK-noise Equivalent Temperature Differences (NETD) (F/1 lens, 30Hz frame rate, 300K background) [2,3]. Nevertheless, as a consequence of such high thermal insulation, in case of excessive radiant power the temperature of the sensing material can increase dramatically leading to a detrimental drift of the thermistor properties. To address this issue, we suggest unique pixel architecture for uncooled infrared detection whose arrangement calls for the replacement of the common thermistor by a non-electric thermal transducer, namely a mechanical nanoresonator designed to be highly sensitive to temperature.

Main Results

We choose a process close to a classical bolometer, which is above IC compatible (i.e. deposition process <300°C) [1]. Two silicon nitride layers of 10nm encapsulate a titanium nitride layer which will act as an electrode as well as an absorber. SiN features high Young modulus and low thermal conductivity which makes it a suitable material for long and narrow insulating rods. A 150nm layer of amorphous silicon is then deposited to have stiff enough resonator. Unlike resistive bolometer, no electrical connection is needed here between TiN and Si-α, simplifying thereby the process. A λ/4 cavity is formed between the reflecting electrodes and the paddle by removing the polymer, using plasma chemical releasing. Consequently, we fabricate a resonant Fabry-Pérot cavity centered at 8µm. The thickness of TiN has been chosen to match the impedance of vacuum (376.7Ω) and minimize the incident wave reflection leading to 50%-absorption efficiency. To drive and read our resonant electromechanical bolometer, we split the reflecting electrode into two electrodes, for electrostatic actuation and capacitive sensing respectively. The TiN incorporated into the paddle would be polarized, in order to raise a capacitive sensing signal. The electrostatic torque applied enables the torsion of suspended rods. Typical devices are shown In Fig 1 a) & b).
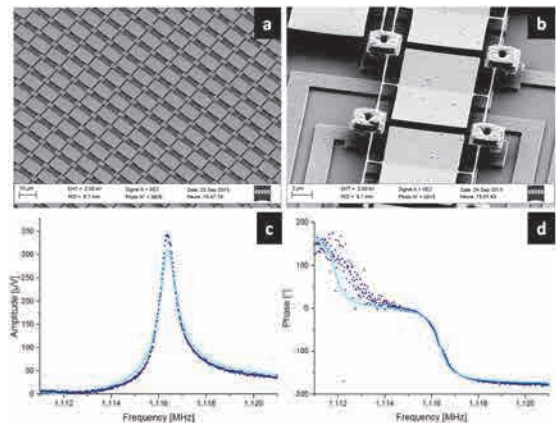

Figure 1: a) & b) Scanning electron microscope (SEM) images of the bolometer - c) & d) Experimental amplitude and phase signals of a typical frequency response (dots) and their theoretical fits (light blue lines - Q=1800)

We performed a frequency sweep of the actuation signal to find the resonance frequency and determine the quality factor. Typical results are shown in Fig. 1c) & d). The quality factor Q extracted from this measurement at $P = 5.10^{-5}\ mbar$ is equal to 1800 – depending on designs quality factors are between 900 and 3000. Remarkably we were routinely able to measure 30aF capacity variation at resonance through a static capacitance 0.18fF with a signal to background ratio 22dB – tiny capacitance variation of 2.6aF was even measured [2]. Experimental sensitivity to 8-12 µm radiation below 27 pW/$\sqrt{}$Hz has been reached leading to a NETD of 2K at 50Hz-bandwidth integration, NETD=1.5K at 100ms, with a sub-millisecond response time.

In conclusion, we have demonstrated the great potential of resonant sensor fabricated with a low temperature process dedicated to infrared imaging. A complete electrical transduction was developed to drive and read the useful signal according to calibrated temperature variations. High dynamic range corresponding to a torque angle up to 13°, i.e. 50% of the gap (113dB), has been demonstrated. That enables to enhance the output electromechanical signal. A NEP of 190pW has been measured with our system at 50Hz-integration time.

Perspectives

To improve the NETD, the temperature sensitivity has to be increased at least by a factor ten. To this end, works based on first order phase transition material should allow to increase the frequency response through a large improvement of the TCF.

RELATED PUBLICATIONS:

[1] L. Laurent, JJ. Yon, JS. Moulet, P. Imperinetti and L. Duraffourg, "Nano-electromechanical sensors for uncooled infrared IMAGING", SPIE Optics and Photonics 2016.

[2] L. Laurent, JJ. Yon, JS. Moulet, P. Imperinetti and L. Duraffourg, "Torsional nano resonator: characterization of a nonlinear hardening behavior and noise", IEEE Sensors 2016.
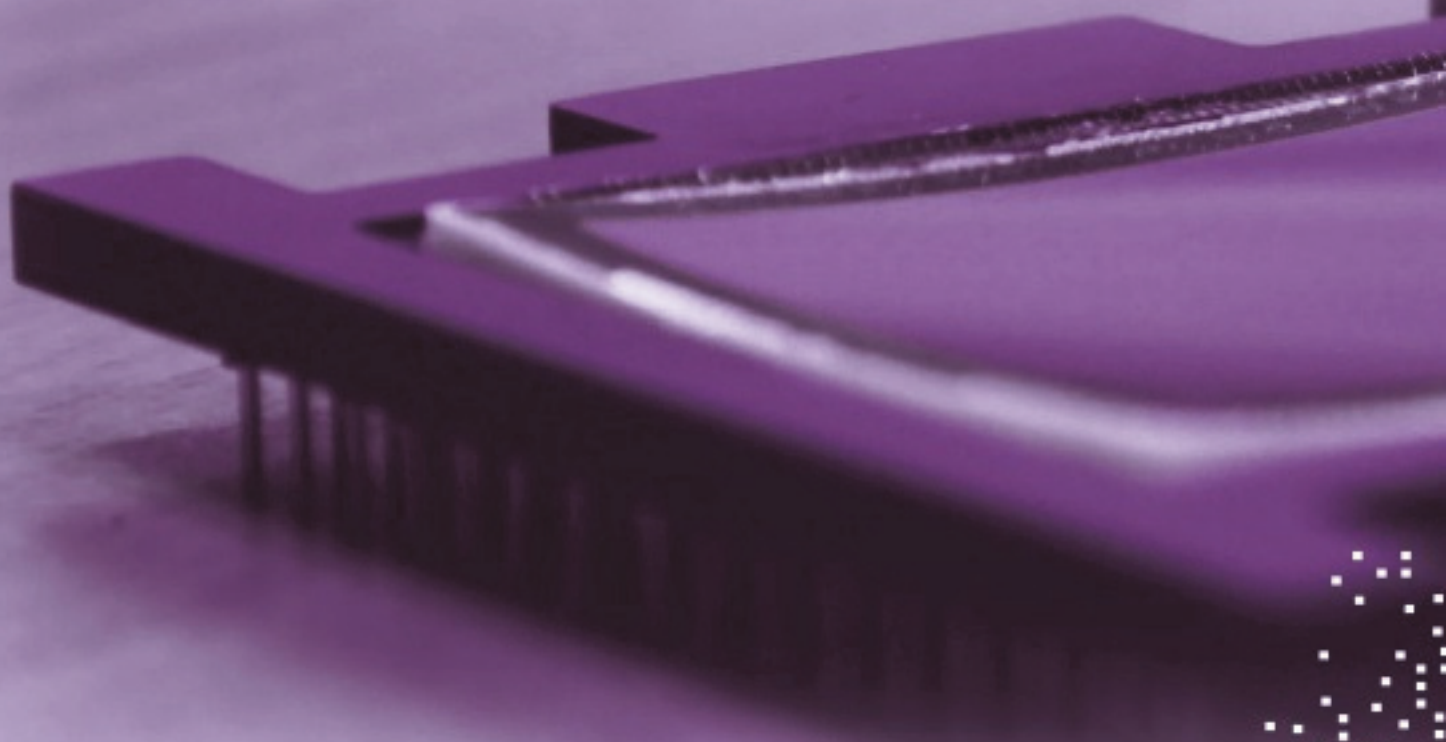
3.

OPTICAL ENVIRONMENTAL SENSORS

- Gas detection
- Non-dispersive IR sensors
- Integrated photo-acoustic sensors

CMOS COMPATIBLE METAL-INSULATOR-METAL PLASMONIC RESONATORS AS NDIR EMITTERS

AUTHORS:

S. BOUTAMI, A. LEFEBVRE, E. LORENT, D. JACOLIN, J.J. GREFFET[1], H. BENISTY[1]

ABSTRACT:

Metal-insulator-metal (MIM) plasmonic resonators have been extensively studied in literature as perfect light absorbers. Owing to Kirchhoff's law, they can be used reciprocally as thermal emitters, in infrared regime. We demonstrate here MIMs behaving as infrared monochromatic thermal emitters, strongly deviating from black body's radiation, with great interest for non-dispersive-Infrared (NDIR) gas spectroscopy. A specificity of our work is the development of a CMOS-compatible MIM technology on 200mm wafer scale, opening the way to low-cost mass production of such atypical infrared sources.

SCIENTIFIC COLLABORATIONS: [1] Institut d'Optique, CNRS (IOGS)

Context and Challenges

A body that is heated emits radiation, which is generally closely related to blackbody's radiation, spectrally broadband, with an intensity and a wavelength of maximal emission related to its temperature. It has however recently been shown by our colleagues from IOGS, that adding plasmonic resonant structures on such bodies could enable to tailor as desired the emissivity of the body, deviating strongly from black-body's radiation [1]. From this principle, we envisioned the way to develop monochromatic thermal emitter, based on metal-insulator-metal (MIM) plasmonic resonators, which are of great interest for NDIR gas spectroscopy for at least three reasons: the narrow spectral emission allows to address one single specific gas, the high angular emission enables high flux of photons for high sensitivity, and the low out-of-resonance emissivity permits to reduce total, and in particular useless, thermal leakage, and therefore the consumption of the final device [2]. This work is a step further that demonstrates the realization of CMOS-compatible MIMs NDIR emitters, using CMOS compatible metals, and wafer-scale lithography technique, to prove the viability of such structures for low-cost mass production, in particular for gas spectroscopy domain [3].

Main Results

The wavelength range of interest in this work is the mid-infrared ($\lambda \in [3\mu m - 12\mu m]$), in which most gases show absorption fingerprints. For MIMs, most state-of-art realizations use Gold as metal, which is an optically good metal; it has a low intrinsic absorption, i.e. a high reflectivity, leading to low background (out-of-resonance) emissivity MIMs. However, gold is a contaminant for CMOS circuits, therefore gold-based MIMs cannot not be realized in CMOS foundries. We opted for Tungsten (W), which we found to be the best compromise between optical properties and CMOS-foundries compatibility. The MIMs' insulator has been chosen as silicon nitride (SiN), which is a very common material in CMOS foundries. For MIM realization, and particularly MIM patterning, we used deep-UV lithography, avoiding production-costly electron-beam lithography. Structures realized are illustrated in figure 1, showing sub-micrometer resolution on a full-wafer scale, using a low-cost process. The results obtained and presented in the following have been highlighted by OSA in 2016 [4].
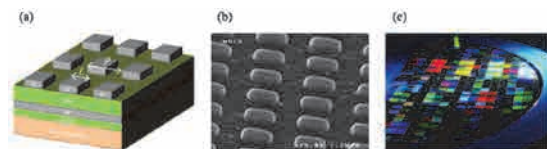

Figure 1: (a) Schematic of MIMs structures on Si wafer; (b) SEM view of MIMs after realization; (c) Photography of the final wafer with 5*5mm² dies with different MIMs configurations.

The experimental characterizations of MIM-dies, both in reflectivity and direct thermal emission, confirmed the monochromatic and high angular emission of structures, both necessary to assure single gas detection with high sensitivity. MIMs tunability or bi-spectrality, allowed by MIMs length variation, thus compatible with CMOS planar technology, has been also demonstrated, enabling fabrication of dies addressing different gases on the same wafer.
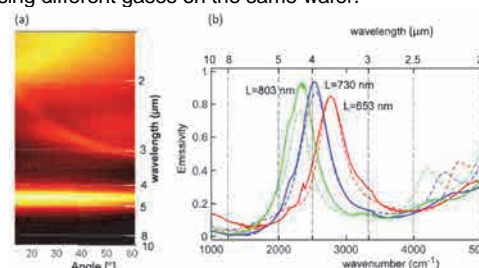
Figure 2: (a) Experimental emissivity diagram of MIMs structure, suited for CO_2 detection; (b) Experimental evidence of MIMs maximal emissivity tuning with lateral MIMs size variation, compatible with planar CMOS technology.

Perspectives

Our perspective consists in integrating these MIMs nanostructures on electrically-driven membrane microsources, to make discrete and integrable components, to be tested in a complete system device with gas. Required thermo-optical simulations of these device have been carried out [5], and realization is currently in progress.

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[2] D. Costantini, A. Lefebvre, A.-L. Coutrot, I. Moldovan-Doyen, J.-P. Hugonin, S. Boutami, F. Marquier, H. Benisty, and J.-J. Greffet, "Plasmonic metasurface for directional and frequency-selective thermal emission", Physical Review Applied 4, 1, 014023 (2015).
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MID INFRARED PHOTOACOUSTIC SPECTROSCOPY FOR MULTIGAS ANALYSIS: ON ROAD TO INTEGRATION ON SILICON

AUTHORS:

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ABSTRACT:

Photoacoustic cells are one type of optical sensors that can be used to detect gas traces. The photoacoustic spectroscopy technique is based on the absorption of photons by the molecules of interest and the subsequent creation of acoustic waves. Our miniPA cell combined with a quantum cascade laser exhibited extreme sensitivities in two different fields of application. A trend towards miniaturization is thus engaged to bring this new generation of high performance multigas sensors to a cost effective and mass production market.

SCIENTIFIC COLLABORATIONS: [1] MIRSENSE

Context and Challenges

PhotoAcoustic Spectroscopy (PAS) is one of the most sensitive techniques used to monitor chemical emission or to detect gas traces [1]. In particular, in the Mid InfraRed (MIR), many gases of interest have their strongest absorption lines. We have demonstrated [2, 3] our centimetric PA-device can compete with bulky systems for multi-gas sensing without any compromises on performances. We believe that this new sensor can already be deployed for several applications from oil industry to medical diagnostic.

Main Results

We have achieved the integration of our miniPA cell in two transportable setup for gas industry and medical diagnostic.
First, a CO detector on hydrogen has been designed, fabricated and tested. Using a CW QCL, and thanks to a fully numeric data processing on PC, we have explored different well known demodulation strategy to optimize the limit of detection. Assessments in a semi industrial condition on CO has been carried out as well as on nitrogen than on hydrogen. Finally a limit of detection of 200ppb has been obtained.

Figure 1 : Transportable miniPA based CO detector, typical package length 40cm.

A NO detector has been realized according to the same buildings blocks and footprint in order to cope with a very ambitious challenge on medical diagnostic field. The device features are namely ultra-low limit of detection (few ppb), fast response time (few seconds) and low cost disposable consumable. Our PAS gas detector has been modified to meet these requirements.

Today, we have showed that this miniPA cell can detect a concentration of NO in nitrogen-matrix of 15ppb in 1 second.
To make a fair comparison between our different miniPA versions, normalized noise equivalent absorption coefficient (NNEA) and noise equivalent concentration (for available laser power and 1s-integration time are summarized for several gases in the table below: .

Gas	Power (mW)	Wavenumber (cm-1)	MNEA 1σ $(cm^{-1}.W.Hz^{-\frac{1}{2}})$	NEC 1σ (ppm)
CH4(N2)	2.2	2939	1,3.10-9	0,03
CO2(N2)	5	2302,5	1,7.10-8	0,16
CO(N2/H2)	30	2127	3,3.10-7	0,3
NO(N2)	130	1906,1	3,2.10-8	0,015

Perspectives

The miniPA concept is being extended to an integrated multigas detector in collaboration with mirSense (www.mirsense.com) under a joint laboratory. We are focusing our development on an ultra-small cell and the TRL improvement assessing our detector on various conditions (temperature, hygrometric, aggressive gas, etc…).
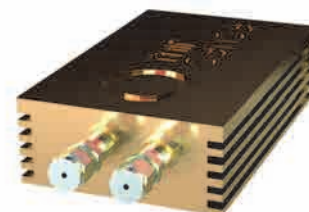

Figure 2: Artistic view of integrated multigas PA detector. Typical package length 7cm

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[[1] A. Miklós, P. Hess, and Z. Bozóki, "Application of acoustic resonators in photoacoustic trace gas analysis and metrology," Rev. Sci. Instrum., vol. 72, no. 4, pp. 1937–1955, Apr. 2001.
[2] Coutard, J.G, Rouxel J. / Brun M. / Lartigue O. / Nicoletti S. / Badets F. / Carras M. / Gliere A.   Development of a high performance miniaturized photoacoustic gas sensor   Laser Applications to Chemical, Security and Environmental Analysis (LACSEA)
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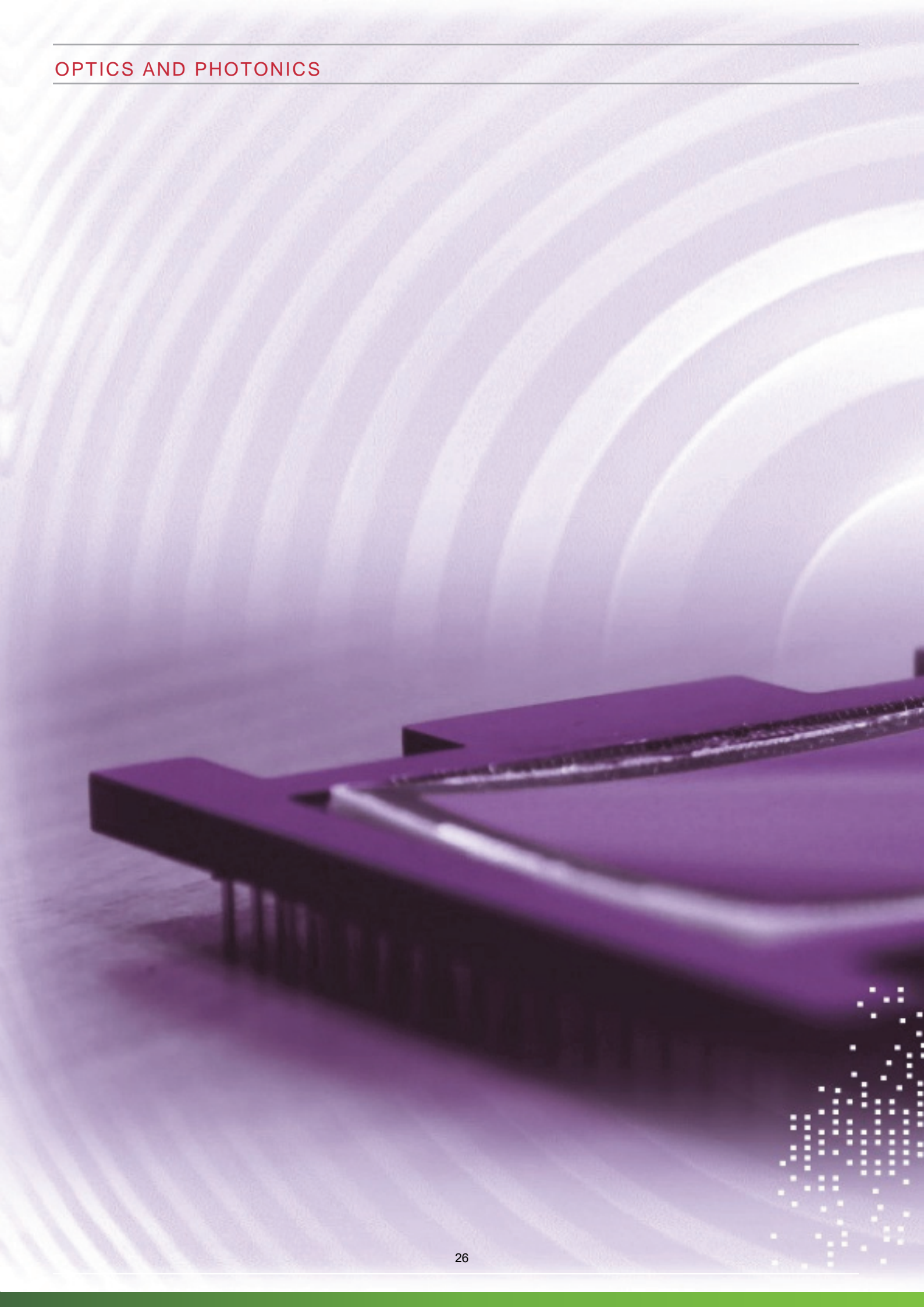
4.

SILICON PHOTONICS

- CMOS photonics III-V /Si devices
- SiNOI non linear photonics
- Modulators and receivers
- Hybrid optical lasers
- Photonic packaging
- Photonic systems

MULTI-PROJECT WAFER (MPW) OFFER BASED ON SOI 300 NM SILICON PHOTONICS PLATFORM

AUTHORS:

A MYKO, F GAYS, P LEMOIGNE, T ANFRAY, B KARAKUS

ABSTRACT:

Silicon photonics attracts more and more academics and fabless companies. Yet, the fabrication of photonic circuits requires expensive facilities and equipment so that very few institutions can afford. To solve this issue, CEA-LETI offers multi-project wafer (MPW) runs, twice a year through CMP and EUROPRACTICE brokers, to reduce significantly the cost of wafer production through sharing mask and process. This service is an excellent way to give researchers and fabless companies access to foundries' silicon photonics platforms and be able to fabricate photonic devices with critical dimensions at low cost.
In this paper, we present CEA LETI's MPW offer based on its 300nm-silicon photonic platform

Context and Challenges

LETI's integrated silicon photonics platform is developed for high-speed optical transceivers and highly-integrated optical interposer applications. The full 300 nm platform library includes waveguides for optical routing, grating fiber couplers, high-speed silicon electro-optic modulators and high-speed germanium waveguide photo-detectors.

LETI's silicon photonics full platform technology consists in:
• 200mm SOI substrate with 300nm Si and 800nm buried oxide
• Multilevel silicon patterning to define various silicon heights of 0, 65, 165 and 300nm allowing shallow rib, deep rib and strip waveguides
• A level for metallic (TiTiN) heater above the Si waveguides
• NiSi for silicided modulator contacts
• Four P and N-type doping levels for electro-optic modulators and silicon doped heaters
• Ge PIN photodiodes
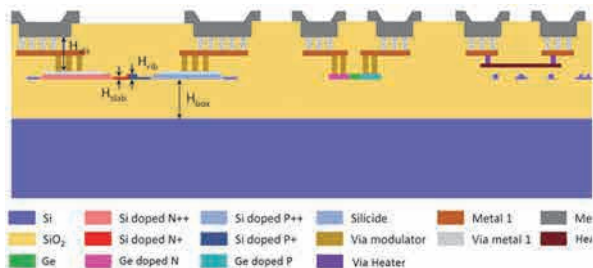• Two metal interconnect levels

Figure 1 : Cross section of LETI's 300nm-silicon photonics platform

LETI's silicon photonics full platform technology is compatible with additional options [1]:
• Under Bump Metallization on pads or Micro-bumping (Cu µpillar) for flip-chip integration
• Optical edge coupler
Moreover, this platform is fully compatible with that of STMicroelectronics which facilitate future volume production.

Main Results

To be able to design a photonic circuit, foundries must provide a complete Process Design Kit (PDK) that includes a set of tools such as compact models of passive and active components, layouts, design and physical verification tools. This PDK can be used by customers on existing CAD software.

Passive components

Component	Specifications	Indicative value
Rib waveguide	Loss	<2 dB/cm
Strip waveguide	Loss	<4 dB/cm
Bent Rib waveguide	Minimum radius	35 µm
Bent Strip waveguide	Minimum radius	3 µm
Transitions	Loss	<0.03 dB
Fiber grating coupler 1D	Insertion loss	<3 dB
	Central wavelength	1310 nm
	1dB bandwidth	27 nm
Fiber grating coupler 2D	Insertion loss	<5 dB
	Peak wavelength	1310 nm
	1dB bandwidth	25 nm
Directional coupler	Loss	<0.05 dB
Ring filter	Loss	< 0.5 dB
	Extinction ratio	>15 dB
	Quality Factor	>10,000
MMI 1x2	Loss	<0.5 dB
	Output balance	+/- 5%

Active components

Component	Specifications	Indicative value
Mach Zehnder modulator (3mm long)	OE bandwidth @-4V	40 GHz
	Loss junction	< 0.8 dB/mm
	VpiLpi @-2V	< 2 V.cm
Ring Racetrack modulator	OE bandwidth @-2V	>15 GHz
	Insertion loss	<0.5 dB
	VpiLpi @-2V	<2.5 V.cm
Ge Photodiode PiN longitudinal	OE bandwidth @-1V	>35 GHz
	Responsivity @-1V	>0.75 A/W
	Dark current @-1V	<50 nA

Perspectives

CEA LETI's MPW offer allows researchers and fabless companies to design their first silicon photonics circuits and to access its silicon photonics platform. New components will be later included, such as the laser, to match with companies' demands. More information on CMP and Europractice brokers: http://cmp.imag.fr/ and http://www.europractice-ic.com/

RELATED PUBLICATIONS:

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SI₃N₄ NONLINEAR PHOTONIC CIRCUITS FOR CMOS-COMPATIBLE OPTOELECTRONIC COINTEGRATION

AUTHORS:

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C. MONAT[1], L. K. OXENLOWE[2], and K. YVIND[2]

ABSTRACT:

We report on the fabrication and testing of Si_3N_4 nonlinear photonic circuits for CMOS-compatible monolithic co-integration with silicon-based optoelectronics. In particular, a novel process has been developed to fabricate low-loss dislocation-free Si_3N_4 750-nm-thick films for Kerr-based nonlinear functions featuring full thermal budget compatibility with existing Silicon photonics and front-end Si optoelectronics. Experimental evidence show nitride-based resonators using such low-temperature crack-free nitride film exhibiting quality factors exceeding $Q > 3 \times 10^5$ with signature of frequency comb onset under CW pumping, while continuum generation spanning 1510 - 1580 nm has been achieved on similar waveguides under pulsed pumping, thus paving the way to low-threshold power-efficient Kerr-based broadband sources featuring full thermal processing compatibility with Si photonic integrated circuits (Si-PICs).

SCIENTIFIC COLLABORATIONS: [1] CNRS / Lyon Institute of Nanotechnology (INL), France,
[2] Technological University of Denmark (DTU), Denmark

Context and Challenges

Silicon-based photonic integrated circuits (Si-PICs) pave the way towards a brand-new optoelectronics featuring a significant integration potential with cost-effective complementary metal-oxide-semiconductor (CMOS) technology and micro-nano-electronics circuits and nodes.

A paradigm shift in optical transmission can be however constituted by exploiting the full potential of X^3 nonlinear optical processes to generate Kerr supercontinua and frequency combs via optical parametric oscillators (OPOs). In this way, tens or even hundreds of optical channels can be obtained thus substituting an equal amount of III-V on Si individual laser diodes to be integrated on a chip as illustrated in Fig. 1. However, prior works based on stoichiometric Si_3N_4-based OPOs made use of high-temperature annealing (~1200°C) of the nitride film and silica uppercladding used to break N-H bonds otherwise causing absorption in the C-band, otherwise severely degrading its nonlinear functionality. As well as that, substrate preparation made by etching crack-limiting trenches in the SiO_2 undercladding has been also used to prevent the propagation of tensile strain-related cracks in the nitride film which would deteriorate dramatically the optical quality of the material. Indeed, the use of such technological building blocks would prevent a straightforward integration of such nonlinear circuits on existing Si-based photonics and optoelectronics as, for instance, extreme annealing would destroy the Silicon optical layer underneath along with its functions (modulation, photodetection, etc…). To prevent the aforementioned drawbacks, a new low-temperature crack-free process has been developed to deposit such thick nitride-based films for nonlinear optics applications exhibiting full process compatibility with Silicon photonics integrated circuits (Si-PICs). Such generated broadband sources can be simply filtered via wavelength demultiplexers into hundreds of separate new optical channels, providing sufficient aggregate data transmission bandwidth to reach 100's of Tbit/s and beyond.
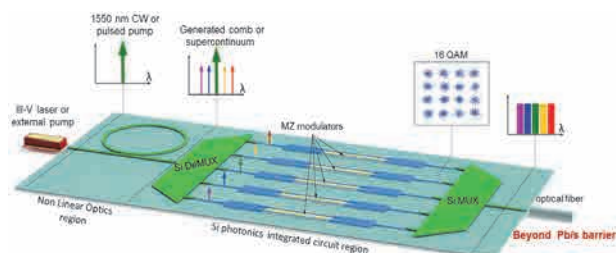

Figure 1: Principle of ultra-high speed rate communications with Kerr frequency combs (or supercontinuum). Artistic view of a future ultra-high rate transmitter, leveraging a Kerr frequency comb source (or supercontinuum) onto a Silicon optoelectronic chip.

Main Results

Continuum generation via nonlinear Kerr SPM. Edge-coupling via inverted taper was used to perform nonlinear optical characterization over a large wavelength span in the 1.55 μm region. Via a pulsed external laser, optical pulses of 4 ps with were put through 2.1-cm-long silicon nitride waveguides with tailored dispersion properties at a repetition rate frequency of 20 MHz. Kerr nonlinearity could be then used to access self-phase modulation (SPM) in such waveguides to generate a broad optical continuum capable to provide hundreds of new available optical frequencies to feed silicon passive or active circuitry for telecom applications including coherent transmission. Relevant experimental results are illustrated in Fig. 2. As shown, by increasing the peak power of the pump pulses, Kerr nonlinearity can be leveraged into a SPM process capable to generate a wide spanning continuum of new optical frequencies. Even wider spanning continua – therefore called supercontinua - can be obtained. Supercontinuum generation can be seen as a more valuable alternative to combs on the pathway towards the heterogeneous cointegration of optical nonlinearities onto Si-PICs. In fact, differently from Kerr-combs generation demanding precise and resonant pumping lock over the time, Kerr continua are more stable over the time, making this an ideal solution for data transmission, reducing the system complexity at the time-scale level.
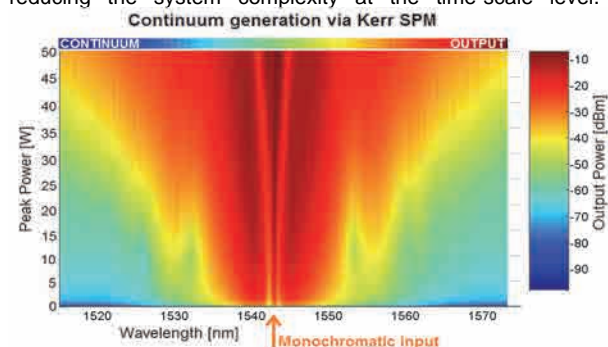

Figure 2: Spectral broadening of pump pulse via Kerr self-phase modulation (SPM) leading to the generation of a frequency continuum spanning from 1510 nm to 1570 nm.

Perspectives

This work paves the way toward the heterogeneous integration of nonlinear Kerr-based combs and supercontinuum sources with Si optoelectronics devices and circuits. Current research is focused on the use of III-V alloys such as AlGaAs on SOI – exhibiting several order of magnitude stronger Kerr nonlinear properties – to reduce the parametric threshold power dramatically. In the end, this would grant nonlinear effects full access to the realm of a cost-effective energy-friendly Silicon micro-nano-photonics.

RELATED PUBLICATIONS: [1] Marco Casale, Sebastien Kerdiles, Vincent Hugues, Houssein El Dirani, and Corrado Sciancalepore, "Low-Temperature Crack-Free Si_3N_4 Nonlinear Photonic Circuits for CMOS-Compatible Optoelectronic Cointegration,"SPIE Photonics West 2017, OE109, Jan. 2017.

LASING EFFECTS IN OPTICALLY PUMPED GeSn MICRODISKS

AUTHORS:
V. REBOUD, J. AUBIN, N. PAUC, A. GASSENQ, Q. M. THAI, M. BERTRAND, L. MILORD, J. ROTHMAN, T. ZABEL[2], H. SIGG[2], A. CHELNOKOV, J.M. HARTMANN, V. CALVO[1]

ABSTRACT:

Lately, germanium based materials attract a lot of interest as they can overcome some limits inherent to standard Silicon Photonics devices and can be used notably in Mid-Infra-Red sensing applications. One of the main challenges in the Silicon Photonic remains the fabrication of efficient group-IV laser sources compatible with the microelectronics industry, seen as an alternative to the complexity of integration of III-V lasers on Si. The difficulties come from the fact that the group-IV semiconductor bandgap has to be transformed from indirect to direct, using high tensile strains or by alloying germanium with tin. Here, a tunable direct bandgap is obtained by adjusting the Sn content, allowing to choose the emission wavelength. We demonstrated lasing operation with optically pumped GeSn micro-disk cavities emitting at 2.5 μm and 3.1 μm at cryogenic temperature.

SCIENTIFIC COLLABORATIONS: [1] CEA, INAC Institute, Grenoble ,France, [2] Laboratory for Micro- and Nanotechnology, Paul Scherrer Institut, 5232, Villigen, Switzerland

Context and Challenges

Si photonics is advantaged by its full compatibility with the current massively produced Si complementary metal-oxide semiconductor (CMOS) technology. Current barriers concern the properties of Si for key active optical functions (e.g. transform light into electrical signals and emit light), but also for passives components (e.g. extension of the current spectral range of integrated Si-based optical platforms to the mid-infrared for sensing applications). Lately, germanium (Ge) appeared to be a good candidate to tackle the current limitations of Si, since it is also fully CMOS compatible.

Recent progresses in Chemical Vapor Deposition (CVD) allowed lately to grow high Sn content in the Ge crystalline matrix. A direct bandgap can be obtained in GeSn if the Sn content is high enough and the residual compressive strain low enough (when grown on Ge). The low thermal stability of GeSn alloys requires a careful selection of process parameters during epitaxy. Growth conditions far away from thermodynamic equilibrium have then to be used, e.g. a combination of high growth rates and really low growth temperatures

Main Results

To grow very high Sn content GeSn layers, we investigated the benefit of using step-graded GeSn layers, instead of thick GeSn layers with nominally the same Sn content. Through a careful optimization of the Sn content in the step-graded layers, mirror-like surfaces were observed under grazing light with no significant Sn segregation over the whole 200 mm wafer (which was not the case for the GeSn grown with the same Sn content).

We studied then in details the influence of the strain relaxation for different devices and layers thicknesses and showed that the intrinsic compressive strain changes as a function of the layer thickness up to a quasi-full relaxation at the top surface for very thick layers (>480nm) [1]. The impact of strain on the band parameters of GeSn with Sn content ranging from 6% to 16% were investigated using PL and reciprocal Space Mappings (RSM) around the (224) XRD in order to measure Sn content of layers and strains.

We developed processes on (i) GeSn anisotropic etching (Figure 1) and (ii) isotropic selective etching of Ge versus GeSn (Figure 2a). Highly selective under etching was achieved even for GeSn with a Sn content as low as 6% (selectivity of 57 for 6% Sn layers, and 433 for layers with 8%) [2].

Figure 1. SEM images of various anisotropic etchings of GeSn/Ge stacks. Different conditions were used: a) Pressure 10 mTorr, Cl2/N2 gases at 100/25 sccm. b) Pressure 5 mTorr, Cl2/N2 gases at 100/25 sccm. c) Pressure 10 mTorr, Cl2/N2/O2 gases at 100/25/10 sccm

Under-etched micro-disks were used as optical micro-cavities. The under-etching of thick GeSn layers selectively versus Ge allows to confine optical modes and to relax the built-in compressive strain inside the layers, resulting in more direct band-gaps behavior (Figure 2a). The strain relaxation on the edge of the microdisks was measured by Raman spectroscopy [3]. Lasing spectra at 15 K are presented on Figure 2b for a 10 μm micro-disk fabricated in the 13 % GeSn layer grown on the GeSn graded buffer [3].

Figure 2: a) 45° tilted view SEM image of a GeSn microdisk, Light emission spectra at 15 K of (b) a 10μm microdisk and fabricated in the 13 % GeSn layer grown on the GeSn graded buffer

Perspectives

Our results give a better understanding of the intrinsic properties of the GeSn layers and the strain properties in GeSn devices with high Sn content for laser applications. The control of strain in GeSn layer, with high Sn content, is one of the keys to further improve the GeSn light emission towards a fully CMOS compatible laser working at room temperature.

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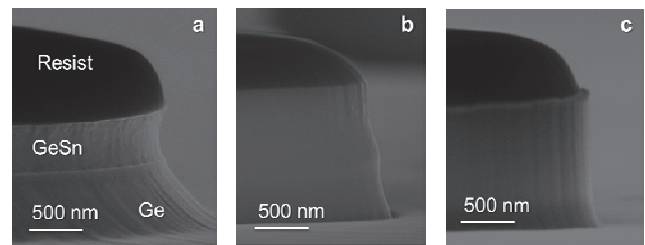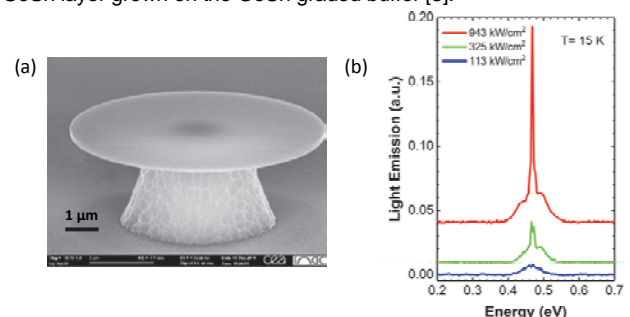
FIRST DEMONSTRATION OF A BACK-SIDE INTEGRATED HETEROGENEOUS HYBRID III-V/SI DBR LASERS FOR SI-PHOTONICS APPLICATIONS

AUTHORS:

J. DUREL[1, 2],, B. BEN BAKIR, C. JANY, S. CREMER, B. SZELAG, T. BRIA, V. LARREY, L. SANCHEZ,

P. BRIANCEAU, J.-A DALLERY[3], R. GUIAVARCH, T.CARD, R.THIBON, J.-E. BROQUIN[2], F. BŒUF[1]

ABSTRACT:

In this paper, to the best of our knowledge, the monolithic integration of a fully CMOS compatible hybrid DBR laser on the backside of a SOI wafer has been demonstrated for the first time. This innovative approach allowed implementing CMOS compatible electric interconnects and optical sources on a same chip. The optical characterizations confirm the single wavelength behavior of the realized devices which present a SMSR higher than 35 dB and can be tuned over 4 nm. This device opens the route to a fully integrated optical transceiver on a mature and industrial Silicon platform.

SCIENTIFIC COLLABORATIONS: [1] STMicroelectronics, 38 Crolles, France; [2] Univ. Grenoble Alpes, IMEP-LAHC, F-38 Grenoble, CNRS, [3] VISTEC Electron Beam GmbH, Jena, Germany

Context and Challenges

In recent years, Silicon Photonics has emerged as a solution for the volume manufacturing of optical transceivers addressing datacenter's needs in terms of increasing data-rate and reduced cost. Several Silicon-Photonics platforms have been demonstrated using standard Si technology [1]. While these platforms differ in many regards, they all lack of a monolithically integrated light source. To solve this problem, the most commonly proposed approach consists in bonding, using an adhesive BCB or a covalent SiO2/SiO2 bonding, an InP-stack onto a Si-wafer in order to fabricate a Hybrid III-V/Si laser [2-3]. Because of the substrates size mismatch between Si and InP, only small size InP-stack vignettes are bonded on Si using a pick and place process. Although promising hybrid lasers results were obtained at the device level, none of those demonstrations have been made with a standard CMOS-BEOL (Back-End of the Line) , preventing a proper electronic-photonic integration. Indeed, InP-stack thickness is about several µm, and needs to be bonded on a very flat silica layer at only ~ 100 nm from the SOI. for this reason, not only vignette attachment cannot be done after BEOL deposition, but also BEOL cannot be processed after the bonding of the InP-stack because of the thickness of this latter. To solve these problems, a back-side integration scheme has been developed.

Main Results

DBR (Distributed Bragg Reflector) cavity based laser has been specifically designed for a back side integration operation [4]. It includes a III-V zone of gain in InP with InGaAsP MQWs (Multiple Quantum Wells) separated from a 500 nm-thick SOI by a silicon oxide layer of about 100 nm-thick. The maximum optical gain of the MQWs is centered at a wavelength of 1310 nm. The fabrication of the hybrid III-V/Si laser can be divided in two different main steps. First of all, the SOI wafer is processed on a 200 mm CMOS platform in order to pattern the silicon part of the hybrid laser, the waveguide, the grating coupler with a metallic layer on top, which is actually the first interconnection layer and acts as a mirror. Then, a new silicon substrate is bonded on top of the SOI. The entire stack is flipped over to remove the initial substrate and BOX by grinding and thinning. The DBR mirrors is then defined and a 3 inches wafer of III-V is directly bonded on the patterned SOI. Finally, the III-V part is patterned and metallized as it would be done in the Front side integration scheme.
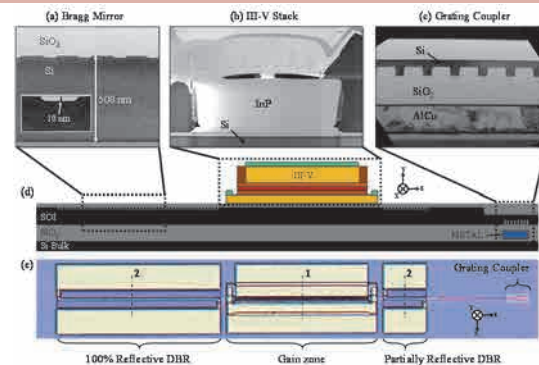

Figure 1. Global view of the fabricated device with (a), (b) and (c) SEM of respectively the DBR, the gain zone and the grating coupler and with (d) and (e) respectively a schematic longitudinal view and a microscope view of the device.

The electrically pumped lasers have been tested under continuous-wave current conditions. The output power is up to 1.15 mW at an injection current of 200 mA. The lasing threshold is 45 mA.The laser spectra are shown in Fig. 2a for different injection currents and reflect its single-wavelength laser operation with a central wavelength of 1291 nm. A Side Mode Suppression Ratio (SMSR) of more than 35 dB has been measured, which proves the good spectral purity of this laser. A shift in wavelength that can be achieved by current injection into heaters above DBRs (Fig2b)
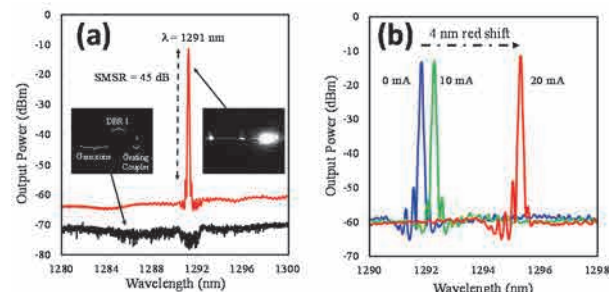

Figure 2. Characterization results: (a) Laser spectra at 20 mA and 100 mA injection currents with an IR picture of the device for each; (b) Laser spectra for different applied currents on the Bragg heaters

Perspectives

With this result, we demonstrate a new laser integration scheme suitable for industrial silicon photonic platform. The next step will be the 300mm integration using CMOS compatible materials and processes on a full silicon photonic platform including active devices and 4 metal levels BEOL.

RELATED PUBLICATIONS:

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[3] S. Keyvaninia, et al., "Demonstration of a heterogeneously integrated III-V/SOI single wavelength tunable laser," Optics Express, vol. 21, no. 3,, Feb. 2013
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SELF-ALIGNMENT WITH COPPER PILLARS MICRO-BUMPS FOR POSITIONING OPTICAL DEVICES AT SUBMICRONIC ACCURACY

AUTHORS:

Y D. ZONOU, S BERNABE, D FOWLER, M FRANCOU, P ARGUEL [1] O CASTANY,

ABSTRACT:

We have studied self-alignment properties between two chips that are stacked on top of each other with copper pillars micro-bumps. The chips feature alignment marks used for measuring the resulting offset after assembly. The accuracy of the alignment is found to be better than 0.5 µm in x and y directions, depending on the process. This high accuracy self-alignment was obtained after studying the impact of flux and fluxless treatments on the wetting of the pads and the successful assembly yield. The composition of the bump surface was analyzed with Time-of-Flight Secondary Ions Mass Spectroscopy (ToF-SIMS) in order to understand the impact of each treatment. This study confirms that copper pillars micro-bumps can be used to self-align photonic integrated circuits (PIC) with another die (for example a microlens array) in order to achieve high throughput alignment of optical fiber to the PIC

SCIENTIFIC COLLABORATIONS: [1] CNRS/ LAAS (Laboratoire d'Analyse et d'Architecture des Systèmes), Toulouse, France

Context and Challenges

Packaging of optoelectronic devices is a major contribution to the module cost (up to 80%) [1]. This is mainly due to the *active alignment* process between single-mode devices, which requires high alignment precision in the micrometer range and is a unitary and time consuming process. Different methods of *passive alignment* were studied in order to reduce manufacturing cost, while enabling the assembly of complex optical devices. In this context, a promising solution is the approach based on the *self-alignment* effect of solder bumps during the melting stage. This solution has the advantage to allow batch assembly process and is compatible with existing manufacturing equipment, which reduces the cost of the packaging.

Main Results

Proper wetting of the solder is a necessary requirement for self-alignment to occur as expected, which requires the application of an adequate surface treatment [2]. In order to understand the actions of the surface treatment on SnAg micro-bump, we performed ToF-SIMS analysis of the oxygen and carbon remaining on the surface of the bumps after each treatment. This gives information on the ability of the treatment to remove the oxide layer and the organic contamination remaining on the bumps

In our study, Self-alignment samples are treated with liquid flux, formic acid, or pre-treated with liquid flux. The alignment marks and the Vernier scale are observed in the infrared with a microscope, in order to measure the alignment accuracy (**Erreur ! Source du renvoi introuvable.**). After flip-chip assembly all samples with efficient surface treatment (halogenated liquid flux, formic acid 8%, and halogen liquid flux with pre-clean) reached a self-alignment precision better than 0.5 µm. In the case of the halogenated liquid flux (**Erreur ! Source du renvoi introuvable.** c) we observe some residues between copper pillars, which are absent with the two other techniques. Since we do not want to alter the optical

transmission with flux residues, we gave our preference to these two techniques for the next set of experiment, namely formic acid (HCOOH 8%) treatment and pre-treatment with liquid flux.
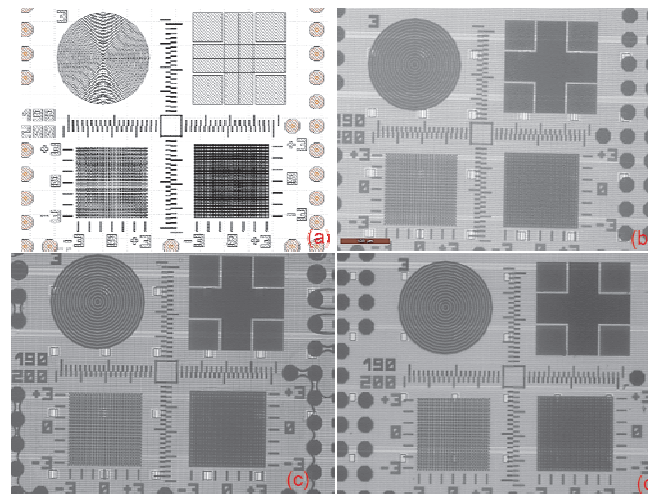

Figure 1: Infrared microscope observation through silicon Chips of the measurement pattern after chip assembly and self-alignment. (a) ideal alignment according to the design (b) self-alignment with formic acid, (c) liquid flux : presence of residues on the borders of the figure between each copper pillar (d) pre-treatment with liquid flux

Perspectives

In this study we demonstrated that self-alignment with copper micro-bumps can reach an accuracy lower than 0.5µm, this will enable low cost, high throughput assemblies of single mode fiber connectors on Photonic Integrated Circuits. Our goal is to address single mode optical interconnection for data centers.

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SILICON PHOTONICS TRANSMITTER AT 32 GB/S FOR DATACENTER APPLICATIONS

AUTHORS:

S. OLIVIER, S. MALHOUITRE, C. JANY, B. CHARBONNIER, G.-H. DUAN[1], G. LEVAUFRE[1]

ABSTRACT:

Silicon photonics is considered as a disruptive technology for next generation data communications such as high data rate short-reach communications in datacenters. Among the different challenges to address are the integration of efficient, low-voltage and low power consumption optical modulators on Silicon and the integration of efficient light sources. We have recently demonstrated a silicon photonics transmitter integrating a hybrid III-V on Si distributed feedback laser source, a hybrid III-V on Si electro-absorption modulator and a booster hybrid III-V on Si booster amplifier. This fully integrated transmitter operates at a data rate of 32 Gb/s at 1.3 μm datacom wavelength, meeting the requirements for next generation transmitters in datacenters.

SCIENTIFIC COLLABORATIONS: [1] III-V Lab, Palaiseau, France

Context and Challenges

Since two years, we have entered the Zettabyte era, which means that more than one billion Terabytes are exchanged each year through the Internet. Datacenters are at the heart of these communications. They generally house several tens of thousands of servers that must be flexible by being capable to allocate any job to any server at any time to meet the user demand. The technology of short-reach datacom networks (< 2 km) must therefore be adapted to high-volume market with low cost, reduced energy consumption and ever increasing bandwidth.

To meet the performance requirements in more and more compact modules, an integrated photonics technology must be developed to replace the assembly of discrete components. Silicon photonics technology is an excellent platform for the development of next generation transmitters and receivers fully integrated with their control electronics.

One of the main challenges of silicon photonics is the integration of an efficient light source. Up to now, heterogeneous integration of III-V semiconductors with silicon through wafer bonding techniques has revealed to be the most suitable in the short and medium terms. In this approach, unstructured InP wafers or dies are bonded, epitaxial layers facing down, on a silicon-on-insulator wafer (SOI) structured with optical waveguide circuits. Then the InP growth substrate is removed and the III-V epitaxial film is processed to define III-V waveguide structures and metallizations. Such approach exploits the highly efficient light emission properties of some direct-gap III-V semiconductors materials such as InP and the compact and low-loss filtering and multiplexing in silicon.

Main Results

CEA-Leti has developed in collaboration with III-V Lab a fully integrated transmitter composed of a hybrid III-V on Si distributed feedback laser integrated with an electro-absorption modulator and a semiconductor optical amplifier to boost the output power.
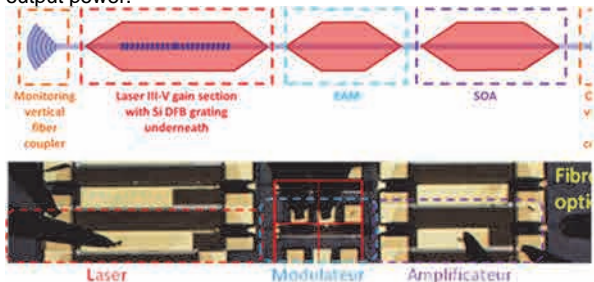

Figure 1: Schematics of a hybrid III-V/Si transmitter integrating hybrid DFB laser, electro-absorption modulator and semiconductor optical amplifier.

The DFB lasers are designed in such way that the light is generated in the III-V material and slightly overlaps the Si DFB (Distributed Feedback) grating underneath. The DFB laser has the advantage to feature a robust monomode behaviour as its wavelength is determined by the pitch of the high-quality grating etched in Silicon.

The architecture of the transmitter is illustrated in Figure 1, together with an optical microscope picture.

The spectrum of the transmitter is shown in Figure 2a. It features an excellent monomode behaviour with a side mode suppression ratio larger than 40 dB. Figure 2b depicts the output power of the transmitter coupled to a monomode fiber as a function of driving laser current for various reverse voltages applied to the modulator. With no bias on the modulator, the output power is around 0.5 mW and drastically drops when a reverse voltage is applied to the modulator. Figure 2c shows the output power of the transmitter as a function of the voltage applied to the modulator. The static extinction ratio is excellent, aroud 20 dB for only -2V applied to the modulator.
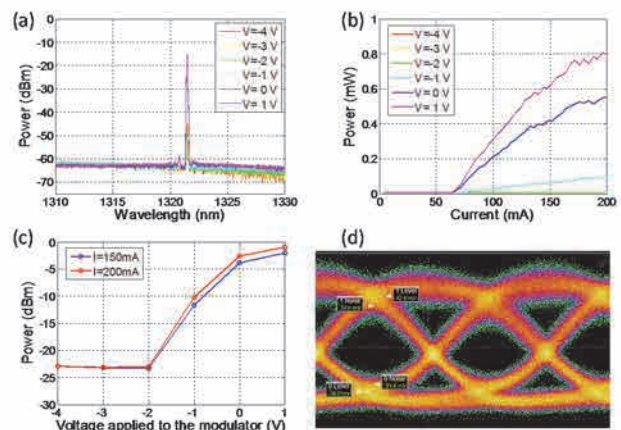

Figure 2: (a) Spectrum of the tintegrated ransmitter ; (b) ouput power of the transmitter coupled to a monomode fiber as a functiuon of laser current and for different reverse bias voltages applied to the modulator (the driving current of the SOA is 100 mA) ; (c) Ouput power coupled to the fiber as a function of reverse voltage applied to the modulator; (d) Eye diagram at 32 Gb/s.

Finally Figure 2d shows the eye diagram at 32 Gb/s for a random modulation signal with optimized pre-emphasis of the electrical signal. A very good dynamic extinction ratio of 6.7 dB is measured for a small modulation voltage of only 0.9V around a reverse DC bias of -0.6V. Such modulation voltage is compatible with CMOS driver electronics for a future photonic-electronic integration.

Perspectives

These results strengthen the potential of hybrid III/V on Si light sources, modulators and amplifiers for applications beyond 100 Gb/s in datacenters by integrating such transmitters in more complex WDM circuits gathering several channels with co-integration of their CMOS driving electronics.

RELATED PUBLICATIONS:

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DESIGN AND IMPLEMENTATION OF AN INTEGRATED RECONFIGURABLE SILICON PHOTONICS SWITCH MATRIX WITH MORE THAN 800 ACTIVE DEVICES DRIVEN

AUTHORS:

C KOPP, M FOURNIER, L ADELMINI, O LEMONNIER, D FOWLER, G PARES, O CASTANY, B BOUILLARD, L BOUTAFA, A VANDENEYNDE

ABSTRACT:

Silicon photonics is widely considered a key enabling technology for further development of optical interconnect solutions to facing growing traffic on the Internet. Thanks to the high index contrast between silicon and oxide, small footprint circuits can be designed with submicron-mode field diameter and few-micron waveguide bend radius. Thus, silicon photonics on a SOI platform provides an unrivalled integration capability level, with the possibility to implement passive and/or active functions. In this quest for higher integration, we report on the design and the assembly of photonic switch matrix demonstrators destined to next generation flexible optical network. The core of the switch matrix is based on a photonic integrated circuit (PIC) which deals with 12 WDM channels, 8 add/drop ports and 4 WDM line ports. The PIC gathers on the same chip more than 1000 passive and active devices driven by a CMOS circuit.

Context and Challenges

Next generation of photonic devices for the optical network are required to be both high speed and flexible. Reconfigurable add and drop multiplexers (ROADM) are key to avoid any manual intervention in case of the configuration of the optical node end points. At this end, we have developed a new architecture based on the use of an additional block denoted as transponder aggregator (TPA) replacing the fixed WDM multiplexer and demultiplexer (Fig. 1).
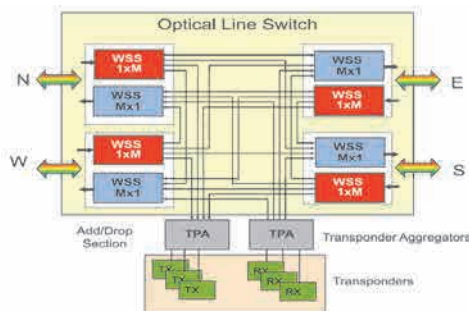

Figure 1: Colorless-Directionless-Contentionless ROADM

Based on silicon photonic integration technology, a new concept of integrated TPA device has been introduced and developed [1]. This TPA can be used for 2 functions: dropping WDM channels from the input line ports to local drop ports and adding WDM channels from local add ports to the output line ports (Fig. 2).
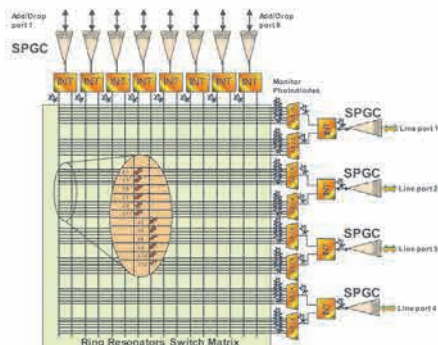

Figure 2: Architecture of the developed TPA

In the Drop switch, four sets of up to 12 WDM channels, 200GHz spaced, arrive at each of the four input line ports. In the Add switch, eight tunable transmitters add a WDM signal to the chip.

Main Results

The core of the TPA is based on photonic integrated circuit (PIC) using silicon photonic integration technology developed at LETI. The PIC gathers on the same chip more than 1000 passive and active devices. Passive devices are mainly waveguides, grating fiber couplers and interleavers blocks to separate the input channels into odd and even channels in order to increase the wavelength spacing in the switching matrix and to relax the channel isolation requirements. The signals are then sent to the switching matrix constituted by an optical crossbar of micro-ring resonators (MRR) switch elements [2]. This approach leads to 768 ring filters and 84 monitoring photodiodes on the 8x8mm² PIC to be driven by a CMOS circuit based on 160nm BCB8sP technology. This electronic integrated circuit is flip-chipped on the PIC (Fig. 3) using a 3D hybrid integration technology proposed by LETI through the Open 3D™ offer : 50µm pitch micro pillar interconnect.
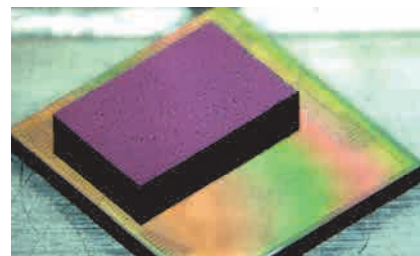

Figure 3: 3D stack optical engine with a flip chipped CMOS driver on the photonic integrated circuit

Perspectives

Several versions of the 3D stack optical engine have been connected to a 12 channel fiber array and mounted onto a test board (Fig. 4). These prototypes are now under test.
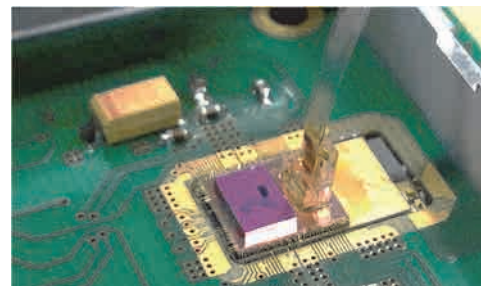
Figure 4: Packaged TPA demonstrator

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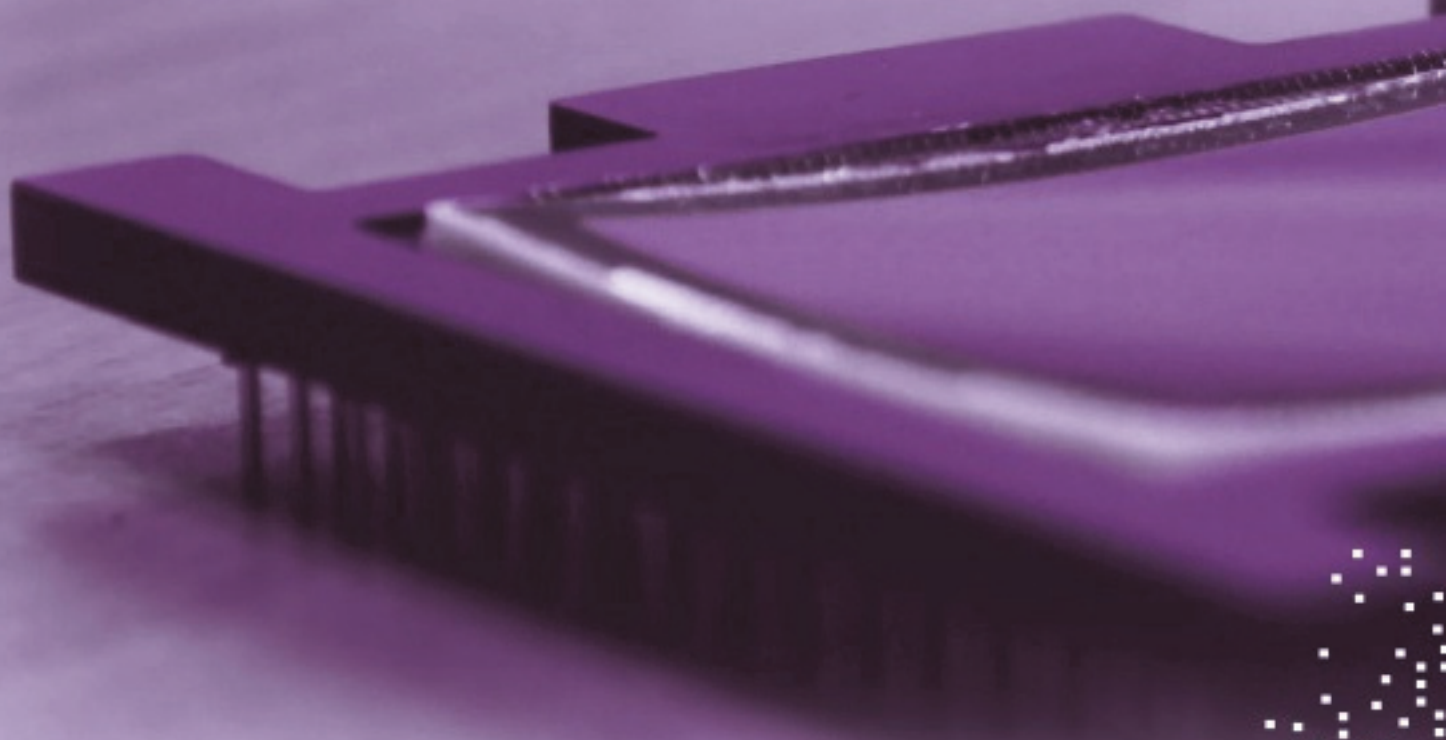
5.

SOLID STATE LIGHTING

- **Growth of high quality GaN on Si**
- **GaNoS advanced substrates**
- **LED Wafer Level Packaging**
- **High voltage LED component**

DEFECT BLOCKING DURING LATERAL EPITAXIAL OVER-GROWTH OF (10-11) GAN ON PATTERNED SILICON SUBSTRATE

AUTHORS:
M. KHOURY, P. VENNEGUES[1], M. LEROUX[1], V. DELAYE, G. FEUILLET and J. ZUNIGA PEREZ[1]

ABSTRACT:

The reduction of internal electrostatic fields in semipolar nitride heterostructures should result in higher LEDs efficacies than in polar structures. Nonetheless, epitaxial growth of these semipolar materials is carried out on hetero-substrates of particular orientations, leading to the propagation of a high density of defects in the active layers. In our case, we use silicon substrates, in the (001) 7° off orientation; the Si wafers are patterned so as to expose <111> inclined facets where epitaxial growth of c oriented GaN crystallites takes place and eventually coalesce. We introduce a novel defect reduction process, whereby growth is interrupted after deposition of the AlN buffer, followed by RIE etching. This eventually results in the blocking of the dislocations emanating from the layer/substrate facet; the mechanisms are analyzed as due to the lateral overgrowth of GaN on a Si enriched GaN semi-polar surface.

SCIENTIFIC COLLABORATIONS:[1] CNRS/ CRHEA, Sophia Antipolis, France

Context and Challenges

The presence of c-oriented internal electrostatic fields in nitrides is a major issue when dealing with polar c-orientation. Indeed, in polar quantum well nitride heterostructures, Quantum Confined Stark Effect (QCSE) results in the spatial separation of electrons and holes leading to reduced radiative recombination efficiencies. Thus surfaces misoriented with respect to the c-orientation appear as the alternative and are referred to as semi-polar surfaces (or non polar if at 90° to the c-orientation). In the particular case where silicon substrates are considered the method relies in choosing a specific wafer orientation, and then etching <111> facets. c-oriented GaN crystallites grow on the facets until coalescence occurs [1]. Nevertheless, the dislocations originating from the hetero-epitaxial interface facet thread through the epitaxial layers and eventually through the active layers. Defect reduction methods are thus highly desired. We propose a novel epitaxial process whereby dislocations are blocked at some point during growth. It relies on the precise control of the different growth steps and the use of specific surface treatments at some point during growth [2].

Main Results

Figure 1 is an SEM image of a semi polar (10-11) GaN layer grown by MOVPE onto a (001) 7°off patterned silicon substrate after coalescence of the GaN pyramids originating from two neighboring Si (111) facets.
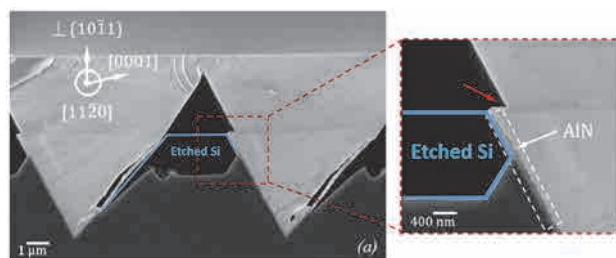

Figure 1. Cross-sectional SEM image of coalesced GaN bands on SF6 treated wafers (a) with close-up of the regrowth interface (b)

Prior to GaN growth, AlN was deposited onto the whole substrate, but only on the selected growth facet did it grow monocrystalline, since the rest of the Si substrate was covered with SiO2 leading to polycrystalline AlN growth thereon. The wafers were further immersed in HF for SiO2 removal and lifting off of the AlN polycrystalline deposition on the SiO2 mask. Subsequently, Reactive Ion Etching (RIE) was used in order to etch the thus exposed Si surfaces. Then GaN was grown on top. Note the dark line contrast and the associated kink on the back side of the pyramid. From the enlarged figure1(b),the kink and dark contrast originate from the extremity of the monocrystalline AlN layer.

Cross-sectional TEM was carried out in this region (figure 2): most dislocations originating from the epitaxial growth upon the facet, are first bent when encountering the side of the growing pyramid and, surprisingly, blocked at this dark contrast line.

Figure 2. Bright field STEM image of the regrowth interface region showing the blocking of dislocations

Through STEM EDX analysis, the presence of a high Si concentration was detected at this location but HR-STEM analysis revealed no particular structure associated to this high Si concentration. As for the optical properties, the SF6 treatment resulted in much better photoluminescence spectra with no basal stacking fault (BSF) signatures. Consequently the density of the main types of defects, i.e. dislocations and stacking faults, is drastically reduced in the semipolar epilayers following the depicted SF6 treatment.

As to the reason behind this defect reduction, we believe that it is due to epitaxial lateral overgrowth over the Si-covered semi polar surfaces. SF6 RIE silicon etching results in a reservoir of available silicon atoms that may diffuse from behind the AlN buffer (Cf fig.1) towards the GaN top semi-polar surface, impeding growth therein. If silicon diffusion does not reach the (0001) c facet of the uncomplete pyramid, nucleation occurs on the c facet and growth propagates back laterally on the Si covered semi-polar facet itself; lateral overgrowth results in dislocation bending at the regrowth interface along the growth propagation direction, hence the blocking mechanism observed. This is to be correlated to the dislocation reduction mechanisms invoked when in-situ SiN treatments are implemented for defect engineering purposes in c-oriented epitaxial growth.

Perspectives

This new defect reduction scheme will be implemented for the growth of visible LEDs on Si in the green to red domain knowing that dislocations and BSFs are a real issue for improving the efficiency of LEDs in this range. Since Si is involved in the treatment, we will also apply a simple SiN insertion during growth of the GaN layers, for implementing a simpler and reproducible process.

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A PROMISING APPROACH TO BRIDGE THE GREEN GAP: FULL INGAN STRUCTURE ON A RELAXED InGaN SUBSTRATE

AUTHORS:

A. EVEN, O. LEDOUX[1], P. FERRET, D. SOTTA[1], E. GUIOT[1], F. LEVY, I.C. ROBIN, and A. DUSSAIGNE

ABSTRACT:

A full InGaN structure is grown on InGaN relaxed pseudo-substrate from Soitec Company (InGaNOS). Due to lattice mismatch reduction between active region and substrate, we demonstrate the ability of InGaNOS to increase indium Incorporation rate. Compared to a MQW structure grown with same growth conditions on GaN substrate, a 49 nm wavelength red-shift is measured by photoluminescence (from 500 nm to 549 nm). By varying growth conditions, wavelengths up to 594 nm were reached. Therefore, combination of full InGaN structure and InGaN relaxed pseudo-substrates appears as a good way to improve long wavelength LED efficiency.

SCIENTIFIC COLLABORATIONS: [1] SOITEC Company, Bernin, Isère, France

Context and Challenges

InGaN-based blue LEDs are very efficient as their external quantum efficiency (EQE) can achieve values up to 80%. However, efficiency decreases dramatically when reaching longer wavelengths. On the other hand, amber and red spectral ranges can be covered by AlGaInP, but region from 520 to 570 nm lacks efficient emission whatever the material system. This is the so called "green gap". InGaN alloy can theoretically cover all visible range but material quality is degraded as In content increases. This limitation may have two main origins: First, the low miscibility of In in InGaN. Second, the high lattice mismatch between GaN buffer layer and $In_xGa_{1-x}N$ wells which implies a strong compressive strain in InGaN active zone. In addition, electron and hole wave function spatial overlap decreases due to increased quantum confined Stark effect (QCSE) when the well is widened or the indium content is increased. In this work, we propose to tackle lattice mismatch issue by growing a full InGaN structure on a new relaxed InGaN substrate. We will show how strain release in InGaN based MQWs is beneficial to improve the In incorporation rate

These new InGaN pseudo-substrate (InGaNOS) has been fabricated by Soitec using their Smart CutTM technology. A thin InGaN layer is transferred onto sapphire substrate. At the end of the process, this thin InGaN layer is partially relaxed.

Main Results

Full InGaN structures have been grown by metal organic vapor phase epitaxy (MOVPE) on top of InGaNOS substrate. To evaluate the impact of reduced lattice mismatch on In incorporation in InGaN quantum wells, three types of InGaNOS substrates characterized by different values of lattice parameters (a lattice parameter = 3.190 Å, 3.200 Å, and 3.205 Å) have been tested.

The grown full InGaN structure consists of a 200 nm thick $In_yGa_{1-y}N$ buffer layer followed by 5x $In_zGa_{1-z}N/In_yGa_{1-y}N$ multiple quantum wells. Same growth conditions have been kept in $In_yGa_{1-y}N$ buffer and quantum barriers in order to get same In content.

To assess the impact of a relaxed InGaN substrate on In incorporation rate, strictly same growth conditions have been applied on the three types of InGaNOS substrates. To achieve this, samples are coloaded in the same run. We applied growth conditions known to get green emission on GaN template. Samples have been compared to a reference sample with conventional structure on GaN template (i.e. with GaN instead of InGaN barriers). Note that same QW growth conditions have been used. Samples were characterized by Photoluminescence

(PL) with excitation at 405 nm. In case of green conditions presented in Fig 1., a strong redshift, as high as 49 nm, is observed for InGaNOS samples compared to the conventional structure. In between InGaNOS samples, the redshift is still important, namely 24 nm. For other growth conditions, an important redshift is also observed as InGaN *a* substrate lattice parameter is increased. In addition to green, an amber emission at 594 nm can be easily obtained using InGaNOS 3.205 Å. The different colors that were obtained on InGaNOs are shown on Fig 2.

We have demonstrated that full InGaN structure combined to InGaN relaxed substrate, namely InGaNOS, leads to an easier In incorporation owing to released strain between well and buffer layers.
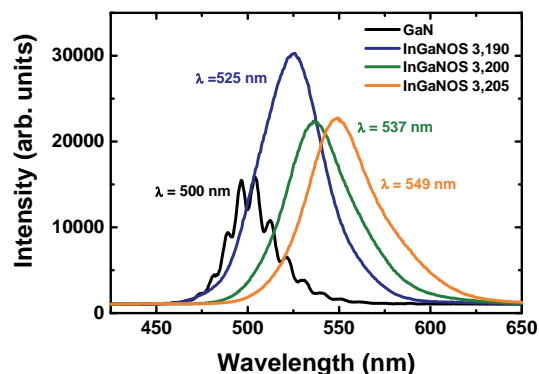

Figure 1: Photoluminescence spectra at room temperature of full InGaN structures (green conditions) grown on InGaNOS 3.190Å (blue curve), InGaNOS 3.200Å (green curve), and InGaNOS 3.205Å (orange curve). Reference sample on GaN template has been added for comparison (black curve).
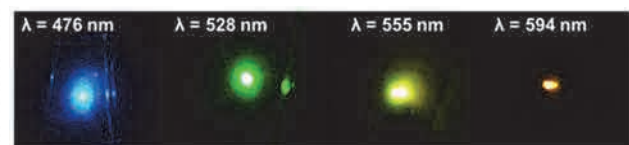

Figure 2: Photos under PL excitation by a 405 nm laser of several MQW structures grown on InGaNOS

Perspectives

The next step is to fabricate green LEDs with our technology. Promising results are expected, which will take us closer to the use of full InGaN structures on relaxed InGaN for delivering ultra-high-quality lighting and colour displays.

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NEW WAFER LEVEL PACKAGING CONCEPT FOR POWER LEDS USING TSV LAST TECHNOLOGY

AUTHORS:

M. VOLPERT, B. SOULIER, P. PERAY, N. AIT-MANI, A. GASSE, D. HENRY, C. TALLET[1], V. BEIX[1] , A. ABOULAICH[1], Z.S. CHIO[1] , J. L. DIOT[2]

ABSTRACT:

Wafer Level Packaging is a response to the critical cost and compactness issues for the LED lighting market development. Flip chip is the preferred configuration to enable easy integration where both contacts are on the same side. This work address a novel approach for LED packaging and fabrication using GaN nanowires grown on a 200 mm Silicon and a Via Last approach. Once the nanowires are fabricated a glass wafer is bonded onto the silicon wafer, the silicon is then thinned for TSV fabrication and RDL design. Both p and n contacts are designed at the backside of the chip through electroplated Cu TSVs. An aggressive aspect ratio of 5 has been achieved for the TSVs (15µm diameter, 70 µm height). The LEDs are then ready for flip chip assembly either on a board or in a carrier.

SCIENTIFIC COLLABORATIONS: [1] ALEDIA Company, Grenoble, France, [2] MINAPACK , Isère, France

Context and Challenges

Today high brightness LEDs are the leading technology for lighting applications. One of the leading factors to improve LED devices as well as to reduce the price is to work on Wafer Level Packaging. The flip chip (FC) configuration is generally preferred but the growing substrate needs to be removed by a complex Laser Lift Off process to tackle some light extraction issues. In this work [1] we present a novel approach where LEDs are first fabricated on silicon wafer by epitaxial growth of GaN nanowires. Wafers are bonded to a permanent transparent glass handle and the Si substrate is thinned down to less than a hundred µm. The N and P contacts on the back side of the LED are interconnected through Cu electroplated Through Silicon Vias (TSVs). One critical issue is the aspect ratio : 15 µm diameter / 70 µm height TSVs have been successfully manufactured to produce functional LED devices. After dicing, the LEDs are then ready for flip chip assembly either on a board or in a QFN (Quad Flat No-leads) carrier to properly handle the thermal management.

Main Results

After achieving the device front side technological steps the wafer is bonded onto a permanent glass wafer. This bonding step should ensure that the Total Thickness Variation after bonding is in the order of 5 µm so that after grinding the Si thickness remains within 5µm throughout the wafer. The used TSV-Last means that they are fabricated through the backside after wafer bonding and thinning. With this technology all the back side process must remain below 200°C which is the maximum allowed temperature for the polymer used in the bonding. The main steps are described in the figures below.
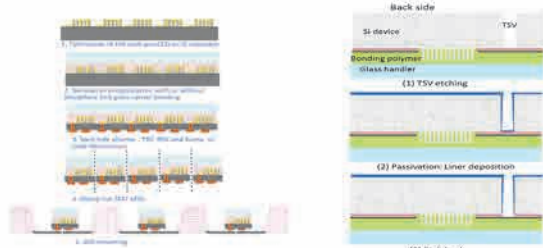

Figure 1: Description of the wafer level approach and 3 key technological steps for TSV fabrication.

TSV manufacturing has been developed on dummy samples to properly manage Si etching rate, passivation deposition within high aspect ratio TSV and etch back step to access front side metallic contact. In particular, a reduced notching has been obtained as displayed below after Cu electroplating [2].
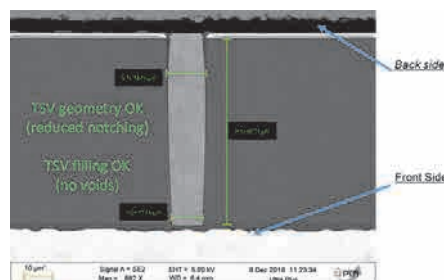

Figure 2 : Cross section view of one Cu filled TSV

After complete processing the wafer has been tested both at the wafer level and after dicing and packaging in a specially designed QFN chip carrier to help thermal management. The dicing and soldering are critical steps due to the stack of the device including a thick glass carrier, a soft encapsulation and a thin Si active substrate. They have been optimized to minimize the chipping during dicing and stress during soldering.
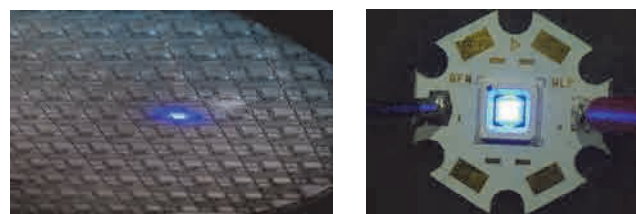

Figure 3 : Die tested directly on the wafer before dicing (left) and blue wireLED soldered in a QFN package and then on a star board (right)

After wafer level packaging, TSVs exhibit a 60 mΩ electrical resistance with a voltage strength higher than 80 V between 2 TSVs.

Perspectives

We have successfully implemented full Wafer Level Packaging technologies to produce high brightness bleu LEDs. The obtained devices can directly be soldered on a board or in package to improve thermal management. Further work will be dedicated to increase the maturity of the process as well as include phosphors within the encapsulation to produce white LEDs.

RELATED PUBLICATIONS:

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[2] M. Volpert et al "New wafer level packaging concept for power leds, 3th International Conference and Exhibition on DEVICE PACKAGING (DPC 2017), March 6-9, 2017(Fountain Hills, Arizona USA

LED LAMP WITH MINIATURIZED DRIVER AND COMPACT HIGH VOLTAGE LED COMPONENT

AUTHORS:

N. AITMANI, F. BERGER, H. BONO, M. CONSONNI, P. DEMARS, J. GARCIA, O. LADHARI, Q. LALAUZE, C. LARGERON, Y. LEE, A. VANDENEYNDE

ABSTRACT:

We worked on the design, realization, integration and characterization of a led lamp which includes a miniaturized driver and a compact led component. By combining a high chopping frequency ac-dc converter with a high voltage led component, we developed a compact and reliable led lamp architecture, which gets rid of the chemical capacitances which are currently used for this type of applications.

SCIENTIFIC COLLABORATIONS: IPDIA -MuRata company

Context and Challenges

LED lamps are currently made with a LED module and an electronic driver, which function is to convert mains voltage into a lower DC voltage. However, driver complexity and size require a large bulb volume and the need of chemical capacitances considerably degrades reliability.

In order to solve these issues, we propose a new driver topology, which combines a high frequency operating mode (through GaN component integration) and a high voltage LED component with high compactness and efficacy.

Main Results

The driver architecture which has been developed is based on a Cuk-topology AC-DC converter. In this configuration, the monitoring of the electrical network signal is done through two GaN switchs, which commutate at high frequency (1 MHz).

Indeed, a high chopping frequency operating mode allows to significantly reduce the driver passive component values: on the one hand, this leads to remove the chemical capacitances which are currently used in these drivers (increase of reliability). On the other hand, this provides the opportunity to replace them by very small capacitances, which can be integrated on silicon (increase of compactness).

Regarding the lighting part of the lamp, we developed a high voltage and compact LED component, which is directly connected to the driver architecture [1]. This 4x4 mm² component is made from a thin film flip chip (TFFC) structure and it is composed of 16 concentric anti-parallel LEDs. The innovative interconnection structure which is integrated in this component allows to considerably increase the active surface of the LED compared to standard components (efficacy gain), but it also removes the galvanic isolation issues which prevent high voltage compatibility.
Starting from commercial GaN on sapphire substrates, we developed the complete LED technological process (P electrical contact, mesa etching, and interconnection) to realize this component. Electrical characterizations done at the wafer level (before dicing) indicate that the resulting components effectively follow the electrical network signal, as each anti-parallel LED branch alternately illuminates, depending on the negative or positive value of the mains voltage.

Finally, a sapphire cutting step followed by soldering allowed to assemble the components on a silicon substrate and to connect them to the driver. A phosphor mix was also dispensed on the chip to convert a part of the emitted blue light and obtain the white color which is required for lighting applications.
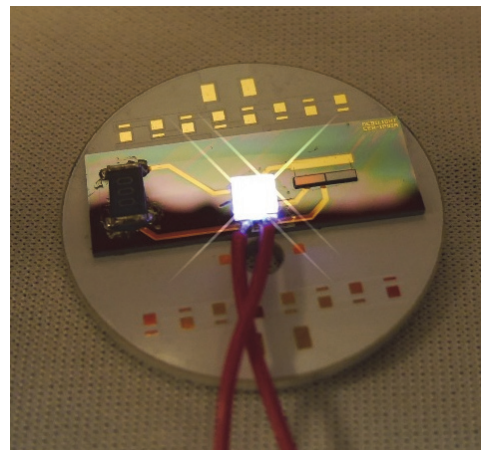

Figure 1. Picture of the LED component after the assembly on a silicon substrate.

Perspectives

The assembly of electronical and optical parts within a LED lamp evidences appreciable functioning of the different system elements, up to high chopping frequencies of 1MHz [2]. This shows the potential of these architectures for lighting applications which require a high level of compactness and reliability.
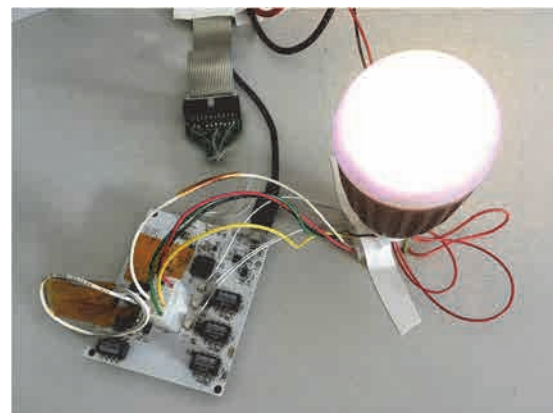

Figure 2. Picture of the LED lamp with the driver and the LED component. Power supply is done through an external control board (shown on the left).

This driver topology also remains interesting for low voltage DC supply applications, like IOTs.

RELATED PUBLICATIONS:
[1] Patent H Bono and J Garcia
[2] O Ladhari, D Bergogne, L Sterna, P Perichon, A Novel Mains Operated LED Driver Using a GaN AC Switch, PCIM conference,2017.
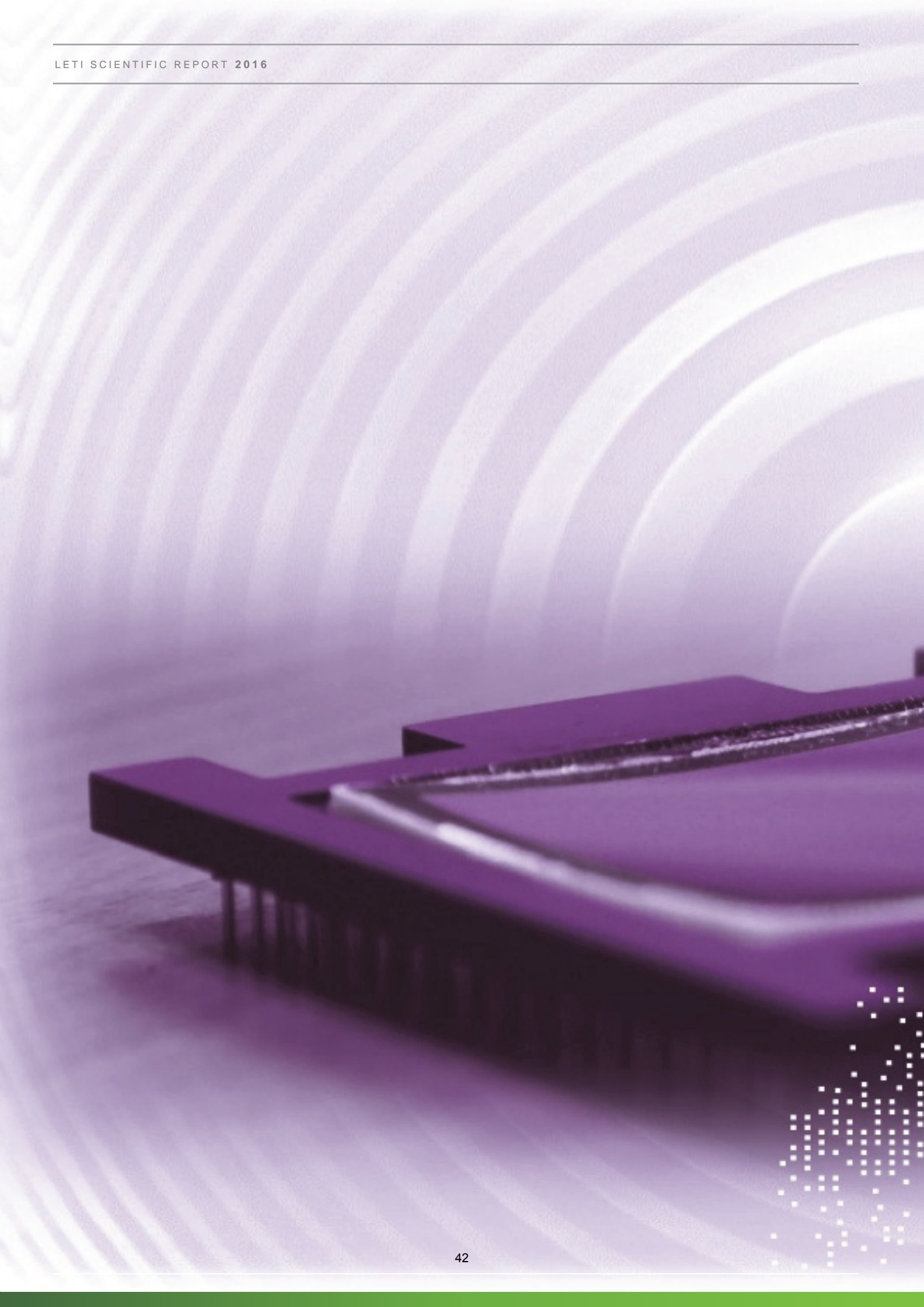
6.

DISPLAY COMPONENTS

- **GaN LED Micro-displays**

- **OLED encapsulation**

- **Near eye projection display**

ACTIVE-MATRIX, GAN MICRODISPLAY WITH WVGA RESOLUTION (873X 500 PIXELS) AT 10 µM PITCH

AUTHORS:

F. TEMPLIER, L. DUPRE, A. DAAMI, B. AVENTURIER, S. RENET, D. SARRASIN

ABSTRACT:

High-brightness GaN-based emissive microdisplays are key components for the demanding high-brightness applications. Using the microtube hybridization technology, we have developed monochrome, active-matrix, WVGA (973 x 500 pixels) GaN microdisplay prototypes with a pixel pitch of 10 µm. The microdisplays operate in full video with no major defects. They provide the highest resolution with the smallest pixel pitch. This technology is paving the way for augmented reality systems or Head-Up Displays.

SCIENTIFIC COLLABORATIONS: III-V Lab., Palaiseau, France

Context and Challenges

The growing interest for wearable devices has highlighted the need for high-performance microdisplays. Such displays are currently based on technologies such as liquid-crystal displays (reflective or transmissive), organic LEDs (OLEDs), or MEMS-based devices like micro-mirror arrays (digital light processing) and laser-beam steering (LBS). For some applications such as see-through glasses, or head-up displays, a brightness of 5000 Cd/m² or more is needed, which exceeds the possibilities of OLED microdisplays. A new type of emissive display, using GaN, has been proposed to provide a drastic improvement of the brightness while maintaining excellent contrast and compactness [1]. A key challenge is to develop active-matrix, high resolution and small pixel pitch microdisplays

Main Results

A new generation of GaN microdisplay prototypes has been developed. It is based on the hybridization of GaN array fabricated on sapphire with CMOS active matrix (Figure 1). Here we use the microtube hybridization technology, which is well suited for small pixel pitch LED microdisplays [2].
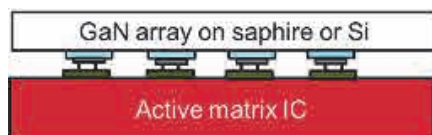

Figure 1: schematic of hybridized LED-array on Silicon circuit with microtube technology.

GaN LED arrays are made on sapphire substrates. Base wafers consist of 2-in. or 4-in. diameter sapphire with 440 nm or 525 nm LED Multi Quantum Well (MQW) InGaN/GaN epitaxial structure grown by metal-organic chemical vapor deposition (MOCVD) for blue or green emission, respectively. GaN array process consists of: (i) patterning the pixels by etching GaN stack using plasma process, (ii) depositing and patterning the P-contact metal pads and (iii) depositing and patterning the N-type contact. Also insulators are deposited to ensure electrical isolation. Finished GaN wafers have a series of LED-arrays having each 873 x 500 at 10-µm pitch. Prior to hybridization, singulation of LED-arrays is made by wafer dicing. Active-matrices for the 873 x 500 pixel displays were fabricated using conventional CMOS process on 200-mm wafers. Each pixel contact is to be connected to the Anode of the LED, while Cathode is a common connection. Microtubes were grown on

the silicon interconnect for passive displays and directly on full-CMOS wafers for active-matrix prototypes, using conventional IC process steps

GaN arrays are then hybridized onto the silicon interconnect as shown on Figure 2 which shows photograph of a series of 4 LED-arrays hybridized on silicon circuit, having each 873 x 500 pixels at 10-µm pitch. Blue and Green emitting GaN arrays have been fabricated [3].

Figure 2: Hybridized WVGA GaN microdisplays

Microdisplays have been packaged on electronic board, and the have been characterized. Nice images could be obtained (figure 3), including in full-video. This GaN display presents the highest resolution with the smallest pixel-pitch.

Figure 3: image from active-matrix WVGA GaN microdisplay

Perspectives

This first active-matrix GaN microdisplays uses an active-matrix not designed for this type of display. Therefore the brightness is presently limited. The next challenge is to design and fabricate a dedicated active-matrix to obtain high-brightness full-video GaN microdisplay.

So far, such displays are monochrome. One of the main challenges of GaN microdisplay is the color. We also focus strongly on the development of full-color GaN microdisplay

RELATED PUBLICATIONS:

1] F. Templier, J-M. Bethoux, B. Aventurier, F. Marion, S. Tirano, M. Lacroix, M. Marra, V. Verney, L. Dupré, F. Olivier, F. Berger, W. Ben Naceur, A. Sanchot, I-C Robin, M-A di Forte-Poisson, P. Gamarra, C. Lacam, M. Tordjman, "Blue and Green 10-µm pixel pitch GaN LED Arrays with very high brightness", The 22nd International Display Workshops 2015 (IDW'15), December 8-11 2015, Otsu, Japan (2015),

[2] F. Marion, F. Templier, T Catelain, F. Berger, L. Dupré, D. Henry « A room temperature flip-chip technology for high density area array micro-displays", 66th Electronic Components and Technology Conference (ECTC) 31st May – 3rd June 2016 Las Vegas (2016)

[3] F Templier, L Dupré, STirano, M Marra, V Verney, F Olivier, B Aventurier, D Sarrasin, F Marion, T Catelain, F Berger, L Mathieu, B Dupont, P Gamarra; "GaN-based emissive microdisplays: a very promising technology for compact, ultra-high brightness display systems"; Society for Information Display Conference 2016 (SID'16), 22-27 May 2016, San Francisco (2016)

A NEW PROCESS FOR ULTRA-HIGH RESOLUTION GAN MICRODISPLAYS

AUTHORS:
F. TEMPLIER, L. BENAÏSSA, A. DAAMI, B. AVENTURIER, M. CHARLES

ABSTRACT:
A new approach for fabricating high-brightness GaN microdisplays is proposed. It is based on the transfer of LED epilayer on CMOS active matrix. The growth substrate is removed, and the LED arrays is patterned directly on the CMOS wafer which provides very high resolution. The demonstration of feasibility is achieved with the production of 3 µm pixel pitch microLED arrays on silicon, the smallest pixel pitch ever reported. Such LEDs have interesting electrical characteristics. This technology is therefore very promising for fabricating high brightness, ultra-high-resolution microdisplays needed for augmented reality.

SCIENTIFIC COLLABORATIONS: III-V Lab, Palaiseau, France

Context and Challenges

The growing interest for wearable devices has highlighted the need for high-performance microdisplays. Self-emitting devices such as OLED microdisplays are attractive, providing excellent image quality and low power consumption, but they have some limitations in brightness. Inorganic GaN LED based arrays are a very promising technology for very high brightness microdisplay. Such microdisplays can be fabricated either via (i) hybridization of a GaN array on sapphire with CMOS active matrix, or (ii) 3D parallel integration of GaN LEDs on a CMOS circuit. Based on the first approach, using microtube hybridization technology we could develop GaN prototypes with a pixel pitch as small as to 10 µm [1]. Using the 3D parallel integration approach, a pixel-pitch of 10 µm pitch has been also demonstrated.However, for high-brightness LED microdisplays, there is a need of a much smaller pixel pitch, typically 5 µm or even 2 µm. Therefore, a new integration strategy for fabricating these GaN LED microdisplays is required.

Main Results

We propose a new approach for fabricating high-brightness LED microdisplays (Figure 1). A GaN LED epilayer is grown on a substrate. This stack is transferred and bonded onto a CMOS active-matrix (b), and the first substrate is removed (c). The LED array is then patterned and fabricated directly on the CMOS wafer (d). The LED arrays are fabricated directly on the CMOS wafer, and can take advantage of the very small feature size available using the latest semiconductor manufacturing techniques. Therefore, with this approach very small pixel-pitch can be achieved.

To evaluate the feasibility of this approach, we have bonded GaN-based LED layers grown on 200 mm silicon wafers onto silicon wafers coated with metal instead of CMOS wafer. The rest of the process was the same. Matrices of GaN microLEDs with different size and spacing were patterned using classical lithography and dry etching. No post-metallization has been applied on these first samples. Figure 2 shows an SEM image (right) of a 2-µm size, 3-µm pitch blue microLED array. Each microLED emits bright blue light (left).

Figure 1: schematic of the new fabrication process

Figure 2: blue microLED array with 3-µm pitch.

This work demonstrates the feasibility of high-resolution and very-small pixel pitch high-brightness GaN microdisplays. The achieved pixel-pitch of the GaN microLED arrays, 3 µm, is the smallest ever reported to the author's knowledge. Also, using this novel process integration, the devices are entirely fabricated using a CMOS line, which simplifies significantly the supply chain and paves the way for future low cost, mass production of GaN-based microdisplays.

Perspectives

The proof-of-concept of the new technology has been made. Now work will focus on developing a full microLED process, including insulation between pixels, top contact metallization and optimized device architecture. This technology is therefore very promising for fabricating high brightness, ultra-high-resolution microdisplays needed for augmented reality.

RELATED PUBLICATIONS:
[1] F. Templier, J-M. Bethoux, B. Aventurier, F. Marion, S. Tirano, M. Lacroix, M. Marra, V. Verney, L. Dupré, F. Olivier, F. Berger, W. Ben Naceur, A. Sanchot, I-C Robin, M-A di Forte-Poisson, P. Gamarra, C. Lacam, M. Tordjman, "Blue and Green 10-µm pixel pitch GaN LED Arrays with very high brightness", The 22nd International Display Workshops 2015 (IDW'15), Invited talk, December 8-11 2015, Otsu, Japan (2015),
[2] F. Templier, L. Benaïssa, I. Degirmencioglu, M. Charles and S. Tirano, "A new Approach for Fabricating High-Brightness GaN LED Microdisplays with High Resolution and Very Small Pixel-pitch", Invited Talk, best paper award, The 23nd International Display Workshops 2016 (IDW'16), December 7-9th 2016, Fukuoka, Japan (2016)
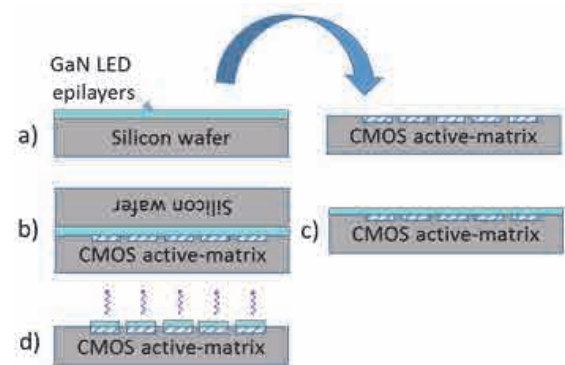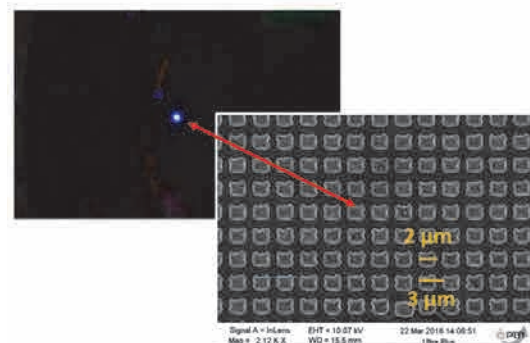
DEFECT ANALYSIS IN LOW TEMPERATURE ALD-DEPOSITED AL_2O_3 AND PVD-DEPOSITED SIO BARRIER FILMS AND COMBINATION OF BOTH TO ACHIEVE HIGH QUALITY MOISTURE BARRIERS

AUTHORS:

T. MAINDRON, T. JULLIEN and A. ANDRE

ABSTRACT:

Al_2O_3 films (20 nm, Atomic Layer Deposition, ALD) and SiO films (25 nm, Physical Vacuum Deposition, PVD) single barriers as well as hybrid barriers of the kind Al_2O_3/SiO or SiO/Al_2O_3 have been deposited onto single 100 nm thick tris-(8-hydroxyquinoline) aluminium (AlQ_3) organic films made onto silicon wafers. Defects in the different barrier layers could be easily observed as non-fluorescent AlQ_3 black spots, under UV light on the different systems stored into accelerated aging conditions (85 °C/85% RH, ~ 2000 h). Using the organic AlQ_3 sensor, the different observations made in this work give a quantitative comparison of defects occurrence and growth in ALD-deposited versus PVD-deposited oxide films as well as in their combination PVD/ALD and ALD/PVD.

Context and Challenges

The Holy Grail for encapsulation of fragile organic optoelectronic devices (OLED, OPV, OTFT) consists in the addition of vacuum deposited thin mineral barrier like oxides, nitrides or oxi-nitrides layers directly onto the organic circuit. The technology basics is somehow similar to the one encountered in the world of food packaging where Al, Al_xO_y or SiO_x barrier materials are vacuum-deposited onto plastic sheet surfaces as barrier layers against moisture and oxygen. The main challenge today for organic optoelectronics is to achieve TFE with Ultra High Barrier (UHB) grade in order to allow a robust encapsulation with Water Vapour Transmission Rate (WVTR) ~ 10^{-6} g/m²/day necessary for OLED devices. Such achievements will open the way to the realization of lightweight, flexible OLED displays. In this work, we have studied the defect occurrence and growth mechanisms of Al_2O_3 ALD and SiO PVD barrier layers as well as combination of both SiO/Al_2O_3 and Al_2O_3/SiO using a single AlQ_3 fluorescent sensor as an alternative to the full OLED component [1].

Main Results

It has been observed that all devices containing an Al_2O_3 layer present a lag time τ from which defect densities of the different systems start to increase significantly. This is coherent with the supposed pinhole-free nature of fresh, ALD-deposited, Al_2O_3 films. For t>τ, the number of defect grows linearly with storage time. For device with the single Al_2O_3 barrier layer, τ has been estimated to be 64 h. For t>τ, the defect occurrence rate has been calculated to be 0.268 /cm²/h. Then a total failure of fluorescence of the AlQ_3 film appears between 520 h and 670 h indicating that the Al_2O_3 barrier has been totally degraded by the hot moisture. Interestingly, the device with the hybrid barrier SiO/Al_2O_3 shows the same characteristics as the device with the single Al_2O_3 barrier (τ =59 h; 0.246 /cm²/h for t>τ), **indicating that Al_2O_3 ALD is the factor that limits the performance of the barrier system when it is directly exposed to moisture condensation**. At the end of the storage period (1410 h), the defect density for the system with the hybrid SiO/Al_2O_3 barrier is 120 /cm². **The best sequence has been obtained when Al_2O_3 is passivated by the SiO layer (Al_2O_3/SiO)**. In that case, a large lag time of 795 h and a very low defect growth rate of 0.032 /cm²/h (t>τ) have been measured. At the end of the storage test (2003 h), the defect density remains very low, only 50 /cm². On the other hand, the device with the single PVD-deposited SiO barrier layer shows no significant lag time (τ ~ 0) and the number of defects grows linearly from initial time with a high occurrence rate of 0.517 /cm²/h. This is coherent with the pinhole-full nature of fresh, PVD-deposited, SiO films. At intermediate times, a second regime shows a lower defect occurrence rate of 0.062 /cm²/h. At longer time span (t > 1200 h), the SiO barrier begins to degrade and a localized crystallization onto the oxide surface, giving rise to new defects (occurrence rate 0.461 /cm²/h), could be observed. At the end of test (2003 h), single SiO films show a very high defect density, 600 /cm². Interestingly, the SiO surface in the Al_2O_3/SiO device does not appeared crystallized at high time span, suggesting that the crystallization observed onto SiO surface in AlQ_3/SiO device rather originates into the AlQ_3 layer, due to high humidity ingress on the organic layer through SiO pinholes. This has been confirmed by AFM surface imaging onto AlQ_3/SiO surface showing a central hole in the crystallization zone with a 60 nm depth, deeper than SiO thickness (25 nm).

Device	A1	A2	B1	B2
Fluorescent sensor on Silicon wafer	AlQ3 (100nm)	AlQ3 (100nm)	AlQ3 (100nm)	AlQ3 (100nm)
Barrier layer 1	SiO (25nm)	Al2O3 (20nm)	SiO (25nm)	Al2O3 (20nm)
Barrier layer 2	-	-	Al2O3 (20nm)	SiO (25nm)
Final defect density in cm^{-2}	600	Very high	120	50
Time at end of storage test	2000	670	1400	2000

Table 1: Description of device architectures studied in this work as well as the black spot densities at the end of storage test

Perspectives

Using the organic AlQ_3 sensor, the different observations made in this work give a quantitative comparison of defects occurrence and growth in ALD-deposited versus PVD-deposited oxide films as well as in their combination PVD/ALD and ALD/PVD. It has been seen that the Al_2O_3 layer, deposited at low temperature ALD, must be passivated by a moisture-stable layer, in that case a single PVD-deposited SiO layer. This strategy is helpful for the improvement of atmospheric barrier layer properties as well for the understanding of atmospheric barrier layer behavior. New scenarios are on the way at DOPT/SNAP/LVE in order to simplify the process to make the double barrier by using a moisture stable, ALD-deposited, TiO_2 layer as Al_2O_3/TiO_2 or single TiO_2.

RELATED PUBLICATIONS:

[1] T. Maindron, T. Jullien and A. André , *Defect analysis in low temperature atomic layer deposited Al2O3 and physical vapor deposited SiO barrier films and combination of both to achieve high quality moisture barriers J. Vacuum. Science and Technology A 34 (3)*

LENS-FREE NEAR-EYE INTRAOCULAR PROJECTION DISPLAY

AUTHORS:
C MARTINEZ, V KROTOV and D FOWLER

ABSTRACT:
We present a concept for a lens-free near-eye display based on an association of waveguides, grating couplers and pixelated holograms. The imaging behavior uses multiple beam interference to produce an image on the retina. A first validation of the diffractive phenomenon is proposed.

SCIENTIFIC COLLABORATIONS: Univ. Haute Alsace LMIPS, Mulhouse, France.

Context and Challenges

Among the various technological solutions studied today for Augmented Reality (AR), the ability to superimpose information on the user's field of view has drawn particular interest. In this domain, near-eye display solutions allow for the use of mobile AR devices such as see-through glasses [1] or peripheral relay displays [2]. These solutions are however still constrained by technical limitations linked to the physiology of the eye. Researchers agree that disruptive technologies are needed to overcome these limitations to allow adequate visual resolution and field of view without severe constraints on the eye location. We present a patented concept of a lens-free near-eye display that could offer a wide viewing angle and eye box in a see-through design [3]. A first evaluation of the diffractive phenomenon that underpins our concept has been analyzed theoretically and experimentally.

Main Results

When looking at an image at a large distance, each point of the scene impacts the eye as a parallel wavefront characterized by its wave vector k_p (figure 1a).

Our concept is based on coherent multi beam emitters. In this design a set of emitting pixels generates multiple directive spherical wavefronts k_s. If the wavefronts are phase adjusted, multiple interference can focus the beams onto a single image pixel (figure 1b): the display produces an image without optics.
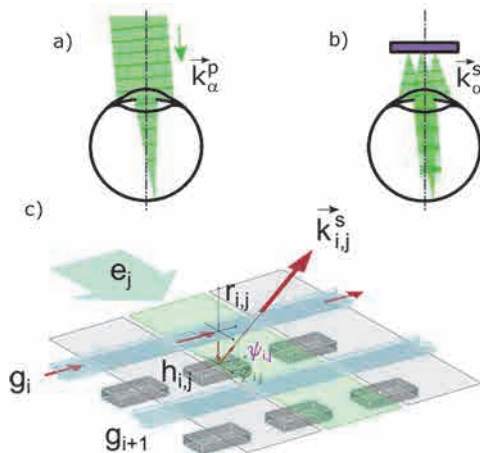

Figure 1: a) vision of point at infinity, b) concept of multiple beam intraocular focusing, c) principle of our device

To realize this non-conventional display we propose the use of switchable grating couplers to activate the beam extraction from a given waveguide g_i at a grating $r_{i,j}$ location activated by e_j electrode (figure 1c). A holographic element $h_{i,j}$ is used to redirect the extracted beam toward the given angular coordinate. Due to the small size of the emitting zone, the extracted beam is associated to a spherical directive beam of wave vector $k_{si,j}$.

We propose an initial analysis of our concept of self-focusing through theoretical and experimental evaluation of the multiple beam interferences. To demonstrate the concept we study a distribution of apertures in a metallic layer [4,5]. We image the diffraction pattern of an incident coherent wavefront after passing through an optical system that mimics the eye (figure 2a).
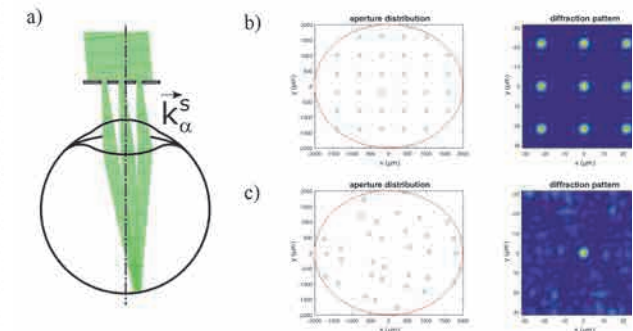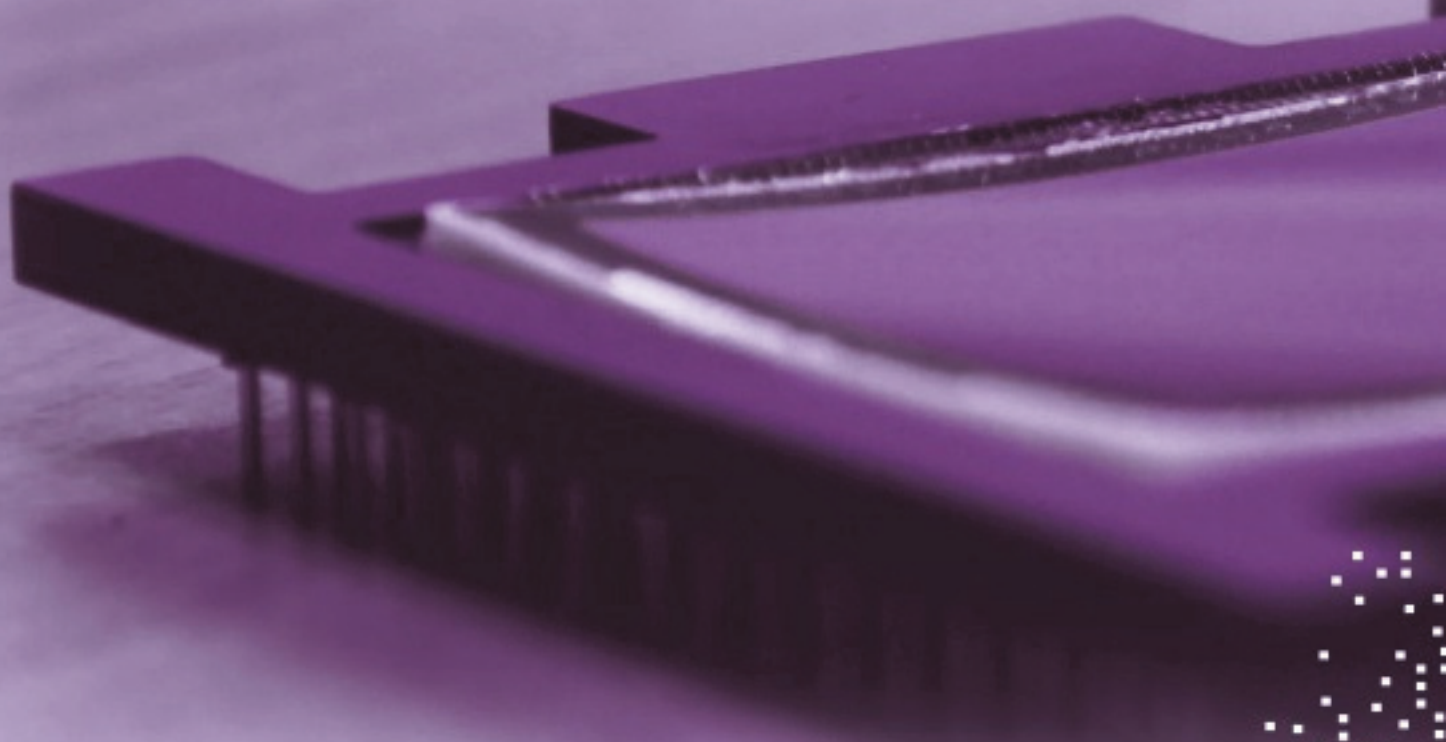

Figure 2: Theoretical simulation of the self-focusing effect a) principle of the set-up, b) and c) diffraction of a periodic and random aperture distribution.

Theoretical simulation and experimental measurements of the diffractive behavior of various aperture distributions has been carried out. Figure 2b shows a quadratic aperture distribution that generates a focus near the eye resolution. In this case the periodic aperture distribution induces multiple focus orders that prevent imaging on the retina. Figure 2c shows a quasi-random distribution that allows a focusing effect and avoids multiple focusing orders. Theoretical simulations have been validated experimentally. We have now to find the best aperture distribution compromise for focus quality and device manufacturability..

Perspectives

Our non-conventional display concept can be integrated on a glass substrate to give an overall device transparency. This very ambitious design is based on various micro/nano technological processes developed in our Optics and Photonics Division (surface micro structuration, integrated photonics, …. The next step will concern the development of a holographic printer to validate the concept of self-focusing towards intraocular image formation.

RELATED PUBLICATIONS:
[1] Lorem ipsum dolor sit amet, consectetur adipiscing elit. Sed non risus. Suspendisse lectus tortor, dignissim sit amet, adipiscing nec, ultricies sed, dolor. Cras elementum ultrices diam. Maecenas ligula massa, varius a, semper congue, euismod non, mi. Proin porttitor, orci nec nonummy molestie, enim est eleifend mi,
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7.

OPTICS AND NANOPHOTONICS

- Optimization of photonic micro-devices
- Topological insulator structures
- Curved visible imager

METAMODELING AND OPTIMIZATION OF PHOTONIC MICRO-DEVICES

AUTHORS:

C. DURANTIN, K. HASSAN, A. GLIERE

ABSTRACT:

Designers of photonic micro-devices increasingly rely on numerical optimization. However, the physics-based model needed to optimize the devices is often too compute-intensive to be directly integrated into the optimization algorithm. Resorting to metamodels constitutes an attractive way to overcome this difficulty. The metamodel is first built from a reduced number of high fidelity calculations, corresponding to a well-chosen sampling of the parameter space. It is then used to quickly evaluate the response of the system to other sets of parameters. Recently, (i) a multifidelity metamodeling method based on Radial Basis Function was proposed and compared to the classical co-kriging method and (ii) a metamodel-based optimization was performed on a photonic device and verified experimentally.

SCIENTIFIC COLLABORATIONS: ACUMES team (INRIA Sophia Antipolis), Chaire OQUAIDO (EMSE)

Context and Challenges

Two challenges, identified in the context of photonic micro-devices, have been addressed recently at CEA-LETI. First, the cost of the high fidelity model often limits the ability to create an accurate enough metamodel. If, at the same time, models having different levels of complexity are available and can be hierarchically ranked in terms of accuracy, a multifidelity approach can be implemented. Second, the robustness of the optimized micro-devices towards environmental changes or fabrication uncertainties is highly desirable and should be directly accounted for in the optimization algorithm.

Main Results

Multifidelity surrogate modeling aims at efficiently combining information coming from different levels of approximation in order to build a metamodel at a reduced cost. During the design of a miniaturized photoacoustic cell, the two models that can be combined are first the accurate but expensive full linearized Navier-Stokes equations and second the simpler acoustic equation. In this context, an original multifidelity metamodel based on radial basis function (RBF) and the corresponding adaptive sampling algorithm have been implemented [1, 2]. It has been shown that (i) the multifidelity approach helps saving computation time (Fig. 1) and that (ii) the new RBF-based multifidelity metamodel constitutes an interesting alternative to the widely used co-kriging approach.
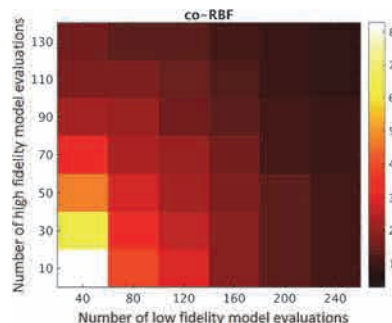

Figure 1: Mean prediction error (%) of the RBF-based multifidelity metamodel as a function of the number of high and low fidelity model evaluations on a test case.

Adiabatic power splitters constitute an elaborated function used in photonic integrated circuits to share efficiently optical power between two output waveguides. Their design is constrained by the adiabaticity criterion which is ensured by a long coupling zone. A new metamodel based optimization method has been devised in order to obtain a compact and wideband coupler [3, 4]. The robustness to wavelength has been ensured by a genetic multi-objective optimization algorithm and a worst case scenario has been assumed. The optimal device has been designed at a reduced computational cost and then fabricated and characterized. A clear improvement of bandwidth and robustness over conventional designs has been observed (Fig. 2).
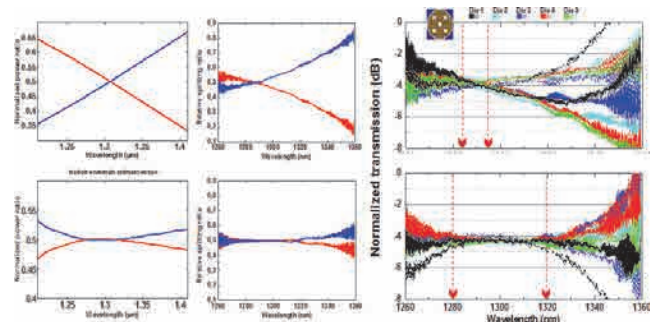

Figure 2: From left to right: simulated and measured power splitting versus wavelength and normalized transmission spectra of both outputs over 5 dies chosen at different locations over a wafer. Conventional design (top) and optimized coupler (bottom).

Perspectives

Beyond spreading the metamodeling approach into the design process of CEA-LETI photonic devices, the research currently progresses in several directions. First the robust design framework is improved by combining a multi-gradient descent algorithm with a genetic algorithm and implementing other robust design strategies. Second, the metamodeling algorithms are extended to the case of mixed problems involving both continuous and discrete variables.

Developments are also active in the domain of shape and topological optimization, where the device geometries are no longer parameterized but completely free and "designed by specifications".

RELATED PUBLICATIONS:

[1] C. Durantin, J. Rouxel, J.-A. Désidéri, and A. Glière, "Optimization of a photoacoustic gas sensor using RBF-based multifidelity metamodeling," ECCOMAS Hersonissos, Greece, 2016.

[2] C. Durantin, J. Rouxel, J.-A. Désidéri, and A. Glière, "Multifidelity surrogate modeling based on Radial Basis Functions," accepted for publication by Structural and Multidisciplinary Optimization, 2017.

[3] K. Hassan, C. Durantin, V. Hugues, B. Szelag, and A. Glière, "Robust silicon-on-insulator adiabatic splitter optimized by metamodeling," Applied Optics, vol. 56, no. 8, pp. 2047–2052, 2017.

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ROOM TEMPERATURE SPIN TO CHARGE CONVERSION IN HgTe/CdTe 3D TOPOLOGICAL INSULATORS

AUTHORS:

C. THOMAS, Y. FU [1], P. NOEL [1], L. VILA [1], J.P. ATTANE [1], S. GAMBARELLI [1], T. MEUNIER [2] and P. BALLET

ABSTRACT:

We present the first spin-to-charge conversion experiment on HgTe/CdTe 3D topological insulator structures. Spin injection occurs from a ferromagnetic NiFe directly deposited on the MBE-grown stack. Spin currents are converted into charge currents at the topological interface where 2D electronic transport occurs with direct evidence of the spin-to-momentum locking property expected for this class of topological material. The spin-to-charge conversion factor is found to be far superior to conventional spin-Hall bulk materials making HgTe a very attractive candidate for novel spintronic applications.

SCIENTIFIC COLLABORATIONS: [1] CEA-INAC-SPINTEC, Grenoble, France and [2] CNRS/ Neel institute, Grenoble, France

Context and Challenges

Topological insulators (TI) are generating a growing interest for spintronics as spin and momentum are locked on their surface states. Indeed, an electron current flowing on topologically protected surfaces turns into a spin-polarized current, thus generating a non-zero spin angular momentum. Spin injection and spin to charge conversion in these peculiar systems are therefore to be investigated to promote and implement topological insulators into various spintronic devices.

Main Results

The MBE growth optimization and HgTe/CdTe topological interface characterization are described elsewhere [1-3] and associated magneto-transport investigation has demonstrated state of the art surface states Dirac fermion electronic transport in 3D structures [4]. Spin-pumping measurements have been performed on samples covered by a 20nm-thick NiFe ferromagnetic layer and brought into ferromagnetic resonance (FMR) by the combination of a radio-frequency (hrf) field transverse to an external static magnetic field H (see figure 1).
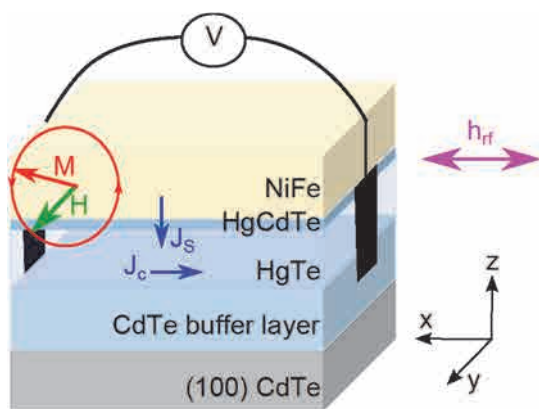

Figure 1: Scheme of the sample and set-up for spin pumping into HgTe TI via ferromagnetic resonance of a NiFe layer. A pure spin current Js is injected on HgTe surface states generating a transverse charge current Jc.

The FMR signal is reported in fig.2a and its narrow linewidth

witnesses the quality of the NiFe layer deposition and the low roughness of the whole stack estimated to about 1nm from X-ray reflectometry. The reversibility of the dc-voltage measurement with magnetic field (fig.2-b) is a direct proof of the spin to charge conversion.
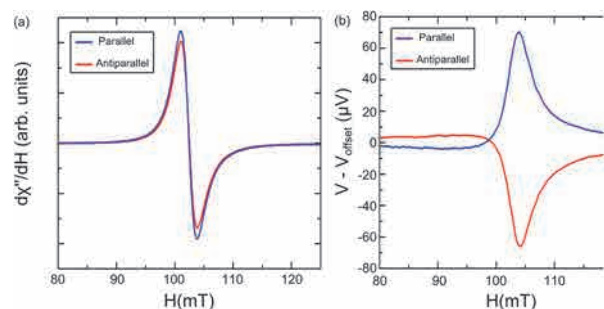

Figure 2: FMR signal for both parallel and antiparallel directions of the magnetic field (a), dc-voltage measurement at 200mW in both directions (b).

For 2D transport arising on the surfaces of a 3D TI, the conversion between spin and charge currents is governed by the Inverse Edelstein Effect (IEE) which represents the counterpart of the Inverse Spin Hall Effect in the case of bulk electronic states. The efficiency of the IEE is measured through the ratio between injected spin current (3D) and generated interfacial charge current (2D) resulting in the definition of a conversion length (1D): λIEE.

With room-temperature λIEE exceeding 2nm in our HgTe/CdTe topological structures, this material system greatly surpasses bulk spin-Hall metals and opens the way toward building more efficient spintronic devices.

Perspectives

These preliminary and very encouraging results promote HgTe 3D-TI as a new spintronic material with potential specific properties linked to its topological surface states. To further understand and optimize spin-to-charge conversion in this system, spin-pumping experiments will be conducted on series of samples with various HgTe thickness and spin-injection barrier. More importantly, the direct Edelstein effect corresponding to the charge to spin conversion will be realized in order to design new spintronic building blocks such as spin-transfer or spin-orbit torque devices.

RELATED PUBLICATIONS:

[1] P. Ballet, C. Thomas, X. Baudry, C. Bouvier, O. Crauste, T. Meunier, G. Badano, M. Veillerot, J.P. Barnes, P.H. Jouneau and L.P. Levy, " MBE growth of strained HgTe/CdTe topological insulator structures", J. Electron. Mater. 43, 2955 (2014)

[2] C. Thomas, X. Baudry, J.P. Barnes, M. Veillerot, PH. Jouneau, S. Pouget, O. Crauste, T. Meunier, LP. Lévy and P. Ballet, "MBE growth and interfaces characterizations of strained HgTe/CdTe topological insulators", J. Cryst. Growth 425, 195 (2015)

[3] B. Haas, C. Thomas, PH. Jouneau, N. Bernier, T. Meunier, P. Ballet and J-L. Rouvière, "High Precision Strain Mapping of Topological Insulator HgTe/CdTe", Appl. Phys. Lett. 110, 263102 (2017)

[4] C. Thomas, O. Crauste, B. Haas, P.-H. Jouneau, C. Bauerle, L.P. Lévy, E. Orignac, D. Carpentier, P. Ballet, and T. Meunier, "Revealing topological Dirac fermions at the surface of strained HgTe via Quantum Hall transport spectroscopy" submitted to Phys. Rev. Lett (2017)

HIGH RESOLUTION COMPACT IMAGING SYSTEMS BASED ON EXISTING CURVED DETECTORS

AUTHORS:

C GASCHET, B CHAMBION, S CAPLET, G MOULIN, S GÉTIN , A VANDENEYNDE, W JAHN[1], D HENRY, E HUGOT[1]

ABSTRACT:

We present high performance imagers based on our current know-how in curved detectors manufacturing for VIS or NIR applications. These extremely compact systems are preparing the future of curved imagery.

SCIENTIFIC COLLABORATIONS: [1]CNRS/ Laboratoire d'Astrophysique de Marseille (LAM), France

Context and Challenges

A huge interest has grown for curved electronics, particularly for opto-electronics systems [1]. Indeed, wide field optical systems always have remaining aberrations in the field, specifically for off-axis rays with Petzval Field Curvature and astigmatism aberrations. Usually, these aberrations are corrected with additional lenses acting as field flatteners, with the aim of coinciding the focal plane array with a flat sensor. By directly curving the focal plane array, the field curvature is directly compensated, leading to simpler systems with increased performances.

Main Results

Packaging: The mechanical behavior of curved sensors has been modeled, using FEM. A parametric study is performed to investigate the influence of 1rst order parameters on the minimum allowable radius of curvature for the plate. These parameters are the edge length L of the square sensor with a range value from 3 mm to 45 mm, the thickness t of the sensor with a range value from 10 to 400 μm and the radius of curvature. Results of the minimum allowable radius of curvature for a silicon plate are plotted on Figure 1.
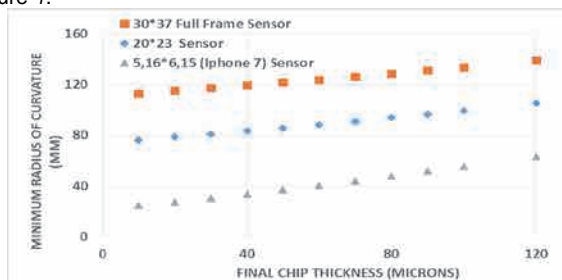

Figure 1: Results of the parametric study conducted for (100)-oriented silicon plate in spherical shape, for 3 chip sizes.

This model has been validated with experimental results. Finally, we fully packaged a 30x37x0.1 mm CMOS image sensor with a radius of curvature of 150mm (Figure 2**:**).
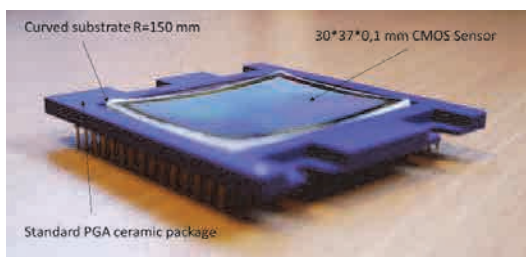

Figure 2: Prototype with a 30*37*0.1 mm sensor, using a standard ceramic package. Spherical radius on curvature = 150mm.

Electro-optical characterization: In flat position, we recorded a dark current at 25 Digital Number per second (DN/s). We did the same for several spherical radius of curvature (up to R= 550mm) and a [18-28] DN/s dispersion were found. This point indicates that there is no significant curvature impact on the electro-optical response, and the sensor keeps its functionality while curving.

Overall system approach: The monocentric system, which has a curved sensor, combines compactness, wide Field of View (more than 120°), high resolution and large light collection [2]. But the technical problem of this monocentric system is the highly curved focal plane. And according to mechanical limits presented before, this type of sensor is impossible. We studied modifications on this monocentric system to provide an optical system in accordance with the mechanical limits. In this way, we founded a new optical architecture (Figure 3), which is made up of a triplet and three single lenses with an aperture stop placed in front of the lenses block. Thus this system is totally asymmetrical, contrary to prior studied systems.
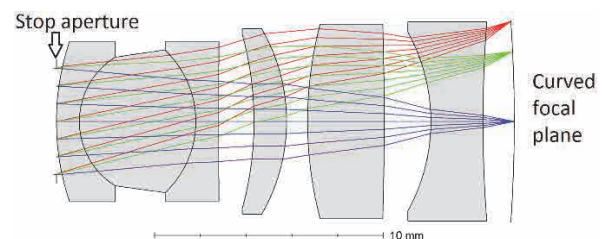

Figure 3: Schematic representation of CEA-LETI optical system new architecture equipped with a spherically curved image sensor.

This system has a large Field of View (FOV), between 40° and 50°. Sensors are also curved at a radius of curvature compatible with the mechanical limits presented in 2. Moreover, the new architecture provides a great compactness for a design without aspheric surfaces and high resolution: 20 mm in axial length from stop aperture to the sensor. This architecture is made for low cost applications, when high resolution and compactness are needed. Compared to a flat sensor design, with the same focal, field of view, and resolution, we obtain a gain of compactness of about 50%.

Perspectives

LETI proposed a curved sensor's technology, with its mechanical limits and electro-optical characterizations. Based on sensor mechanical results, we found a new optical architecture, providing compactness and high resolution. This system is more performant than current technology without curved sensors, demonstrating the interest of this new technology for future optical design generations.

RELATED PUBLICATIONS:

[1] B Guenter et al., "Highly Curved Image Sensors: A Practical Approach for Improved Optical Performance," Optics Express 25, no. 12 (June 12, 2017): 13010.

[2] I Stamenov et al., "Optimization of Two-Glass Monocentric Lenses for Compact Panoramic Imagers: General Aberration Analysis and Specific Designs," Applied Optics 51, no. 31 (2012): 7648–61.Braunschweig, Germany, June 5-9, 2017.
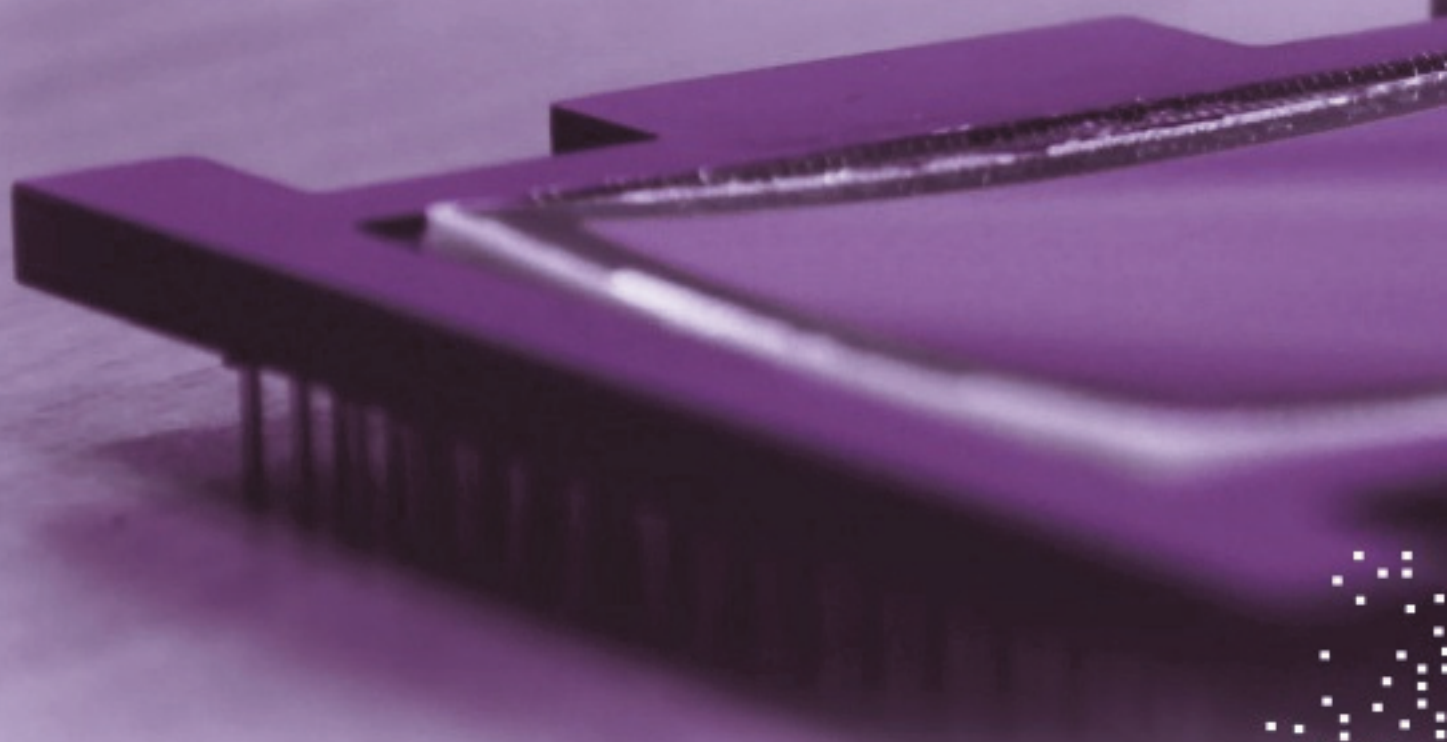
8.

PhD DEGREES AWARDED IN 2016

- **Alexis ABRAHAM**

- **Jocelyn BERTHOZ**

- **Florian DUPONT**

- **Hélène DUPREZ**

- **Thomas FERROTTI**

- **Etienne FUXA**

- **Marc GUILLAUMONT**

- **Michel KHOURY**

- **Anthony LEFEBVRE**

- **Nicolas MANTE**

- **Candice THOMAS**

Alexis ABRAHAM

DEVELOPMENT OF LOW POWER CONSUMPTION SILICON OPTICAL MODULATORS FOR THE NEXT GENERATION OF OPTICAL INTERCONNECTS

The subject of my PhD is focused on one of the basic block of the optical transmitter for high-speed links: the electro-optical modulator, a key component which converts an electrical signal into an optical signal. It should support high speed transmission, have low losses, and have low power consumption. During my PhD, the improvement of these performances was made by three different ways.

By integrating fabrication effects in the existing optimization process, more reliable numerical results were obtained. The key point of this approach is the successful comparison between experimental characterizations and numerical simulations of two types of PN modulators. A substantial part of my PhD was also focused on the development of new modulators with high efficiency, based on vertical capacitive junctions. The use of dedicated numerical tools allows us to optimize these components, and find a functioning point regarding the targeted specifications. A new fabrication process has been established, and we have extracted useful information from the first run of fabrication.

Then, a comparative study between most of modulators reviewed during this PhD was performed. The results allow us to determine which configuration has the best performances, and to generate compact models. These models can optimize the component in a drastically reduced time, and can be integrate in a more complex circuit.

Jocelyn BERTHOZ

PERFORMANCE CHARACTERIZATION AND MODELING OF SMALL PITCH IR COOKED FOCAL PLANE ARRAYS

The purpose of this thesis is to evaluate the electro-optical performances of infrared detectors based on photodiodes. The performances studied are the quantum efficiency and the modulation transfer function. The problematic is to understand which phenomenon impacts these performances for reducing the development time. In order to answer this problematic, this study is made through measurements and numerical simulations.

Firstly, electro-optical performances are discussed with their link to the infrared market. Then, measurements and numerical computations are made in order to explain the reasons of the actual values. Finally, by computation, advance technologies are analyzed and compared.

Florian DUPONT
CRYSTALLINE NUCLEATION OF GAN NANOWIRES ON CONDUCTIVE SUBSTRATES, FOR LED APPLICATIONS

GaN-based light-emitting diodes (LEDs) have seen a tremendous increase in interest in the past few years, as their high efficiency allows for important energy savings. However, their penetration in the general lighting market is still limited as a result of their relatively high production costs.

Realizing LEDs on 8in silicon substrates could allow for a 75% reduction to the production costs of standard LEDs (source: Aledia).

In order to realize LED structures on 8in silicon substrates, 2 major roadblocks exist. Firstly, the coefficient of thermal expansion of Si, which is very different to that of GaN, causes cracks after the epitaxy of the layers in standard architecture. This can be solved using 3D core-shell microwire geometry, which is the geometry that was chosen for this PhD thesis.

The second major roadblock is the high reactivity of Si substrates. In fact, due to the reactivity of silicon with the gallium precursor during the GaN MOVPE growth, a buffer layer is needed. In the state of the art, the most commonly used buffer layer is AlN. However, this material is insulating and does not allow the current to flow through the silicon substrate to the LED. The goal of this PhD was to identify and develop a conductive buffer layer to overcome the limitations of AlN.

First, a new and innovative conductive material, suitable for the use as a buffer layer, was identified. The growth of GaN microwires onto a thin film made of this was demonstrated; thus, overcoming the second roadblock. However, the uniformity of the dimensions of the wires was found to be a new limiting factor for a complete 3D-LED-on-Si process. A new architecture, built on the basis of the conductive material, was then developed, and a very-high-uniformity GaN wire array on a conductive material was demonstrated. This architecture, and the corresponding processes, have been implemented by Aledia for the production of its 3D-LED-on-Si as it produces a highly satisfying uniformity, even over a large diameter Si substrate. These PhD results open the way for an innovative low-cost LED manufacturing process, and 6 patent requests were filed as a result.

Hélène DUPREZ
FROM DESIGN TO CHARACTERIZATION OF HYBRID III V ON SILICON LASERS FOR PHOTONIC INTEGRATED CIRCUIT.

This 3 years work covers the design, the process and the characterization of III-V on silicon lasers at 1.31 µm for datacommunication applications. In particular, the design part includes the optimization of the coupling between III V and Si using adiabatic tapers as well as the laser cavity, which is formed within the Si. Three types of lasers were studied, all of them based on cavities which consist of gratings: distributed feedback (DFB) lasers, distributed Bragg reflector (DBR) lasers and finally sampled-grating DBR (SGDBR) lasers. Regarding the DFB lasers, two solutions have been chosen: the grating is either etched on top or on the edges of the Si waveguide to form so called vertically or laterally coupled DFB lasers. The latter type, quite uncommon among hybrid III V on Si technologies, simplifies the process fabrication and broadens the designs possibilities.

Not only the lasers demonstrated show high output powers (~20 mW in the waveguides) but also very good spectral purities (with a side mode suppression ratio higher than 50 dB), especially for the DFB ones. The SGDBR devices turn out to be continuously tunable over a wavelength range higher than 27 nm with a good spectral purity as well and an output power higher than 7 mW in the waveguide with great opportunities of improvement.

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Thomas FERROTTI
DESIGN, FABRICATION AND CHARACTERIZATION OF A HYBRID III-V ON SILICON TRANSMITTER FOR HIGH-SPEED COMMUNICATIONS.

For several years, the volume of digital data exchanged across the world has increased relentlessly. To manage this large amount of information, high data transmission rates over long distances are essential. Since copper-based interconnections cannot follow this tendency, high-speed optical transmission systems are required in the data centers. In this context, silicon photonics is seen as a way to obtain fully integrated photonic circuits at an expected low cost. While this technology has experienced significant growth in the last decade, the high-speed transmitters demonstrated up to now are mostly based on external laser sources. Thus, the aim of this PhD thesis was to conceive and produce a high-speed silicon photonic transmitter with an integrated laser source.

This transmitter is composed of a high-speed silicon Mach-Zehnder, co-integrated on the same wafer with a hybrid III-V on silicon

distributed Bragg reflector laser, which emission wavelength can be electrically tuned in the 1.3µm wavelength region. The design of the various elements constituting both the laser (III-V to silicon adiabatic couplers, Bragg reflectors) and the modulator (p-n junctions, travelling-wave electrodes) is thoroughly detailed, as well as their fabrication. During the characterization of the transmitters, high-speed data transmission rates up to 25Gb/s, for distances up to 10km are successfully demonstrated, with the possibility to tune the operating wavelength up to 8.5nm. Additionally, in order to further improve the integration of the laser source with the silicon photonic circuit, a solution based on the low-temperature (below 400°C) deposition of an amorphous silicon layer during the fabrication process is also evaluated. Tests on a distributed feed-back laser structure have shown performances at the state-of-the-art level (with output powers above 30mW), thus establishing the viability of this approach.

Etienne FUXA
THEORETICAL STUDY OF THE DIMENSIONING TO A 5µm PITCH OF A BOLOMETER MATRIX OF BONDED SOI DEVICES ON FREE STANDING STRUCTURES FOR

The work reported in this document relates to pixel size reduction in uncooled infrared imaging in the LWIR range. While the motivation for such a downsize is pretty straightforward (better matrices performances or lower production costs), achieving this without lowering the pixel performance is a true challenge. That is, for state of the art detectors based on thermistors, pixel downscaling leads to lower signal to noise ratio as well as a decrease in detector thermal isolation that in turn reduces the signal's amplitude.

Our work focused on the study of SOI components for use as thermal transducer in a 5µm pixel design. As such we evaluated these components' intrinsic thermal properties to compare the expected performance of a 5µm SOI bolometer with that of a state of the art bolometer scaled to the same pixel size, which allowed us to conclude that the interest for SOI bolometers is well-founded.

We were also able to confirm that our pixel design is able to maintain sufficient IR absorption, but that the thermal isolation is yet problematic. This problem is however not specific to SOI bolometers and as such does not undermine the interest for SOI detectors for 5µm pixel pitch bolometers for uncooled IR imaging.

Marc GUILLAUMONT
VARIATIONS OF TRANSITION METAL OXIDES: RELATIONSHIP BETWEEN STRUCTURE, TRANSPORT AND BOLOMETRIC PERFORMANCES

InfraRed detection, formerly reserved to defense and spatial applications, is currently undergoing deep changes which open new opportunities. Uncooled microbolometer technologies, compatible with classical semiconductors processes, are now able to produce low cost thermal imagers and this will open the door to customer markets in a close future.

The technology developed in the CEA/LETI laboratory use the amorphous silicon (noted "a-Si") as the thermistor material. This material has many advantages, in particular, its excellent compatibility with the classical tools used in microelectronic industry. However, better performance in the thermistor material is still needed to address future applications.

To handle this challenge, CEA/LETI laboratory is currently developing thermistors made of transition metal oxides thin films. The study presented hereby is based on various transition metal oxides samples deposited in the CEA/LETI Laboratory.

Characterization of the structure and the electronic transport for each of these samples allowed us to put in evidence correlations between microscopic structure and conduction mechanisms. Two main figures of merit impacting the overall material performance were investigated: the TCR, Temperature Coefficient of Resistance (which must be maximized) and the $1/f$ noise (which must be minimized).

Finally we conclude this work by highlighting majors outlines governing the performance of a thermistor.

Michel KHOURY
MOVPE GROWTH OF SEMIPOLAR GAN ON PATTERNED SILICON SUBSTRATES

Growth of device-quality semipolar GaN, however, comes at a price, and the only currently available option is homoepitaxy, which is limited in size and is highly priced. At this point, the growth on foreign substrates becomes appealing, especially on silicon.

The main motivation of this PhD thesis is devoted to improve the quality of semipolar GaN on patterned silicon substrates. The process adopted consists of patterning the appropriate silicon wafer orientation in order to reveal Si (111) facets, over which the selective growth of GaN along the +c-direction will be carried out. The c-oriented crystals will be brought to coalescence such that a continuous semipolar layer is achieved. Indeed, the overall approach to selectively grow semipolar GaN on patterned substrates has been previously demonstrated. However, no major advancement has been reported for producing universal methods that reduce the density of defects in these layers.

The contribution of this thesis encompasses four main aspects: first, since a previous study on semipolar GaN-on-Si in our laboratory was lacking before this work, the first target was to establish the know-how of substrate fabrication, over which the hetereoepitaxial growth of GaN is then carried out. Second, the presentation of an original method whose purpose is the efficient defect blocking that may pave the way towards high-quality heteroepitaxially grown (1011) semipolar GaN layers. Third, the demonstration of the (2021) semipolar orientation, which has not been previously reported on silicon substrates before this work. Finally, a study towards a better understanding of the so-called meltback etching effect and the presentation of methods that lead to its prevention.

Anthony LEFEBVRE
FROM SIMULATION TO DESIGN AND TEST OF INFRARED NANOPHOTONIC MICRO-HOTPLATES FOR GAS SENSING APPLICATIONS

Joule-heated suspended microhotplates can be used as infrared sources in cheap, low-consumption spectroscopic gas sensors. To enhance the very low efficiency of first generation structures, both their thermal and optical designs have to be optimized. The implementation of frustrated plasmonic resonators on top of the membrane grants both spectral and angular control of its emissivity. It is thus possible to make it radiate only at the frequencies absorbed by the gas under study, and in the solid angle of the detector. This leads to an increase in useful radiated power while the overall electrical consumption is decreased.

Dynamical studies of membrane heating provide welcome insight on the relationship between membrane radius, heating time and energy consumption per measurement. The existence of a compromise is demonstrated in order to maximize the radiative efficiency, and its physical interpretation is detailed. Eventually, membranes fabricated in LETI's clean room were characterized to measure their electrical, optical and mechanical properties. The implementation of such sources in a CO_2 prototype sensor led to state-of-the-art results, with a few dozen ppm sensitivity with a power consumption of only one milliwatt.

Nicolas MANTE
HETEROEPITAXY OF GAN ON SI: FROM NUCLEATION TO STRAIN RELAXATION, TRANSMISSION ELECTRON MICROSCOPY STUDY

This work is dedicated to GaN on Si heteroepitaxy, at nanometer scale by transmission electron microscopy. First we study the AlN buffer layer growth, by analysing its interface structure with Si substrate, and the first growth stages. This is done by comparing MBE and MOCVD growth processes, for which differences are observed, as the formation of amorphous inter-layer for high temperature MOCVD. Then nanodiffraction with precession (N-PED) allows us to determine strain distribution among the entire heterostructure. With the help of conventional TEM imaging, we correlate threading dislocation behaviour (loop and inclined dislocations) to the strain relaxation in GaN. Hybrid growth based on a combination of MBE and MOCVD layers appears to be quite efficient concerning the reduction of dislocation density, and thus interesting for LED applications. Cathodoluminescence highlights presence of impurities and their effect for each epitaxy stages. Finally we explore the possibility to grow GaN epilayers on a thin Si layer on insulator (SOI), as a compliant substrate. This last study is mainly conducted for MBE layers, and requires to be extended to MOCVD structures, for which observed compliant effects may potentially be more significant.

Candice THOMAS

STRAINED HGTE/CDTE TOPOLOGICAL INSULATORS, TOWARD SPINTRONIC APPLICATIONS

Topological Insulators (TI) are a new class of materials that recently attracts a large interest both theoretically and experimentally thanks to the unique electronic and spin properties that arise on their interfaces. Indeed, with graphene-like transport properties carried by massless Dirac fermions and a topological protection preventing from backscattering phenomena, TI surfaces are full of promise for the design of future quantum electronics.

However, so far, only few material systems fulfill the requirements to make strong TIs. With an inverted band structure, the semi-metal HgTe is one of them assuming the opening of a bandgap by tensile strain.

This PhD thesis aims at experimentally demonstrating the topological nature of strained HgTe as well as its eligibility for applications, especially for spintronics. To do so, strong efforts have first been dedicated to the improvement of the growth process by molecular beam epitaxy, leading nowadays to structures with flat interfaces and very high mobility (up to 600,000 cm2/(V.s)). Such a material quality has then enabled quantum Hall effect to be unambiguously demonstrated using low temperature magneto-transport measurements, exhibiting direct evidences of Dirac fermions at the surface of strained HgTe from temperature dependence analysis. Finally, the ability of HgTe surfaces to generate spin-polarized currents has been experimentally verified, paving the way toward the use of this TI system for future spintronics. On this basis, the implementation of strained HgTe into simple p-n junction has been investigated to realize a first spin-based logic element.

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