SILICON TECHNOLOGIES AND COMPONENTS

2017
Annual research report
Committed to Innovation, Leti Creates Differentiating Solutions for its Industrial Partners.

Leti is a research institute of CEA Tech and a recognized global leader in miniaturization technologies. Leti’s teams are focused on developing solutions that will enable future information and communication technologies, health and wellness approaches, clean and safe energy production and recovery, sustainable transport, space exploration and cybersecurity.

For 50 years, the institute has built long-term relationships with its industrial partners, tailoring innovative and differentiating solutions to their needs. Its entrepreneurship programs have sparked the creation of 64 start-ups. Leti and its industrial partners work together through bilateral projects, joint laboratories and collaborative research programs. Leti maintains an excellent scientific level by working with the best research teams worldwide, establishing partnerships with major research technology organizations and academic institutions. Leti is also a member of the Carnot Institutes network*.

* Carnot Institutes network: French network of 34 institutes serving innovation in industry.

CEA Tech is the technology research branch of the French Alternative Energies and Atomic Energy Commission (CEA), a key player in research, development and innovation in defense & security, nuclear energy, technological research for industry and fundamental physical and life sciences.

www.cea.fr/english

Leti at a glance

- **€315 million budget**
- **800 publications per year**
- **ISO 9001 certified since 2000**
- **Founded in 1967**
- **Based in France (Grenoble) with offices in the USA (Silicon Valley) and Japan (Tokyo)**
- **350 industrial partners**
- **1,900 researchers**
- **2,760 patents in portfolio**
- **91,500 sq. ft. cleanroom space, 8” & 12” wafers**
- **64 startups created**
Within CEA Tech and Leti, silicon technologies and components research activities are shared between two divisions gathering together around 600 researchers:

The **Silicon Technologies Division** carries out innovative process engineering solution and research, operates 24/7 year round, 7500m² of state-of-the-art cleanroom space divided into three different technology platforms.

The **Silicon Components Division** carries out research on nanoelectronics and heterogeneous integration on silicon and is focusing on two mains areas: on-going shrinking of CMOS devices to extend Moore’s Law for faster, less-expensive computing power, and the integration of new capabilities into CMOS, such as sensors, power devices, imaging technology, and new types of memory, to enable new applications.

This booklet contains 42 one-page research summaries covering advances in the focus areas of our Silicon Devices and Technologies Divisions, highlighting new results obtained during the year 2017.
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Dear Reader,

We are proud to release our eighth Silicon Components and Technologies Annual Scientific Research Report, for the year 2017. This booklet contains 42 one-page research summaries covering advances in the focus areas of our Silicon Components and Technologies Divisions, highlighting new results during the year.

The year 2017 illustrates the continuing innovation of our Si technologies divisions to contribute from a hardware point of view to the big data and artificial intelligence area, Internet of Things (IOT), automotive, energy, health and environment monitoring. In this annual report, we confirmed our positioning in disruptive Si research with several highlights including quantum-computing development on Si CMOS, neuromorphic architecture with emerging resistive memories, reduced programming consumption in RRAM arrays, innovative back-end selectors for memories, disruptive 3D concepts or advanced mask-less patterning, opto-mechanic resonators, RF switches concepts with emerging materials, advanced GaN-on-Si for power electronics.

Our research on future IoT sensing systems includes new transducers, embedded RF functionalities and substrates, embedded intelligence, dedicated packaging, energy harvesters and micro-batteries.

In 2017, the Silicon Divisions produced 400 publications, achieving impact factors as high as 18.

We thank our industrial partners for their continuing confidence in us. We are committed to ensuring the transfer of the most advanced research to industry. Strong industrial partnerships are the foundation of our culture of innovation.
We are very proud of our valuable collaborations outlined in this report with several French universities and research institutes, CNRS (IMEP-LAHC, LTM, III-V Lab., IEMN, Néel Institute, LAAS, LNCMI, ...), CEA-DRF, CEA-LIST, INSERM, and, locally, University Grenoble Alpes and INPG, INL, CPE, Ecole Centrale and INSA-Lyon, CEA-LITEN involved in nanotechnologies for electronics.

We are very grateful to our international academic collaborators cited in this report including teams at Jülich (Germany), Stanford university (USA), Caltech (USA), the University of California (USA), Fraunhofer institutes (Germany), Università degli Studi di Ferrara (Italy) University of Cambridge (GB), Université Catholique de Louvain (Belgium), Politecnico Di Milano (Italy), Paul Scherrer Institute (Switzerland), École Polytechnique Fédérale de Lausanne (Switzerland), ETH – Zürich (Switzerland), CNR (Italy), University of Chicago (USA), Sherbrooke University (Canada), NIMS (Japan), University of Southern Denmark, University Cagliari (Denmark), Institute for Technical Physics and Materials Science (Budapest), Hungarian Academy of Sciences (Budapest), Korea University (Seoul), centro universitario FEI (Brazil), University of Tsukuba (Japan).

We are committed to international scientific collaborative research by participating in major European research programs, European Research Council grants, international conferences, program committees, boards of governors and evaluation committees.

Underlying all these efforts is the cooperation of all our researchers and management, as well as the Silicon Technologies and Components Divisions and CEA-LETI’s scientific advisory board.

I also wish to extend my appreciation to the editors and authors of the eight chapters of the 2017 Scientific Report, who spared no effort in the preparation of this document.

Thomas Ernst
Chief Scientist
Silicon Technologies and Components
Dear Reader

With an expected growth about 8% in 2018, the global semiconductor industry is again in a healthy growth phase, with strong demands in new promising applicative fields such as the accelerating adoption of AI, the establishment of the 5G protocol targeting initial deployment in 2019 to provide high bandwidth for UHD videos, autonomous driving, IoT devices, and the momentum in the adoption of electric and hybrid electric vehicles. Development of new technologies and components is mandatory to fully satisfy these demands in a swiftly evolving environment. This is the central objective of our Silicon Components Division. To efficiently achieve this mission, a large staff of microelectronics experts relies on a state-of-the-art 300 and 200 mm facilities where it:

- Continuously benchmarks the different technology roadmaps (FinFET vs FDSOI, 3D stacking vs sequential integration…) and identifies the most appropriate technologies for a wide range of applications.
- Pioneers disruptive technologies to prepare and anticipate the required solutions for future markets.
- Federates global partnerships for an efficient industrial manufacturing path of these solutions.

Within this context, the Silicon Components Division has achieved significant successes in 2017. Let me highlight some of them below, in our central activities

**More Moore – CMOS and beyond CMOS**

- In the field of FDSOI, Léti has brought an efficient support to its partners, with the implementation of NVM (PCM) and RF capabilities into STMicroelectronics 28FDSoI platform and with increasing the maturity of GF 22FDX platform, as well.
• New advanced lithography process by Directed Self Assembly for Si nanowires for sub-7nm MOSFET transistors has been fruitfully demonstrated. The development of a CMOS-derived technology platform allowing to implement both qbits devices and peripheral control electronics operating at low temperature has been undertaken.

• In the domain of 3D integration, implementation of advanced direct Cu/Cu bonding modules and self alignment techniques for die to wafer bonding has been put in place within the frame of IRT Alliance.

Power Electronics and Energy
• A major partnership has been signed with STMicroelectronics for the development of GaN power components, covering a wide range of power devices and various applicative fields.

• The achievement of a compact H-bridge motor driver on silicon by integration of power transistors with interposer-based collective packaging. Done in close collaboration with AMS and Infineon, this silicon H-bridge is five times more compact, faster, and less expensive to manufacture, compared to conventional ones.

• The broadening of hybrid direct bonding technologies, which today allows to integrate and innovate in components as various as image sensors, micro-displays, power convertors and RF filters.

More Moore and Microsystems
• The implementation of generic platforms (M&NEMS for inertial sensors, NEMS for gravimetric sensors, spintronic platform for magnetic sensors, piezoelectric materials platform for actuators) is providing an efficient help to our partners in the swiftly evolving field of microcomponents.

• The development of new innovative technologies and concepts: optomechanical detection to greatly improve the detection levels of our future sensors, haptic technologies to create new user interfaces, or the demonstration of new RF components such as purely acoustic based RF filters and RF switches using phase change materials.

• Several industrial transfers on advanced processes and materials have been successfully achieved worldwide.

All these results were obtained due to the sustained efforts of our team, and, I would like to sincerely thank them all. This report provides you with an overview of their achievements.

Jean René LEQUEPEYS
Head of Silicon Components Division

I would like to introduce to you my colleague Pascale Berruyer who is responsible for DCOS since January 2018 and will produce the next scientific report.
Dear Reader

The mission of our division is to provide our internal and external customers with the best innovative engineering solutions, so they can perform world-leading research on next-generation technology nodes. To achieve this, we provide 7,500m² of advanced research facilities, 3,000m² of nano characterization platform and the best human competencies.

In 2017, DTSi invested in new R&D equipments and continued to develop a strong policy of collaboration with equipment suppliers. The idea is to build win-win partnerships. Leti takes advantage of innovative tools or materials to develop next-generation technologies. In return, our partners gain insight into the requirements needed for future market positioning.

In 2017, an important investment was made with the acquisition of our 300mm immersion scanner and the associated upgrade of a new clean room space.

The year also was rich in scientific results for our division with more than 171 scientific papers published. The international recognition we received, in particular the Helmholtz international fellow award given to Jean-Michel HARTMANN (eight distinctions and awards obtained in 2017) underscores the excellence of our teams and their accumulated skills and expertise. We have also generated 41 patents.

Our teams are focusing on key challenges around advanced CMOS, 3D, photonics and advanced memories. We are also addressing key 200mm challenges around MEMS, power electronics, RF, display, and other fields.
Examples of our achievements include:

In the piezo actuators domain, we have developed a new 200 mm plasma etching process on full piezo electric module (PZT) including electrodes to provide an industrial solution to the market. Extension of these developments to lead free materials is envisaged for future requirements.

Our lithography plateform expanded with the installation of our 200 mm fully automated Nano-Imprint plateform within the frame of our INSPIRE program. This new capability opens a new range of applications and completes our set of lithography equipment on offer.

In the domain of image sensors and eNVM, we have developed new 300 mm CMP processes for next generation Back Side Imager as well as for memory based on phase change materials (PCM). We have also demonstrated a new 300 mm hybrid bonding Cu/Oxide with less than 200 nm alignment precision allowing high Cu interconnection density.

In the beyond CMOS domain and within the frame of our quantum electronics activities, we have developed a 300mm epitaxy process to obtain Silicium 28Si using a specific precursor of 28SiH₄ with high level of enrichment of the isotope 28 (99.992%).

In terms of new material development, we have demonstrated the scalability of monolayers of MoS₂ in an ALD 300 mm chamber, using a specific precursor developed in collaboration with our partner C2P2.

In off line characterization, within the ERC Holoview project. we are now able to electrically test nanoscaled materials with one nanometer resolution in a TEM. Different TEM-based techniques are used to measure the structure, electric & magnetic fields, composition changes and also perform spectroscopy. This now allows us to understand better how nanoscaled devices work in order to improve their properties.

Concerning 2018 perspectives, DTSi will maintain a strong 200mm activity with a specific focus on GaN applications for both power and display, and in 300mm the priority will be made to install and qualify complementary equipments in order to gain in autonomy and allow new development capabilities in key application domains:

- eNVM (PCRAM, RRAM)
- CMOS FDSOI
- 3D integration
- Vertical SPAD Image sensors
- Far Back End Optics
  - Photonic with integrated IIIV laser
  - Next generation SOI substrats

This scientific annual report includes additional details about key achievements, which were made possible by the work of our researchers and technicians. I would like to take this opportunity to thank all of them for their constant commitment.

Best regards.

Fabrice Geiger
Head of Silicon Technologies Division

I would like to introduce to you my colleague Laurent Clavelier who is responsible for DTSi since January 2018 and will produce the next scientific report.
Key figures

623 researchers
135 industrial residents
95 PhD students in 2017
28 Post-docs in 2017

200 & 300 mm platforms for advanced CMOS/3D
270 tools for 200 mm, non stop operation
120 tools for 300 mm, non stop operation
6100 m² cleanroom ISO3-5

200 mm platforms for MEMS
130 tools, non stop operation
2200 m² cleanroom ISO4-5

22 commun laboratories
129 patent filed in 2017
376 papers issued in 2017 (WOS, SCOPUS)
TECHNOLOGICAL PLATFORMS

The silicon divisions operate 8300 m² of state-of-the-art cleanroom space divided into three platforms, gathering 500 process tools and a combined staff of more than 450; they run industry-like operations, 24 hours a day, 7 days a week, all year round.

- The Nanotech200&300 platform provides 200mm and 300mm CMOS wafer processing, which can be applied to both semiconductor and microsystem devices.
- The MEMS200 platform produces non-CMOS Micro-ElectroMechanical Systems (MEMS).

Both platforms are focused on the More than Moore initiative to develop new semiconductor capabilities. An innovative cleanroom shuttle system links the two platforms to add process flexibility and faster processing.

- The third platform 3D Integration aims to integrate various microelectronics objects together in order to juxtapose complementary functions, such as sensing, storing, processing, actuation, communication and energy scavenging. This provides advanced system solutions in three dimensions.

This line is open to our customers for prototyping through the Open3D service.

All research carried out in our cleanrooms benefits from the Nano-Characterization Platform, which is located on the MINATEC campus. This platform, unique in Europe, covers eight domains of competencies, including electron microscopy, X-ray diffraction, ion beam analysis, optics, scanning probe, surface analysis and sample preparation, magnetic resonance.
ORGANIZATION

Silicon Technologies Division is organized according to six departments.

- Three Process Departments whose missions are to execute generic process steps for all projects and to develop innovative processes to provide state-of-the-art solutions to internal and external customers. These departments are focused on patterning, deposition, and surface treatments. Their research activities in collaboration with key universities will support Leti’s advanced position in the future.
- A Characterization Department whose mission is to perform off-line observations to characterize process steps, materials or components. This department also has a research activity to maintain its level of excellence.
- Two Support Departments: one is in charge of the planning, the interface with internal divisions or external customers as well as methods, training and clean-concepts. The other is responsible for facilities operations and engineering.

Silicon Components Division is organized around three departments with clear objectives and market focus.

- The MOS Department’s mission is to simulate, model, develop, demonstrate and test new generations of circuits and modules for sub-20nm CMOS, digital and memory.
- The MEMS Department designs and develops innovative microsystem components (sensors, actuators and RF) and the associated toolbox (packaging, heterogeneous integration, reliability).
- The Power and Energy Department develops and demonstrates technology modules and components for power and energy (photovoltaic, power electronics, integrated storage)
Publications

Prize and awards
• 7 Best paper awards (RADEC, ICICDT, SINANO, IEPBN, ISTFA, EIPBN, ICPT)
• 2 Best PhD distinctions (Sabrina Fadloun, Gaben Loic)
• 2 on-going European Research Council Grants (Sebatien Hentz, David Cooper)
• Helmholtz international fellow award, Jean-Michel Hartmann
• European Semi Award, Gilles Poupon
• 10 Years ECTC Volunteer Award, Gilles Poupon
• Roger Fourme Price (Munique Kazar-Mendes)
• FDSOI Gold Electron price

Experts
4 Research Directors, 8 International Experts, 35 Senior Experts, 54 Experts, 9 of whom hold HDR.

International Collaborations
Jülich (Germany)
Stanford University (USA)
Caltech (USA)
The University of California (USA)
Fraunhofer institutes (Germany)
Università degli Studi di Ferrara (Italy)
University of Cambridge (GB)
Université Catholique de Louvain (Belgium)
Politecnico Di Milano (Italy)
Paul Scherrer Institute (Switzerland)
École Polytechnique Fédérale de Lausanne (Switzerland)
ETH – Zürich (Switzerland)
CNR (Italy)
University of Chicago (USA)
Sherbrooke, University (Canada)
NIMS (Japan)
University of Southern Denmark
University Cagliari (Denmark)
Institute for Technical Physics and Materials Science (Budapest)
Hungarian Academy of Sciences (Budapest)
Korea University (Seoul)
Centro universitario FEI (Brazil)
University of Tsukuba (Japan).

Scientific committees
• National Research Agency «High performance infrastructures, software technology and science » committee.
CORE & BEYOND CMOS

- Harnessing FDSOI CMOS technology for quantum information processing
- 3D sequential integration: towards application driven devices definition
- Key low temperature process steps for high performance and reliable 3D sequential integration
- Optimization of CMOS FDSOI technology devices for RF applications using 3D TCAD simulation
- Performance and design considerations for gate-all-around stacked-nanowires FETs
Harnessing FDSOI CMOS Technology for Quantum Information Processing

RESEARCH TOPIC:
Spin-based quantum information in Silicon

ABSTRACT:
We pursue our progress on the demonstration of the basic building blocks of quantum information processing derived from a Si CMOS technology platform. In our approach, characterized by an emphasis on foundry compatibility in terms of processes and materials, the so-called qubits are encoded in the spin degree of freedom of gate-confined elementary charges. We show that the SOI Back-Gate not only provides an additional handle for optimizing the speed and fidelity of spin readout in charge detectors, but also represents a significant asset for reducing the energy dissipation of potentially co-integrated classical control electronics.

SCIENTIFIC COLLABORATIONS: CEA IminC, CNRS Institut Néel, STMicroelectronics

Context and Challenges
The building block of quantum processors is the quantum bit (qubit) which is made out of a two-level quantum system. In contrast with a classical bit the information is encoded in a superposition of 0 and 1. Along with entanglement, this property can be harnessed by specifically designed algorithms to achieve a computational acceleration for applications such as cryptography, searching large databases or simulation of quantum processes. In silicon-based quantum devices, the qubit is formed by the spin degree of freedom of a single charge carrier (electron or hole) trapped in quantum dots. In our recent work, we demonstrated two-axis control of the first hole spin qubit in a Si transistor-like structures using a CMOS technology platform. However, the qubit state was then evaluated by averaging repeated destructive measurements followed by qubit re-initialization. In order to perform fault-tolerant quantum computation, the so-called error correction codes, the single-shot (real-time) detection of the spin state is required.

Main Results
We have shown [1] an ultra-compact device fabricated in foundry-compatible Si MOS technology, with a built-in charge detector (Single Electron Transistor, or SET) capacitively coupled to two Gate-defined Quantum Dots (QDs). Thanks to an energy-selective transport scheme, we have demonstrated single-shot readout of the spin-state in one of the QDs (Figure 1), which is an essential requirement to implement fault-tolerant quantum computing. On FDSOI, the possibility of using the back-Gate as an additional handle is an asset for further optimizing the readout speed/fidelity trade-off. In particular, it can be used to tune the cross-capacitance between the SET and the QD in order to improve the readout signal.

Another longer-term advantage is the perspective of reducing the parasitics by seamlessly co-integrating Si qubits with conventional control electronics circuitry [2]. Since qubits operate at T<1K, a drastic constraint is set on power dissipation by the classical circuits, which is proportional to the square of the supply voltage (V_{DD}). At low temperatures, the subthreshold slope steepens but the threshold voltage increases. Having the ability to shift the transfer characteristics towards lower voltages is a key asset that allows leveraging the commutation abruptness for low supply voltage operation. The Ground Plane in 28FDSOI technology is shown to successfully modulate the threshold voltage at liquid helium temperature (Figure 2).

Perspectives
Future work will include the development and implementation on our devices of alternate single-shot readout techniques such as RF reflectometry [3], which do not require flowing DC current in the vicinity of the qubits. Further modelling, design and characterization of low temperature and low supply voltage-operating classical electronic circuits aiming at addressing, controlling and reading out the states of the qubits are also planned. A common SOI CMOS platform for integrating both the quantum devices and their associated control and auxiliary functions looks as promising as ever.

REFERENCES:
3D Sequential Integration: Towards Application Driven Devices Definition

RESEARCH TOPIC:
3D sequential integration, low thermal budget process flow, technology applications

AUTHORS:
P. Batude, F. Andrieu, L. Brunet, C. Fenouillet-Beranger, J-P. Collinge, D. Lattard, R. Berthelon, M. Vinet

ABSTRACT:
Leti is renewing its vision on the application of 3D sequential integration, not limiting its research scope to the high performance computing field. This technology has also been identified has a powerful asset for alternative computing to Von Neuman architecture with neuromorphic computing and processing in memory for example. This roadmap draws new opportunities of research in term of device, with junctionless FET being a low cost and ultra-low thermal budget FET compatible with the stacking of numerous active layers (≥4). Finally, the use of 3D sequential integration to co-integrate easily MOSFETs with sensor shows promise. The success of this More than Moore roadmap relies on the ability to design low temperature high voltage analog MOSFETs. Also, 3D sequential integration has been shown to offer the ability of having a local ground plane for the top level. A 24% frequency gain on double-gate low-leakage inverters at VDD=0.6V and 29% read and write current gains on 6T SRAM at a given static power is highlighted.

SCIENTIFIC COLLABORATIONS: Université Grenoble Alpes / IMEP-LAHC / ST Microelectronics / Applied Materials

Context and Challenges
3D sequential integration, with its unique 3D contact characteristics offers a large set of applications. The stacked device process is highly dependent on the targeted application. The CMOS over CMOS integration with intermediate BEOL between the stacked MOSFETs targeting the interconnect delay reduction impose stringent constraints in term of stability process window (500°C) and the Low Temperature (LT) MOSFET need to have the same performance as the bottom one. All the technological bricks to reach this goal have been successfully demonstrated (Figure 1) [1].

Main Results
The objective of this work is to infer the new directions for device optimization for other application than traditional Van Neumann computing. For example, IoT applications or neuromorphic computing could require lower performance devices, justifying the development of ultra-low thermal budget FETs (TB <400°C) such as TFT, CNT and junctionless devices. The neuromorphic computing should be boosted in power efficiency thanks to the stacking of a high number of stacked layer MOSFETs layers with RRAM being inserted in the back end of line (see Fig. 2). Thanks to their smaller thermal budget and also small cost, these devices are perfectly adapted to this application.

RELATED PUBLICATIONS:
Key Low Temperature Process Steps for High Performance and Reliable 3D Sequential Integration

RESEARCH TOPIC:
3D sequential integration, low thermal budget process flow, gate stack reliability, iBEOL, ULK reliability, FinFET, SPER

AUTHORS:

SCIENTIFIC COLLABORATIONS: IMEP LAHC (France), STMicroelectronics (France).

ABSTRACT:
Breakthroughs in key technological modules for high performance and reliable 3D Sequential Integration with intermediate BEOL (iBEOL) in-between layers are highlighted. We demonstrate for the first time that (i) a high-quality solid phase epitaxy process is possible at 500°C for FDSOI devices and FinFETs activation with an innovative low temperature (LT) double SPER (DSPER) is demonstrated (ii) TiN native oxide removal prior to poly deposition leads to an improvement in gate stack reliability below 525°C and (iii) state-of-the-art SiOCH ULK in iBEOL is reliable up to 550°C with W metal lines. A process integration is thus proposed to match the process windows of bottom layers (bottom FET and iBEOL) stability and top devices performance and reliability, opening perspectives for a wide range of applications and technologies using 3D Sequential Integration.

Context and Challenges
3D Sequential CoolCube™ integration is based on stacked layers of devices fabricated one on top of each other, allowing extremely scaled 3D contact pitch. One major difficulty however is to process devices of the top layer without degrading what is below, which is translated into a thermal budget (TB) limitation. Our previous works have aimed at lowering the TB of offset spacers deposition, raised sources and drains (RSD) epitaxy and dopants activation. Low-k dielectrics, cyclic deposition/etch (CDE) epitaxy to deal with selectivity issues, extension-first integration (XFirst) to place dopants below the spacers, Solid Phase Epitaxy Regrowth (SPER) and nanoseconds laser anneal are key technological solutions in order to decrease the thermal footprint on bottom layers below 600°C. Meanwhile, the TB “seen” by the gate stack modifies its properties which need to be studied. Reliability of top devices is a major concern when decreasing temperatures below 800°C. In parallel, regarding low TB FinFET processes, very few published data have been found in the literature. We report a novel SPER activation process for high-performance, low thermal budget FinFET fabrication. Finally, intermediate back-end-of-line (iBEOL) needs to be implemented between top and bottom tiers to avoid routing congestion. The use of tungsten provides a higher thermal stability (up to 550°C 5h) compared to conventional copper in terms of capacitance and resistance variations, but reliability needs to be evaluated.

Main Results
The main remaining questions in 3D Sequential Integration are now answered: exhaustive reliability issues has been addressed for the first time. The TB of dopant activation has been further reduced from 600°C 1min down to 500°C 10min using SPER. TiN native oxide removal prior to poly deposition is a key process in order to improve top pFET reliability within a 525°C restricted TB (Figure1) [1].

Regarding FinFETs devices, activation with an innovative LT double SPER (DSPER) is demonstrated for the first time (Figure 3) [2]. The performance of the devices is 90% of HT POR, while the LT thermal budget is compatible with 3D sequential integration technology. This process is using a gate-last and SAC approach which are characteristic of advanced high performance FinFET nodes [2].

Besides, state-of-the-art SiOCH ULK has been shown to be the reliable up to 550°C 5h with W metal lines [1,3]. All in all, a process window has been identified between 525°C and 550°C for a few hours [1], leading to high performance and reliable top devices while preventing bottom layers from any degradation (Figure 2) paving the way for the integration of CMOS over almost any technologies.

Perspectives
A full low temperature 500°C devices integration is ongoing. For FinFET, guidelines for achieving a quasi-ideal junction profiles have been given for advanced fin width (w<7nm) confirming the device diversity pluggable in 3D sequential integration.
Optimization of CMOS FDSOI Technology Devices for RF Applications Using 3D TCAD Simulation

RESEARCH TOPIC:
FDSOI, RF, High-K metal gate, cSiGe, TCAD, compact model, cutoff frequency, maximum oscillation frequency, gate resistance

AUTHORS:

ABSTRACT:
This research work addresses the optimization of CMOS devices for RF applications, starting from the simulation until the final technological fabrication. The choice of a fully depleted silicon on insulator technology (FDSOI) with the pFET channel made of strained SiGe leads to an outstanding value of 420 GHz for the cutoff frequency of the transistor. The optimal combination of process and layout configurations is inferred from 3D TCAD simulations which draw the guidelines for both the stress engineering in active and continuous-RX regions and the minimization of parasitics.

SCIENTIFIC COLLABORATIONS: GLOBALFOUNDRIES, IEMN

Context and Challenges
In the frame of the considerable spreading of Mobile, IoT and RF applications, FDSOI CMOS offers as the successor of bulk CMOS to deliver HF performance in the range of hundreds of GHz. Such operating frequencies have been demonstrated with CMOS FDSOI having a gate length of about 20 nm. We recently addressed two items: first, finding a process integration scheme including stress engineering for improving the pFET cutoff frequency (Ft) and secondly, understanding the gate resistance impact on Ft and the maximum oscillation frequency (Fmax).

Main Results
RF-pFET in FDSOI: A TEM micrograph of the pFET device with a thin 7nm SiGe channel, raised source/drains, high K-metal gate is shown in Figure 1 a. The SiGe channel is undoped and strained for improved mobility. From 3D TCAD, we developed a compact model to evaluate the stress relaxation in the SiGe channel for any configuration of the active and continuous-RX regions (see an example of stress distribution in Fig. 1 b) infer the optimal stress level for RF performance [2].

Full-3D TCAD for parasitics modelling: A strategy involving calibrated 3D simulation and a multilayered description of the resistive gate is proposed [3]. A structure allowing an accurate calculation of parasitics has been built for reliable computing of RF performance, as shown in Fig. 2a. Then, various effects impacting the values of the Ft/Fmax RF figures of merit were assessed and a sensitivity analysis allowed to identify the main process factors acting on RF performance. The beneficial impact of a larger contacted-poly pitch (CPP) versus the gate finger width is illustrated in Fig. 2b and can be explained by an improvement of the channel transconductance due to lower series resistances rather than by a lowering of the gate capacitance.

Perspectives
Next to the optimization of FDSOI MOSFETs with 20 nm gate length, the research work is pursued with: (i) Spice and small-signal-equivalent circuit modeling of the FDSOI transistor with a focus on RF properties and model-hardware correlation; (ii) TCAD simulations to get physical insight in the mechanisms affecting the RF figure-of-merit; (iii) Definition of process and integration variations that could impact the RF properties of the device; (iv) Characterization, analysis and physical interpretation of RF and high-frequency noise characterization of new devices.

RELATED PUBLICATIONS:
Performance and Design Considerations for Gate-All-Around Stacked-Nanowires FETs

RESEARCH TOPIC:
MOSFET, 5nm node and below, gate-all-around nanowire, replacement-metal-gate process, TCAD, design, benchmark

AUTHORS:
S. Barraud, V. Lapras, B. Previtali, C. Virzioz, J.M. Hartmann, C. Comborouere, V. Loup, N. Rambal, F. Alian, M. Vinet, T. Ernst

ABSTRACT:
Gate-All-Around (GAA) field effect transistors are now recognized as offering the best solution to short-channel-effects with a high current drivability per layout footprint due to 3D vertically stacked channels. Horizontal GAA nanowire (NW) and nanosheet (NS) also have the advantage of being fabricated with minimal deviation from FinFET devices in contrast to vertical NWs which require more disruptive technological changes. For these reasons, the GAA stacked-wire MOSFET architecture is today regarded as an attractive option to push CMOS scaling beyond 7/5nm nodes. Several IC companies have integrated this MOSFET architecture in their roadmap for sub-5nm nodes. Although significant progress have been reported during last years, a particular attention must be paid to intrinsic performances and design considerations of GAA structures for an optimal performance and power efficiency.

Context and Challenges
For several decades, the Si CMOS technology has enabled manufacturers to produce integrated circuits with ever-increasing levels of performance and functionality. If chipmakers seek to extend FinFET, scaling at the 5nm and beyond, they will likely need to move to the evolutionary alternative of GAA MOSFET architecture in order to keep low leakage current as the gate length gets smaller. Then after having fabricated and characterized vertically stacked wires FETs including inner spacer and strain, the width-dependent carrier mobility in Si NW was analyzed and intrinsic performance and design consideration of GAA structures were considered in order to offer more freedom to designers for the power-performance optimization.

Main Results
GAA NS structures could instead be used to maximize the effective width (W_{eff}) for a given layout footprint, which will improve the drive current without increasing power density. As compared to FinFET, the conventional square (or round) NW has a lower W_{eff} for a given layout footprint while the effective width can be significantly enhanced with wider and thin NS compared to conventional FinFETs. A large footprint allows wider NS which yields higher W_{eff} and ultimately better performances while maintaining Drain-Induced-Barrier-Lowering (DIBL) lower than in short-channel FinFET devices (Fig. 1).

FIG 1.

We have shown that GAA stacked-NS can be thought of as a practical compromise between speed and power dissipation. However, to make the best of GAA stacked-NS structures, effective current I_{ eff} enhancement achieved by higher mobility and W_{eff} should not be canceled by an excessive increase in parasitic capacitances. The larger the footprint will be (allowing for the greater width of NS), the larger load capacitance (C_{eq}) will be due to the effective width enhancement. However, it should be noted that C_{eq} is reduced for NWs (W=7nm) but no delay reduction is achieved, while performance can be significantly improved for nanosheet design having wider wires. A delay reduction of around 20% is expected for W_{eq}=30nm. The nanosheets have a higher effective width for a given footprint and therefore drive a capacitive load better. The benefit offered by GAA stacked-NS enabling to relax the fin pitch by using double or triple stack to match or overcome the effective width at constant footprint may be reduced when considering ultra-scaled standard cell height with small fin pitch and few fins. However, a fine tuning of NS width with EUV lithography would tentatively result in improved power/performance management through the modulation of threshold voltage and subthreshold slope.

Obviously, the technological challenges facing the development of a new technology platform featuring GAA nanosheet transistors are still numerous (shape optimization with reduced roughness, inner spacer, access optimization and strain management). Nonetheless, some significant experimental advances have been made recently and show the high competitiveness of this technology for future technology nodes. Nanosheet transistors offers more freedom to designers for the power-performance optimization thanks to a fine tuning of the device width.

Perspectives
We intend to use these methods to study a range of different materials that change their properties after electrical or thermal stimulus. These could include different resistive memories, piezoelectrics, ferroelectrics and magnetic specimens. In addition we will be able to study III-V materials and different photovoltaic materials to measure how the local electrical properties are linked to defects, dopants and interface states.

Further developments are still ongoing in order to improve process integration and predictability of compact modeling for stacked-nanowire devices.

RELATED PUBLICATIONS:

24
• Ultra-low power consumption in RRAM arrays
• Resistive memories for new computation systems
• Back-End Selector for Emerging Memories
• Overcoming phase-change materials science issues
Ultra-Low Power Consumption in RRAM Arrays

RESEARCH TOPIC:
Non-volatile memories, resistive memories, memory hierarchy

AUTHORS:

ABSTRACT:
In this report, programming operations are optimized for low energy consumption and short latency time applications in RRAM kb arrays. Origin of consumption (role of pulse’s time, programming current and voltage in SET and RESET operations) is quantified on HfO2 oxide based RRAM technology. Specific patterns are evaluated to reduce latency time and energy consumption in memory devices. Innovative circuit with on the fly switching detection is proposed, allowing to reduce programming consumption down to single pJ operation in large memory arrays.

SCIENTIFIC COLLABORATIONS: Leti DACLE

Context and Challenges
Energy consumption becomes a critical concern, in data center, due to popularity of cloud storage and mobile devices. It is thus urgent to develop lower energy consuming devices. RRAM energy consumption is typically of 10μJ at the single cell level and is very promising on that concern. However, looking at RRAM statistics, large programming time can be required to insure sufficient window margin (WM) for a high number of cycles, due to intrinsic RRAM variability. Thus, programming energy can drastically increase in high density and high endurance applications. Here, we investigate how optimized programming schemes can help reducing RRAM consumption, providing good endurance and short latency, based on experiments performed on HfO2/Ti kb arrays integrated on 130 nm CMOS logic on top of Metal 4.

Main Results
Pulse optimization
Figure 1a plots WM at 2σ extracted from 10⁴ cycles versus energy consumption measured on kb arrays. Various SET and RESET times (200 ns to 100 μs) and currents (10 μA to 50 μA) were used. Consumption was estimated at the 1st order by Ec = Vprog×Iprog×Tprog. We observe that large WM required targeting dense memory arrays can hardly be reached under 10 μJ. In order to assure sufficient WM while the lowest energy consumption, minimum Iprog of 50 μA and Tprog of ~200 ns are identified. In conclusions, in memory arrays, reducing time is more efficient than reducing programming current to limit energy consumption and ensure sufficient WM.

Pulse shape optimization
Using Ramp Stress Voltage (RVS) instead of constant voltage stress (CVS) significantly increases RRAM programming efficiency, reducing impact of intrinsic RRAM switching time dispersion. Programming time is then strongly reduced in comparison with CVS (Fig.1.b), reducing energy consumption.

Smart procedures
Smart programming (pulse ramp is stopped when cell switches) offers lower consumption, especially when large RRAM array are considered. Smart procedure also allows to improve window margin up to >4σ. Combining optimized RVS pulses and smart procedures, RRAM consumption is significantly reduced to ~1pJ (median value) and ~10pJ at 4σ extrapolations, and window margin is kept open Fig.2).

Perspectives
Perspectives are twofold. First we will analyze the impact of low energy optimized programming schemes on RRAM reliability (retention and endurance). Then ultimate RRAM switching speed (<100ps) will be tested using new designs with on die RF switches.

RELATED PUBLICATIONS:
[2] “Study of the energy consumption optimization on RRAM memory array for SCM applications”, C. Cagli et al., 2017 IEEE International Memory Workshop (IMW), Pages 1 - 4 ; DOI: 10.1109/IMW.2017.7939106
Resistive Memories for New Computation Systems

RESEARCH TOPIC:
RRAM, HfO$_2$, TCAM, variability, characterization, reliability, performance, artificial synapses, neuromorphic circuits

AUTHORS:

ABSTRACT:
Resistive memory technologies (RRAM) can play a crucial role in different emerging fields of application, such as non-volatile logic circuits or neuromorphic systems, to save energy and increase performance. Concerning the introduction of non-volatile functionalities at the logic level, we study the use of RRAM as ternary content-addressable-memory (TCAM) for fast-searching big data. Concerning neuromorphic circuits, we provide guidelines to program RRAM based synapses in a Spiking Neural Network (SNN) for object tracking applications. We clarified the role played by synaptic variability and the robustness to variability.

SCIENTIFIC COLLABORATIONS: INSERM, Clinatec, CEA-LIST, Università degli Studi di Ferrara

Context and Challenges
Understand, classify, and organize a vast amount of data in real-time is a key enabler for big data and Internet of Things applications. To face this challenge, it is mandatory for future technologies to have tightly integrated logic and memories devices. Resistive RRAMs (RRAMs) present huge potential to bring the memory close to the processing unit. In this work, first, we elucidate the interest of RRAM to implement ternary content-addressable memories (TCAM). TCAM systems allow searching a stored information by its content, as opposed to searching by its address. This approach avoids frequent and expensive memory accesses in applications where searching operations among a large amount of data are required, such as: pattern recognition, routing tables and branch prediction in a processor. Second, we study RRAMs for implementing energy-efficient bioinspired synapses, creating a path towards online real time unsupervised learning. This approach will enable the extraction of useful information from sensor data (such as video, audio, biological data...) in wearable devices.

Main Results
Multi-kbits arrays of HfO$_2$-based RRAM have been fabricated and characterized under several programming conditions, resulting in different combinations of endurance and Low Resistive State (LRS) and High Resistive State (HRS) values (Fig. 1). Strong programming condition (A) allows to obtain a large memory window (HRS/LRS) at the cost of shorter endurance (~100 k), whereas with soft programming condition (B) the memory window is reduced but the endurance is improved (~1 M cycles).

First, to impact the tradeoff of this choice on RRAM-based TCAM, we performed SPICE simulations of a single row of 128 TCAM cells sharing the same match line. The ideal RRAM should have unlimited endurance and very large memory window to guarantee a short search latency, while maximizing the ratio between match and mismatch discharge times. Strong programming condition (A) could be used for high-speed networking applications, such as routing tables and database acceleration. Soft programming condition (B) can be adopted for emerging applications like neuromorphic associative memories and reconﬁgurable computing. In these applications, the pattern to be matched is varied frequently and the match does not need to be perfect.

FIG 1. LRS and HRS cumulative distributions measured on 4 kbits array after Set and Reset with soft (B) and strong (A) programming conditions (left). Integrated RRAM used to implement bioinspired synapses and TCAM cells (right).

Second, we clarified the role played by synaptic variability in a SNN for object tracking applications by means of system level simulations performed with the N2D2 tool. To achieve high performance after the training phase, the majority of the synaptic weights have to be weak (RRAM in a HRS), with a tail of stronger connections (RRAM in LRS). Consequently, a large RRAM dynamic range is required. Resistance variability increases the dynamic range for a given memory window (HRS/LRS). Therefore, both the programming conditions (A and B) allows achieving a detection rate higher than 95%.

Perspectives
The results obtained from the experimental characterization of a 4-kb RRAM array have been exploited to give general guidelines for the design of RRAM based TCAM suitable for different applications and for the design of hardware-oriented neuromorphic circuits.

RELATED PUBLICATIONS:
Context and Challenges
Non-Volatile Resistive Memory technologies (NVRM), such as Phase-Change Memory (PCM) and Resistive Switching Memory (RRAM), represent today a real breakthrough in a market context that is evolving and differentiating fast in terms of applications and storage needs. Among the different architectures, Crossbar NVRM Array represents a valuable Back-End technology that can simultaneously achieve stackability over CMOS digital circuits to reduce the access and the writing time, a reduced cell footprint, and 3D integration to realize a higher memory density. This architecture is made possible by the Back-End selector device, such as the Ovonic Threshold Switching (OTS), whose engineering becomes fundamental to achieve high memory performances.

Main Results
We studied the impact of N and Sb doping in Ge-Se based OTS devices, in particular highlighting that Sb doping allows low voltage switching operations and showing how N doping improves the stability of the material against the recrystallization (i.e. detrimental for the device functionality). In Fig. 1, we report the higher performances (i.e. higher selectivity, and sub-threshold non-linearity STNL) finally achieved in our Ge-Se-Sb-N based optimized alloy (GSSN) versus the other studied compositions [1].

**FIG 1.** Current vs-Voltage characteristics for OTS devices based on Ge-Se (GS), on N doped (GSN) or Sb doped (GSS) Ge-Se, and on Ge-Se-Sb-N alloy (GSSN).

We co-integrated our engineered OTS selectors with both PCM and RRAM devices [2, 3], in 1S1R crossbar-like architectures (Fig. 2 and 3 a). Therefore, we demonstrated the possibility to improve the endurance of the 1S1R cells (up to $10^9$ cycles) thanks to innovative reading strategies allowed in such integrations.

**FIG 2.** OTS selector + PCM memory device structure schematic.

Finally, integration engineering was also addressed thanks to an innovative fluorine-free W liner process in order to reduce the contact plug resistance [4]. Fig. 3 b shows the gain in resistivity achieved thanks to such optimization.

**FIG 3.** TEM cross-section of the selector + RRAM (1S1R) device (a); Cumulative distribution functions obtained for contact plug resistance using the process of reference (POR) or the fluorine-free W liner process (b).

**Perspectives**
LETI developments on OTS materials and innovative 1S1R cell designs are ongoing to explore the new horizon of this technology. Back-End Non-Volatile Crossbar Resistive Memory has started a revolution of the memory concept and of the system architecture, which already represents a real breakthrough.
Overcoming Phase-Change Materials Science Issues towards the Development of Ultimate Phase-Change Memories

RESEARCH TOPIC: Non-volatile resistive memories, phase-change memories, chalcogenide

SCIENTIFIC COLLABORATIONS: CNRS-LNCF, CNRS-LTM, CNR-IOM-OGG c/o ESRF, Université de Liège


ABSTRACT: Phase-Change Materials (PCMs) memories are the most promising candidates among emerging non-volatile memory (NVM) technologies. Nevertheless, PCMs memory technology has to overcome several challenges to definitively invade the NVM market. For instance, scaling down PCMs memories for large-scale integration means the incorporation of the PCM into more and more confined structures and raises materials science issues in order to understand interface and size effects on PCM crystallization. Thus, we evidenced the impact of interface on crystallization mechanism of PCM. Besides, we show that incorporation of Indium in GeTe thin films obtained by PECVD is expected to permit to achieve the trade-off between increasing the programming speed of PCM memories without decreasing the amorphous phase stability and thus data retention in devices.

Context and Challenges
Chalcogenide PCMs, such as Ge-Sb-Te alloys, exhibit fast and reversible phase transformations between crystalline and amorphous states with very different transport and optical properties leading to a unique set of features for non-volatile PC memories, such as fast programming, good cyclability, high scalability, multi-level storage capability, and good data retention [1]. At LETI, we examine the main technological challenges that PCM memory technology must face and their associated materials science issues [2]. Among these challenges, the impact of confinement and related size/Interface effects on PCM phase transformation is a first magnitude for ultimate PC memories [1-3, 5]. Interfaces are shown to have a significant impact on the crystallization mechanism of PCMs thin films [3, 5]. Then, increasing the programming speed becomes also a challenge for new PC memory applications such as Storage Class Memory. In that context, Indium incorporation in PECVD GeTe thin films is a promising route to increase the speed limit of GeTe without detrimental on its amorphous phase stability [4]

Main Results
Incorporation of the PCM in a small confined structure allows to significantly improve the efficiency of Joule heating and reduce the RESET current. However, in confined structures, the PCM is in contact with both insulators and metallic electrodes, which raises issues about impact of geometrical confinement on the material properties and phase transformations.

FIG 1. Temperature-resolved resistivity of surface-oxidized (blue) or non-oxidized (red) GeTe films evidence two different crystallization mechanisms: heterogeneous crystallization starting at the oxidized interface (Rdrop ~180°C) followed by growth and crystallization of whole GeTe film (Rdrop~210°C), and one-step homogeneous crystallization with non-oxidized GeTe film volume near 230°C as shown by STEM snapshots acquired in situ during anneals [3].

Increasing the crystallization speed of PCMs is also a major challenge in order to increase the programming speed in PC memory devices. In this context, we investigated the properties of In-GeTe thin films [4]. The crystallization temperature Tc of In-GeTe films with In content up to 11 at. % does not significantly change in this doping range (Fig 2a) whereas the structure of crystallized In-GeTe films is modified by In incorporation. X-ray photoelectron spectroscopy evidenced the presence of In-Te bonds in amorphous In-GeTe films. Upon In incorporation, the progressive formation of InTe6 cubic phase by detriment to GeTe rhombohedral phase is observed by X-ray diffraction after 400°C annealing. Surprisingly, the Kissingar activation energy for crystallization is showing to monotonically decrease as the In content is increased indicating a promising effect of In doping on crystallization speed in memory devices while keeping a good thermal stability for data retention (Fig 2b).

FIG 2. (a) Tc of In0.42Ge0.58Te5.16 (red) and In0.58Ge0.42Te5.16 (blue) films as a function of the In content. (b) Kissingar activation energy Ea for crystallization as a function of the In content for both GeTe films: when the In content increases, Ea monotonically decreases.

Perspectives
The performances of PC memories are intimately related to the physical and crystallization properties of PCMs. The combination of a high crystallization speed during programming and a high thermal stability of the amorphous phase at the operating temperature is required in PCMs. Interface engineering, scaling effect as well as material engineering are promising route to fulfill these challenges.

RELATED PUBLICATIONS:

SIlicon Technologies and Components
PATTERNING

- Innovative 3D nano-patterning into a silicon substrate
- Characterization of photoresist films exposed to high-dose implantation conditions
- Multi-beam lithography: patterning technologies with new integration challenges
- Full wafer scale imprint lithography
- DSA lithography for contact/via patterning
- DSA integration for line/space patterning
Innovative 3D Nano-Patterning into a Silicon Substrate

RESEARCH TOPIC:
Silicon structuring, Implantation, Si anodization

AUTHORS:
L. Nouri, N. Posseme, S. Landis, F.-X. Gaillard, F. Milesi

ABSTRACT:
3D complex structures are nowadays very challenging and require many complicated and expensive steps. CEA-Leti developed a new technique that allows to obtain 3D structures, on silicon based materials, in three steps: First, the nano-imprint lithography defines a 3D pattern, then an ion implantation step transfers the pattern into the subjacent layer and finally the wet etching reveals the implanted areas.

Context and Challenges
Fabrication processes that microelectronic developed for integrated circuit (IC) technologies for decades, do not meet the new emerging structuration’s requirements, in particular non-IC related technologies one, such as MEMS/NEMS, Micro-Fluidics, photovoltaics and lenses. Actually complex 3D structuration requires complex lithography patterning approaches such as gray-scale electron beam lithography, laser ablation, focused ion beam lithography or two photons polymerization. It is now challenging to find cost effective and simple technique to achieve 3D structures. In this context, CEA-Leti proposed a straightforward process to realize 3D structuration of silicon material. This technique consists on transferring a (2D/3D) resist pattern, obtained by either conventional or non-conventional lithography, onto a subjacent layer by Ar implantation, in order to create localized modifications in the material. After the resist stripping, the implanted areas are selectively removed by wet cleaning (Figure 1) [1, 2].

Main Results
After comparing wet etching solutions for silicon (alkaline and acid), or anodic dissolution of Si in HF to remove implanted silicon, silicon anodization was found to be the most efficient way to remove selectively the modified zones without modifying the non-implanted ones. The following SEM photos show a cross section of the wafer at different stages of the process. The anodization process reveals perfectly the implanted areas either for 3D patterns (Figure 2).

Perspectives
After this proof of concept of silicon structuration, the next step will be to extend this new technique to other materials.

FIG 1. Schematic description of the process flow for 2D and 3D patterns (a), (e) Lithography, (b), (f) Implantation through the patterned resist mask and resist stripping, (c), (g) Selective modified material removal by wet cleaning.

FIG 2. Si sample at different steps of the 3D process (a) Nano imprint Lithography, (b) Implantation through the patterned resist mask and resist stripping, (c) Selective removal of the modified material by anodic dissolution of Si in HF.

RELATED PUBLICATIONS:
Characterization of Photoresist Films Exposed to High-Dose Implantation Conditions

RESEARCH TOPIC:
Photoresist, high-Dose Implantation Stripping, Advanced Node Technology

ABSTRACT:
Alternative approaches are now required to fulfill the stringent requirements of photoresist (PR) dry strip process after high-dose implantation. A better understanding of the PR degradations induced by the ion bombardment during the implantation is thus required. In-depth characterizations of PR films after arsenic and phosphorus high-dose implantations using different complementary techniques like TEM, STEM-EDX, TOF-SIMS, XRR, AFM, and XPS are presented.

SCIENTIFIC COLLABORATIONS: STMicroelectronics, CNRS-LTM

Context and Challenges
During the fabrication of integrated circuits, the source and drain of metal–oxide–semiconductor field-effect transistors (MOSFET) are defined by implantation of donor and acceptor ions. This step requires a photoresist (PR) mask to protect some parts of the wafers from the implantation. For most implantation steps, the ion dose ranges from $10^{11}$ to $10^{15}$ ions/cm$^2$ and the implanted resist is easily removed by conventional wet or dry stripping processes. However, advanced technologies require higher implantation doses making dry strip process even more challenging. The main difficulty is to remove efficiently the modified layer (called “crust”) formed during the implantation on the PR surface due to energetic ion bombardment. The second challenge is to be compatible towards implanted substrates and the other materials present such as the metal gate or the high-K materials [1]. The stripping requirements become even more difficult to fulfill with commonly used processes like fluorine-based plasma ashing and hot sulfuric/peroxide mixtures wet cleaning especially because of the unacceptable levels of oxidation and material losses. In order to develop alternative approaches for the stripping of high-dose-implanted PR, a deeper understanding of the PR degradation occurring during the implantation step is needed.

Main Results
In this context, several characterization techniques such as TEM, STEM-EDX, TOF-SIMS, XRR, AFM and XPS have been used to understand the physical and chemical modifications of 200nm thick PR films exposed to implantation processes [2]. Hence TEM observations (fig.1) allowed to distinguish a light area corresponding to the underlying non modified layer (called “bulk”) and a darker area corresponding to a denser material formed at the PR surface called the crust ; moreover thickness comparison showed a shrinkage of PR during implantation attributed to PR densification and sputtering.

These physical changes have been highlighted by XRR analyses and showing that densification is more pronounced for higher implantation energy. TOF-SIMS in-depth profiles of implanted PR have been compared to non modified PR. It revealed that the first decades nm-depth are clearly depleted in O and H and enriched in C (see fig.2) and that this modified layer corresponds to the crust layer observed previously by TEM. This result is in good agreement with XPS analysis showing that the dopants are present in the PR under their elemental (P or As) and their oxidized form but they are also bonded to carbon atoms of PR backbone. Moreover these modifications of PR structure and composition were directly related to the increase of hardness and elastic modulus observed by nanoindentation. Finally SRIM simulations carried out with different implantation conditions were compared with EDX and TOF-SIMS dopant in-depth profiles in order to understand more precisely the PR degradation mechanism. These simulations have shown that electronic stopping that leads to crosslinking phenomenon is predominant over nuclear stopping that drives the PR atoms displacements. This mechanism is also consistent with the densification observed by XRR.

Perspectives
Based on this understanding, plasma chemistries either reductive or oxidizing have been investigated. O$_2$-based chemistry is not efficient to remove dopants under their oxidized form; it remains oxidized dopants residues and moreover it generates the highest substrate consumption. On the other hand NH$_3$ (3% of H$_2$) plasma is the most suitable on this both criteria with a better efficiency to remove the crust layer but with the major risk to generate popping with thick PR. A tradeoff has to be found between residue left, substrate consumption and/or resist popping. Photoresist chemistry development are ongoing to meet these criteria.

FIG 1. TEM cross-section image of implanted PR (As 4keV)

FIG 2. ToF-SIMS analyses (Cs$^+$ beam) of implanted PR using (a) As 4 keV 2x10$^{15}$ atoms/cm$^2$, (b) P 4 keV 1.5x10$^{15}$ atoms/cm$^2$.

RELATED PUBLICATIONS:
Multi-Beam Lithography: Patterning Technologies with New Integration Challenges

RESEARCH TOPIC:
Lithography, Electron beam

AUTHORS:
S. Landis, I. Servin, M.L. Pourtreau, Y. Blancquaert, J. Pradelles, A. Bernadac, B. Dal'zotto,

ABSTRACT:
Massively parallel direct write E-Beam lithography technique is without any doubt an attractive alternative lithography technology. It offers a huge panel of competitive advantages, such as for example cost of ownership benefit, full writing flexibility opportunity and high-resolution potential. On this field, MAPPER Lithography remains the leading company pushing the insertion of this technology solution up to the industrial maturity. Through a joint partnership initiated in 2008 with MAPPER, CEA-LETI works to demonstrate the capability of the MAPPER technology by evaluating the pre-production FLX-1200 Mapper platform, through tool performance assessment, electron beam qualification with embedded metrology and inline metrology and process integration.

Context and Challenges
In the lithography landscape, extreme-UV (EUV) lithography technology recovered high credibility recently. However, its large adoption remains uncertain, because its infrastructure still requires significant development with pending question about the real associated costs. In this context, massively parallel electron-beam lithography remains highly attractive. Even if efforts are still needed to overcome the lithography side issues, the recent development introduced new challenges and opportunities for the integration schemes.

Main Results
The 2017 program was focused on the Metrology assessment based on Optical Critical Dimension approach (Scatterometry) [1], and on process-integration [2] development compliant with the single via layer (N40) for security application [3, 4].

The evaluation of scatterometry for monitoring non-uniformities potentially caused by multi e-beam Maskless Lithography (ML2) were investigated. Specific innovative scatterometry targets consisting of lines and spaces arrays with programed CD non-uniformity were manufactured. The scatterometry, or OCD (Optical Critical Dimension), spectra showed clear shifts caused by the regions with shifted CD.

The trends measured by OCD matched well with trends of the estimated CD (calculated from designs) as well as the trends extracted from scanning electron microscope (CD-SEM) measurements. Taking into account resist morphology variations across the wafer, correlations between OCD and CD-SEM of the weighted average CD are shown to be very good (figure 1(a)) and correlations for each pattern are done using the rigorous TMU analysis methodology (figure 1(b)).

The fully process/integration development for the N40 single via layer were assessed on dual damascene process employing porous low-k dielectrics, combined with copper metallization, using trench first metal hard-mask approach. Etch transfer into via layer was carried out on 300mm Capacitive Coupled Plasma Chambers dedicated to BEOL stack. Results achieved during this year demonstrated that the lithography exposure on FLX-1200 tool for via patterning integration is mature enough to start first customer demos for security application (figure 2).

 Perspectives
The next steps will consist to further qualify OCD but also standard image based overlay approaches to fully monitor CD variation within the beam stripe (2 µm wide) as well as stitching and overlay. Following the firsts success through the via 3 exposures, further investigations will be performed on lithography and etching processes to collect CDU and overlay data.

FIG 2. (a) 300mm Si wafer exposed on FLX-1200 multi-beam tool. (b) Top-view SEM image of via3 patterns on real product at CD ~ 80nm.

RELATED PUBLICATIONS:
Context and Challenges

After twenty years of development, nanoimprint lithography (NIL) remains as an attractive low cost patterning strategy and starts to be introduced in high volume manufacturing. Two well-established options are now available: the full wafer imprint and the step and flash imprint. The main challenges for the NIL technology are the master manufacturing (resolution and cost), the imprint materials (e.g. etching or optical properties) and equipments. Among these, the challenges addressed by Leti in 2017 were the integration capabilities of NIL with the distortion assessment, imprint material performances and master lifetime & manufacturing solutions. For these purposes, advanced qualification masters were manufactured for improved efficiency and cross qualification.

Main Results

The distortion in the nanoimprint process comes from the thermal expansion, the soft stamp handling and the lamination process. In collaboration with EVG, CEA-Leti has demonstrated the impact of each parameter on the overlay and showed the improvement path. The root causes identified, an improvement from 20 µm down to 1 µm have been demonstrated this year. This latter value raises the integration capabilities with mix and match approach needed by the program customers. Due to its cost, the life time of the Si master was improved. This life time can be increased with high performance anti-sticking layer (ASL) to prevent organic contamination of the features. In collaboration with Arkema, a new ASL, based on the grafted technology. This 7 nm layer was applied to a customer product to keep the defectivity of the master below 180 defects on 200 mm (fig. 1a) and to allow the replication and etching of 70 nm contacts (Fig.1b).

To prevent this low cost technology from suffering from mastering costs, innovative solutions for 3D and high resolution[2], combining implant and wet etching steps (patented), were developed by Leti.

Perspectives

In 2018 the goal is to use the wafer scale NIL technology for integration processes. This will require an improvement of the mastering capability, which will be supported by the other lithography programs [3], but also to reach a distortion down to 500 nm and to improve the overlay stability in order to guarantee a minimum yield on product functionality. For that purpose, CEA-Leti will increase its activity on master corrections and rules-based strategies [4] to further improve the process capabilities. Finally, the imprint material assessment will be strongly addressed, with the benchmark of the market's and R&D's solutions to be adapted to the applications: etching mask, permanent layer, high index materials, etc. The main topic will be the study of imprint resist diffusion into the soft stamp during imprint (up to 300 nm/min) and the surface adhesion characterization between the polymeric films.
DSA Lithography for Contact/Via Patterning

RESEARCH TOPIC:
Lithography, Directed self-assembly, Block copolymer

AUTHORS:

ABSTRACT:
Advanced surface affinity control for graphoepitaxy directed self-assembly (DSA) patterning is essential for providing a reliable DSA based solutions for the development of semiconductor patterning. An independent control of surface affinity between the bottom and the sidewalls of the topographical guiding structure was achieved by embedding an ultrathin layer in the guiding template stack. The DSA performances of this novel graphoepitaxy integration were evaluated by monitoring the success rate and the critical dimension uniformity of the shrunk contacts. This new integration, leads to the control of the polymer residual thickness (a few nanometers) and uniformity (inferior to 1nm) at the bottom of the guiding template that will facilitate the subsequent DSA pattern transfer.

Context and Challenges
Directed self-assembly (DSA) patterning is a promising solution for advanced lithography as a complementary technique to standard and future lithographic technologies (193nm immersion, multiple e-beam and extreme ultraviolet lithography). Although a great achievement has been made on material development and process optimization allowing major improvement in key patterning metrics (critical dimension uniformity (CDU), placement error (PE)), defectivity is still a major challenge for DSA insertion in the semiconductor manufacturing. In this context, we particularly investigated the potential of DSA to address a low-defect contact/via patterning using the 300 mm DSA pilot line available at CEA-Leti and Arkema’s microelectronics grade materials.

Main Results
We report here a novel DSA process flow for contact/via patterning allowing a perfect control of both the polymer sidewall and bottom thicknesses inside the guiding template and thus ensuring enhanced defect density after subsequent etching transfer to underlayers [1-4]. The process flow, as depicted in figure 1, is based on the DSA graphoepitaxy and planarization of polystyrene-b-poly(methyl methacrylate) (PS-b-PMMA) block copolymer (BCP) inside a typical silicon containing organic guiding template which judiciously integrate an embedded grafted layer of non-preferential affinity to the two blocks of the BCP.

FIG 1. DSA process flow of contact/via patterning based on an embedded polymer brush for advanced surface affinity control in graphoepitaxy by planarization [1]

Whereas the planarization enables a good uniformity of the BCP thickness with the guiding template density, the embedded grafted layer allows the control of the surface affinity at the bottom of the guiding template. Hence, fully opened contacts after PMMA removal are obtained with uniform and thin residual polymer thickness that is defined by the embedded brush layer. Figure 2 summarizes the key DSA performances achieved with a good CDU of less than 10 % of the mean CD and a free-DSA-defect area superior to 0.01mm² that represents more than 6x10⁵ of inspected valid contacts. From scanning transmission electron microscopy (STEM) images, the polymer residue thickness was measured at 7 nm with a good uniformity (∆σ = 0.6 nm) which corresponds to the embedded brush layer thickness. These results are at the DSA state-of-the-art for contact/via patterning by graphoepitaxy and show the potential of the technique to be adopted in high volume manufacturing.

TABLE 1: Main manufacturing parameters of DSA process. Top-down SEM and STEM images after PMMA removal [2]

Perspectives
Etching transfer and defectivity study will be implemented by using the low molecular weight brush layer which will lead to ultra-thin grafted layer thickness (=3 nm) allowing more efficient DSA pattern transfer.

RELATED PUBLICATIONS:
[2] Embedded neutral layer for advanced surface affinity control in graphoepitaxy directed self-assembly, F. Delachat et al., Nanoscale, under final revision, submitted in December 2017
**DSA Integration for Line/Space Patterning**

**RESEARCH TOPIC:**
Advanced Lithography, Directed Self-Assembly, Block-Copolymers, Line/Space Patterning

**AUTHORS:**

**ABSTRACT:**
Directed self-assembly of block-copolymers is one of the most promising solutions for advanced patterning of sub-10nm technology nodes. For its high-resolution capability, cost effectiveness and process compatibility, DSA continues to attract the semiconductor industry. Using the 300mm pilot line available in Leti and the Arkema’s advanced materials, this work investigated DSA process development and integration for line/space patterning.

**SCIENTIFIC COLLABORATIONS:** Arkema, Brewer Science, Screen, LTM

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**Context and Challenges**
Affordable, simple, versatile: Directed self-assembly (DSA) is still highly investigated as a sub-10nm features lithography technique for next generation node in the CMOS industry. From different integrations evaluated today, throughout literature, chemoepitaxy seems the consensus. The use of topographic gratings to direct the assembly, known as graphoepitaxy, can also provide well defined structures. Moreover, sub-10nm technology nodes require extremely aggressive resolution block-copolymers (BCPs).

**Main Results**
DSA graphoepitaxy patterning process was successfully implemented on the 300mm pilot line at Leti by using a PS-b-PMMMA lamellar BCP from Arkema (38nm pitch), and integrated in a process flow for the manufacturing of nanowire transistors. As illustrated in figure 1, different Si-active structures on SOI substrate (2 or 3 Si fins, length until 2µm) was achieved for the 20nm technology node [1]. Moreover, the efficiency of an innovative UV-assisted method was especially demonstrated for a precise control over the surface affinity of topographic gratings (guide sidewalls and bottom differentiation) [2]. In collaboration with Screen a DSA dedicated bake process with ultra-low oxygen concentration was implemented on the 300mm pilot line in order to improve the defectivity [3].

In order to address stacked Si nanowires devices first demonstrations of patterning have been achieved. As illustrated in figure 2 36nm-height Si/SiGe multilayer stack have been demonstrated (pitch = 38nm / CD = 15nm).

Sub-10nm technology nodes require more aggressive resolution BCPs called high-chi BCPs. In collaboration with Arkema and Brewer companies DSA proof of concept regarding two chemical platforms of BCPs have been established [4-5].

**Perspectives**
Electrical characterizations and process optimization are ongoing regarding Si nanowire devices. The developments will be intensified around the chemoepitaxy process flow to push it in the range of the sub-10nm resolution with the high-chi platform BCP materials.

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**RELATED PUBLICATIONS:**
MEMS, NEMS & RF COMPONENTS

- Large Scale Optomechanics for Sensing
- Self-sustained mems oscillator based on thermal piezoresistive back-action in p-type silicon nanogauges
- Germanium telluride phase-change RF switches
- Thin-film piezoelectric actuators for biological applications
- Microstructure of lead zirconate titanate (PZT)
Large Scale Optomechanics for Sensing

RESEARCH TOPIC:
Optomechanics, nanomechanical resonators, sensors, NEMS

AUTHORS:

ABSTRACT:
Cavity optomechanics has become a promising route towards the development of ultrasensitive sensors for a wide range of applications including mass and biological sensing. We have shown the potential of Very Large Scale Integration (VLSI) with state-of-the-art low-loss performance silicon optomechanical microdisks for real-world applications. We obtained microdisks exhibiting optical Whispering Gallery Modes (WGM) with a million quality factors. This was the result of a large modelling effort for unambiguous optical parameter identification and optimization. Our high-Q microdisks allow their Brownian motion to be resolved at few 100 MHz in ambient air. These results show our VLSI process is a viable approach for future high-end sensors.

SCIENTIFIC COLLABORATIONS: Paris Diderot (MPQ, group Ivan Favero)

Context and Challenges
Nanooptomechanical resonators have attracted much interest in the last decade and have shown orders of magnitude higher displacement sensitivities than electrically transduced resonators. Close-field optical readout offers very large bandwidth too, allowing for even more miniaturized, high-frequency devices. On-chip cavity optomechanics has been a privileged route towards quantum studies and has now become mature enough to reach a more applied realm, like mass or chemical sensing, as well as biosensing in liquid. Displacement sensitivity is proportional to optical quality factor and much work has been dedicated to the understanding of how this relates to both optical coupling losses. Nevertheless, potential misinterpretation of experimental data can remain if specific modelling is not developed for the low-loss regime. Moreover, industrial applications will require reaching state-of-the-art performance with VLSI processes and packaging.

Main Results
Silicon optomechanical microdisks were fabricated in an industrial-grade clean-room on 200 mm SOI wafers (Fig. 1). The main lithography level was performed by Variable Shape Beam (VSB) and the optical waveguides and resonators were patterned by Induced Coupled Plasma (ICP) dry etching. On-chip light coupling is compatible with standard silicon photonics packaging and uses grating couplers. The devices are the first optomechanical resonators fabricated on 200 mm wafers with VSB lithography, allowing for both high fabrication throughput and high patterning resolution: each wafer contains more than 120,000 optomechanical devices. Most measured loaded quality factors are in the high 100,000 s, and many resonances show quality factors above 1 million (Fig. 1). These figures are among the best measured in the literature with silicon disks of a few µm radius [1]. This is the result of a large modelling effort, in order to optimize both extrinsic (geometrical) and intrinsic (fabrication related) losses. In the high-Q regime, two degenerate optical modes can be observed, which needs to be properly modelled in order to unequivocally extract and optimize all relevant parameters [2]. Thermomechanical motion was then easily resolved at a few 100 MHz frequencies at ambient pressure (Fig. 2). Sufficient signal to noise ratio was obtained without the need for an optical amplifier with very low power.

FIG 1. Left: Scanning electron microscope image of a Si optomechanical disk. Right: optical spectrum with 1 million optical quality factor.

FIG 2: Thermomechanical spectra of three different disks vibrating in air.

Perspectives
These results show our VLSI process is a promising route towards real-world sensors with optomechanical devices: inertial sensing, single-particle mass sensing as well as biosensing in liquid are currently under way.

RELATED PUBLICATIONS:
[2] L. Banniard et al., Intermodal coupling in an optomechanical system, MME 2017, 28th Micromechanics and Microsystems Europe workshop, Uppsala
Self-Sustained Mems Oscillator Based on Thermal Piezoresistive Back-Action In p-Type Silicon Nanogauges

RESEARCH TOPIC:
Suspended Silicon Piezoresistive nanogauges can alter the mechanical response of a MEMS when they are electrically biased, because of Thermal Piezoresistive Back Action (TPBA)

AUTHORS:

ABSTRACT:
We report self-sustained motion of a low frequency MEMS resonator that leans on tiny p-type silicon piezoresistive nanowires, as a result of Thermal Piezoresistive Back Action (TPBA). In this device, a velocity-dependent force arises from physical coupling between mechanics and electronic transport in small conductive silicon beams because of self-heating. Up to date, only damping rate increase has been reported for p-doped silicon beams based MEMS resonators. So far, most papers required n-doped silicon beams to allow self-sustained oscillations. Yet, this work demonstrates self-sustained motion using p-doped silicon nanobeams as TPBA actuators under a constant bias voltage. The quality factor (QF) of the resonator increases from 28000 under vacuum to at least 1x10^6 for DC-bias voltage down to 190 mV. Self-sustained oscillations are observed above a threshold voltage of 200 mV corresponding to a power of 16 µW dissipated by Joule heating in the silicon nanobeam.

Context and Challenges
M&NEMS technology relies on the combination of a large MEMS part with tiny suspended piezoresistive silicon nanobeams used to read out its motion. Three-axis accelerometers, magnetometers or gyroimeters have then been designed to benefit from the large sensitivity provided by this technology. In this context, special attention is required to account for the influence of nanobeams on MEMS operation. When biased, silicon nanogauges can tweak the mechanical response of the structure because of a thermal piezoresistive back action effect [1]. Under vacuum, it has been shown that TPBA could totally offset damping rate for n-type doped silicon beams and could then lead the MEMS into self-sustained oscillations. The negative piezoresistive coefficient in n-type nanogauges has been pointed as the main prerequisite to achieve such operation regime. In the work performed at Leti, investigations have been carried out to extend self-sustained oscillations capability to p-type silicon nanobeams, despite a positive piezoresistive gauge factor. The possibility to actively reverse, amplify or cancel the damping rate of a MEMS structure appears to be a major achievement of the study.

Main Results
TPBA is usually described as a circular coupling between mechanical, electrical and thermal domains. As depicted in figure 1, a motion of the MEMS structure x induces a resistance modification through Joule effect. A thermoelastic force on the MEMS structure then arises from the motion x as a back action effect. The study described in [2,3] proposes a new analysis of this phenomena chain and highlights the role of biasing circuit in the control of the positive and negative damping rate tuning. It also unveils a biasing configuration capable of disabling TPBA effect, what appears to be a significant benefit for cases where no mechanical response change is desired. Finally and equally significantly, self-sustained oscillations have been observed for an operation point characterized by a power consumption in nanobeams as low as 16 µW, as anticipated in a previous study about TPBA power efficiency in silicon nanobeams [1]. Figure 2 reports the oscillations startup and stabilization with a starting time that can be controlled by the damping rate intensity.

Perspectives
TPBA in silicon nanobeams turns out to show a strong effect on MEMS mechanical response when operating at very low pressure (P<10^3 mbar) with low pneumatic damping factors. The study performed at Leti has demonstrated the ability to actively tune or even cancel this effect on M&NEMS devices. Self-sustained oscillations triggered at low power offer interesting perspectives for applications that require such ability, like gyroimeters or resonant sensing scheme based devices.

FIG 1. Signal chain of the TPBA effect. The circular physical coupling is initiated by the nanobeam electrical bias

FIG 2. Self-oscillations startup and stabilization phase. The signal is shifted from 6830 Hz down to 130 Hz by a Lock in Amplifier device (demodulation at 6700 Hz).

RELATED PUBLICATIONS:
Germanium Telluride Phase-Change RF Switches

RESEARCH TOPIC:
RF switches, Phase-Change Materials, GeTe

AUTHORS:
A. Léon, B. Reig, D. Saint-Patrice, N. Castellani, G. Navarro, V. Puyal, (F. Podevin, P. Ferrari, E. Perret)

ABSTRACT:
RF switches based on phase-change materials, such as GeTe, are an attractive solution to challenge conventional technologies such as MOS transistors, PIN diodes or RF MEMS. Their nonvolatile change in phase offers a solution to decrease energy consumption and to design complete circuits using GeTe switches for reconfigurability.

Context and Challenges
Switching is a key function in many RF and mm-wave circuits. In particular, at the front-end modules (FEM) level of new mobile networks, switches play a fundamental role for reconfigurability. Performing switches need low ON-state resistance $R_{on}$ and high OFF-state capacitance $C_{off}$. As a trade-off, the cut-off frequency $f_{cut} = 1/(2\pi R_{on}C_{off})$ is the main Figure-of-Merit for switches. Switching time, power consumption, reliability, power handling, linearity and ease of integration are also of major importance. Phase-change material based RF switches is a recent approach to challenge RF-MEMS and silicon-based technologies such as SOI.

Main Results
A phase-change RF switch, based on GeTe (Germanium Telluride) material was developed by CEA-Leti [1, 2, 3]. GeTe is a material that can change between two stable phases: a crystalline phase and an amorphous phase. This change in the phase is based on a thermal actuation applied through electrical pulses (Joule heating). It goes along with a change in resistivity of the material to obtain an electrically bi-stable device: a high resistivity for the amorphous phase (OFF-state) and a low resistivity for the crystalline phase (ON-state). GeTe is a good candidate for realizing RF switches because of its low ON-state resistivity (~$5 \times 10^5$ Ω.m), high $R_{off}/R_{on}$ ratio (~10$^5$) and fast switching time (~60 ns). Moreover change in phase is nonvolatile, so no power is needed to maintain the state of the switch offering a solution to decrease energy consumption. The developed devices are realized with materials and processes that are fully compatible with CMOS back-end-of-line and that can be considered for further integration. As shown in Fig. 1.a, the GeTe directly contacts the first metal layer in order to optimize electrical contact. A second metal layer is contacting the first one allowing line crossing for complex routing. S-parameters were measured for both ON and OFF-states from 40 MHz to 40 GHz (Fig. 2). The insertion is constant with frequency in the ON-state. It ranges from -0.1 dB to -0.12 dB from 40 MHz to -40 GHz for geometries shown in Fig. 1.b and Fig. 1.c. Isolation is lower than -15 dB up to 40 GHz. The cut-off frequency reaches 22 THz with $R_{on} = 1$ Ω and $C_{off} = 7 fF$. This is about an order of magnitude improvement compared to currently available switches.

Perspectives
The RF performance of GeTe switches is state-of-the-art and are highly promising to meet the future needs of switching functions of RF and mm-wave circuits. Evaluation of power handling capability and linearity of the devices will allow to validate overall performance and to design complete circuits using GeTe switches for reconfigurability.

RELATED PUBLICATIONS:

SCIENTIFIC COLLABORATIONS: Univ. Grenoble Alpes
Thin-Film Piezoelectric Actuators for Biological Applications

RESEARCH TOPIC:
MEMS; piezoelectric actuators; microfluidic; biological applications

AUTHORS:
F. Casset, B. Neff, V. Agache, N. Verplanck, F. Boizot, S. Fanget, (A. Millet)

ABSTRACT:
Micro Electro Mechanical System (MEMS) can address a large domain of applications in microfluidics and biology for sensing or actuation purposes. Thanks to the generation of mechanical waves, vibrating MEMS offer the possibility to control fluid flow inside a microfluidic cavity. Vibrating structures allow to create positions of stability called vibration nodes where flowing particles tend to stay, or can be used to study the physical properties of biological materials. This offers outstanding interest concerning manipulation of a large variety of particles from microbeads to living cells. We describe in this paper the development of a vibrating structure using thin-film piezoelectric actuators, immerged in liquid to operate in liquid media for microfluidic applications.

SCIENTIFIC COLLABORATIONS: INSERM

Context and Challenges
Lab-on-chip systems are in continuous development thanks to their capacity to carry out biological analysis and potentially further reduce time to diagnostics. In this domain, Micro Electro Mechanical System (MEMS) can bring new possibilities and functionalities to perform new biological assays. In particular, we present the development of a lab-on-chip system leveraging local acoustic vibrations produced by thin-film piezoelectric actuators in liquid media.

Main Results
The core of the device is composed of thin-film piezoelectric Aluminum Nitride (AlN) actuators deposited onto a glass substrate. The device is embedded into a microfluidic hermetic packaging enabling its implementation in liquid media for biological applications (Fig. 1).

The electromechanical characterization of the device is performed using a Polytec Laser Doppler Vibrometer (LDV). Two out-of-plane Lamb modes have been identified thanks to vibrometry measurements at the center of the plate. For each one of the modes, the measurement results, in good agreement with FEM simulations, show a mass loading effect of the liquid media on the resonant frequency as it is shifted towards lower frequencies (Fig. 2). The displacement amplitudes of the Lamb modes measured in liquid are relatively close to their values measured in air: for example, an amplitude of 5.4 nm is obtained in liquid for the Lamb mode with 6 nodes measured in liquid under only 20 Vrms, for a reference value of 6.4 nm in air. This limited reduction (by 15%) confirms that Lamb waves are well suited for implementation in a liquid environment.

To optimize the performance obtained on the Lamb mode with 6 nodes, we studied the influence of the sealing material on the displacement amplitude. We measured that the vibration amplitude increases with the stiffness of the seal (Fig. 3). Thus a 190µm thick plastic seal is selected for our packaging.

Perspectives
We aim to mechanically stimulate biological materials with our system in a close future. Indeed electromechanical characterization in liquid media reveals that it meets literature specifications in terms of resonant frequency and displacement. This device paves the way for an easy to use system able to apply and control mechanical stimuli to biological cells. As a prospective point of view, we expect that using acoustic waves generated by thin-film piezoelectric actuators could be leveraged for assessing biological cells physical properties at the population scale. This system can be used to measure the viscosity, in patterning of cell surfaces and stimulation of adherent biological cells.

RELATED PUBLICATIONS:
Microstructure of Lead Zirconate Titanate (PZT)

**RESEARCH TOPIC:**
PZT, surface, interface, electrodes, dielectric, piezoelectric and pyroelectric applications

**AUTHORS:**

**ABSTRACT:**
We aim at identifying and explaining physicochemical phenomena that could inhibit the integration of Lead Zirconate Titanate (PZT) film in Metal-Insulator-Metal (MIM) structures for piezoelectric, pyroelectric and dielectric applications. This study has enabled us to highlight several aspects such as the presence and the composition of nanostructures, the variation in the texture and in the morphology of the PZT layers depending on the lead excess and the presence of interface phases and residual Pb oxide in Pt/Ru/PZT/Pt capacitors. The electrical performance of PZT-based MIM capacitors is a sensitive function of the Pb excess used in the precursor solution during synthesis.

**SCIENTIFIC COLLABORATIONS:** Synchrotron-SOLEIL, LIST

**Context and Challenges**
Lead zirconate Titanate Pb(ZrxTi1−x)O3 (PZT) is an ideal candidate for applications such as piezoelectric actuators, infrared pyroelectric detectors, and decoupling capacitors. Lead loss occurring during the crystallization annealing steps requires excess lead precursor for obtaining the near stoichiometric values. This may lead to changes in surface composition and hence modifications of the PZT/electrode interface chemistry. We investigated the influence of the surface microstructure and chemistry of sol-gel grown PbZr0.52Ti0.48O3 on the electrical performance of PZT-based metal-insulator-metal (MIM) capacitors as a function of Pb precursor excess.

**Main Results**
Figure 1 shows the surface microstructure of PZT deposited with Lead excess set to 10, 15, 20, and 30%. Low Pb excess gives rise to a nanostructures phase layer on a (100) textured PZT film. At high Pb excess (above 15%), the nanostructures disappear while the PZT grain size increases and the film texture becomes (111) orientation.

![SEM images of as deposited PZT](image)

**FIG 1.** SEM images of as deposited (a) PZT10, (b) PZT15, (c) PZT20, and (d) PZT30.

As shown in Figure 2, the capacitance density, dielectric losses and breakdown voltage are significantly influenced by the amount of Pb excess [1].

![Capacitance density and loss tangent](image)

**FIG 2.** Maxima of surface capacitance density and loss tangent (left) and EBD (right) as a function of Pb excess.

Using quantitative X-ray photoelectron spectroscopy and transmission electron microscopy, we were able to detect the presence of either ZrOx or PbOx surface phase depending on Pb excess amount (Figure 3). By carrying out operando hard X-ray photoelectron spectroscopy of the top interface in a Pt/Ru/PZT(220 nm)/Pt capacitor structure, we found that the presence of ZrO1.89 nanostructures at the surface of the bare sol-gel film acts as a dead layer in the dielectric structure and reduce screening of the surface polarization charge in PZT capacitor [2]. A large Pb excess induces the presence of residual lead oxide phase, thus contributing to a reduction of both capacitance and breakdown voltage. These results show that the optimization of PZT via the elimination of parasitic ZrOx and PbOx phases are needed to improve performances in view of an optimal use of PZT in capacitor based applications.

![Cross section of Pt/Ru/PZT interface](image)

**FIG 3.** Cross section of Pt/Ru/PZT10 interface: (a) High-resolution bright TEM and (b) EDX analysis

**Perspectives**
Thermal treatment is often performed after patterning capacitors. This annealing has been shown to impact electrical behavior of capacitors, probably as a result of modification of interfacial states. This is under current investigation, in particular through TEM/EDX analyses of the Pt/Ru/PZT interfaces.

**RELATED PUBLICATIONS:**
• Tunneling Approach to the operation of CMOS compatible GaN heterojunction diodes

• Developments of surface passivation and protection layers for gallium nitride based structures

• Advanced GaN based power devices dynamic characterizations

• New thin film electrode materials for lithium(-ION) solid-state microbatteries with customized voltage

• III-V on Si multi-junction solar cells by wafer bonding
Tunneling Approach to the Operation of CMOS Compatible GaN Heterojunction Diodes

RESEARCH TOPIC:
CMOS compatible GaN on Silicon devices physics for power conversion and radio-frequency applications.

AUTHORS:

ABSTRACT:
Due to their wide band gaps, III-N materials can exhibit behaviors ranging from the semiconductor class to the dielectric class. Through an analogy between a GaN heterojunction diode and a MOS contact, we make use of this dual nature to capture the essence of the heterojunction in a straightforward way. In combination with a quantum transport formalism, we show that the fabricated power diode operates as a pure tunnel diode in contrast to its Schottky diode designation. It is demonstrated that in the forward conduction regime, tunnel events account for transport at room temperature and at 150°C. Note that the highest temperature used is representative of harsh environments within which such power devices are expected to bring major benefits in the context of energy conversion.

Context and Challenges
At the core of most power and radio-frequency GaN devices lies the AlGaN/GaN heterojunction due to its exceptional properties, in particular the existence of a two-dimensional electron gas. Thanks to the combination of high carrier mobilities and the capability to withstand high critical electrical fields, wide band gap III-N heterojunction devices are extremely promising for applications in areas such as electrical transportation, solar and consumer power conversion or in the emerging 5G market. To address such applications, CEA-Leti has developed a 200 mm CMOS compatible GaN on Silicon fabrication line, from GaN growth and processing to device characterization. Today, with the increase in process maturity, device evolution and optimization requires a deeper understanding of the physics of this new generation of wide band gap devices.

Main Results
Two main active components enter any power converter: transistors and diodes. In the context of this study, the focus was set on the transport properties of a 10A/650V GaN power diode fabricated at CEA-Leti, especially on the transport features in the forward conduction regime (on state). Through an analogy between the GaN heterojunction and a MOS contact, a direct path was found to capture the energy landscape of the heterojunction. Moreover, by using an approach involving quantum transport known as the Landauer formalism and electron transmission probability calculations, it was shown that the power diode is the stage of tunnel events in the on state from room temperature to 150°C [1]. As can be seen in figure 1, the diode current is reproduced across 10 orders of magnitude at 300K and 425K, allowing to describe the sub turn-on regime and the linear operation. All calculations involve material parameters known from literature in combination with experimental measurements carried out in line. Once the calculation is calibrated at a given temperature, a single free parameter remains, the series resistance. We emphasize that the model and results obtained contrast with the common approach found in literature which relies on thermionic emission which in the present case is ruled out. In essence, the power diode fabricated and often referred to as a Schottky diode consists of a pure tunnel diode.

Perspectives
Thanks to the successful quantum modelling of the power diode, a robust physical picture was given as far as transport in the on state. The proposed approach allows first to account for the diode’s turn-on voltage tunability which permits to foresee various applications, from free-wheeling diodes to ESD protection diodes as discrete or cointegrated devices. Beyond, the model presented is not limited only to diodes and can be applied to power and RF transistors where the gate and ohmic physics are already been explored and quantified. Additionally, tunnel diodes may also address ultra-fast rectification by taking advantage of quantum tunneling. At 100 GHz and beyond, a rectenna (diode coupled to an antenna) could in principle rectify infrared light and allow energy harvesting from thermal sources. A perspective GaN diodes could fulfill. Finally, we emphasize that beyond such modelling approaches, device simulations using 2D TCAD calculations [2] are also the subject of intense efforts to support the understanding of the physics of GaN power architectures developed internally.

RELATED PUBLICATIONS:
Developments of Surface Passivation and Protection Layers for Gallium Nitride Based Structures

RESEARCH TOPIC:
Passivation and protection of GaN layers for improved device performance, and for advanced processing such as implantation

AUTHORS:

ABSTRACT:
Lett development of III-N high power transistor and diode devices require that all areas of the device structure are optimized to ensure the highest performance. A specific focus this year was the optimization of the passivation layer that caps and protects the active layers of HEMT structures which are particularly sensitive to surface effects. This layer should be morphologically and electrically stable, so that complicated components can be produced directly without further treatment. This work has enabled the development of robust capping layers which allow activation of implanted atoms in GaN layers using high temperature annealing without degrading the surface morphology of the layers.

Context and Challenges
One important strength of silicon based MOS technologies is the formation of a high quality oxide layer on the surface. This stabilizes the silicon surface with an amorphous layer, and enables high quality processing. A suitable oxide has not yet been demonstrated for gallium nitride, and so an alternative must be used in order to passivate and protect the surface. Implantation is a specific challenge which shows the requirement of these protective layers. When atoms are implanted into GaN layers, annealing must be performed in order to heal defects and activate these dopant atoms. As GaN has strong atomic bonds, this anneal needs to be at high temperature, which can degrade the surface if it is insufficiently protected.

Main Results
Lett power devices based on GaN use a thin (~25 nm) AlGaN layer on GaN, which produces a 2-dimensional electron gas (2DEG) at the interface between the two layers. This electron gas has very high mobility and a high electron density, enabling low resistance and high frequency devices. However, this AlGaN layer is very sensitive to surface effects, and so needs a capping layer, to protect it. We investigated GaN caps, SiN caps and a combination of the two.

Figure 1 shows that from the rough un-capped AlGaN, our growth of SiN capping gives high quality, smooth layers, even after only 1 nm of growth. This excellent morphology is conformal and amorphous, as shown in the TEM image on the left of fig. 2, and this layer also ensures that we maintain the electrical properties. GaN cap layers also gave very good surfaces, but they increased the sheet resistance of the 2DEG. When combining GaN and SiN layers, we created pits in the GaN cap, as seen in Fig. 2 (right), and this structure also degraded leakage properties in processed power diodes. We have therefore shown that our high quality SiN caps give excellent morphology, sheet resistance and device performance, and these are now integrated into our devices.

Perspectives
The high quality SiN capping layers developed at Leti give excellent morphology and electrical properties. This guarantees high performance devices across the processing steps, and also allows the integration of advanced processing steps such as implantation into the process flow. Implantation brings a new flexibility to process integration, which can take Leti to a new level of performance in our devices.

RELATED PUBLICATIONS:
Advanced GaN Based Power Devices Dynamic Characterizations

RESEARCH TOPIC:
GaN HEMTs, GaN based Schottky diodes, Power transistors, Current collapse, Dynamic Ron, DLTS.

AUTHORS:
W. Vandendaele, T. Lorin, P. Ferrandis, F. Gaillard

ABSTRACT:
Let us developments of high power transistor and diode devices require all parasitic effects during AC operation to be suppressed or at least minimized as much as possible. Active traps located in the GaN buffer, at semiconductor/passivation interfaces or in the volume of inter-metal passivation can induce so called “current collapse” effect which leads to a dynamic increase of the on-resistance after an electrical stress. This year, we have worked on developing new setup to characterize dynamically the GaN based devices. These novel advanced methodologies, such as fast dynamic Ron measurements or DLTS, enable the extraction of the traps properties in the structure (position, energy).

SCIENTIFIC COLLABORATIONS: STM Tours

Context and Challenges
GaN is now considered as the most promising candidate for medium power (650 V rated and below) and high frequency (>1 MHz) operations with nearly no switching losses. Trapping effects in the structure can increase dramatically the switching and conduction losses. This parasitic dynamic effect, called “current collapse”, is recoverable within time range of 1 µs to several ks. This year, a strong effort has been made on setting up GaN dedicated fast Ron, dynamic measurement as well as DLTS to study the amount of parasitic trapping as well as its intrinsic properties.

Main Results
No commercial SMUs solution allows the dynamic Ron measurement on devices below the millisecond at wafer level. We developed a µs dedicated solution (Fig. 1) which embeds a clamping circuit to measure accurately the on-resistance of the device after a switching from high voltage state to on state.

FIG 1. Test setup dedicated to ultrafast dynamic Ron measurement on GaN based Schottky diodes

This test setup has been used to perform dynamic Ron measurement on Schottky diodes with various cathode field plates configurations (Fig. 2). We managed to extract the normalized Ron = 10 µs after the switching from OFF to ON state as a function of the reverse voltage value (from 50 V to 750 V). We demonstrated the influence of the cathode field plate length on the resistance increase. The longer the field plate, the stronger the parasitic effect is.

FIG 2. (a) Schottky diode on GaN on Si wafers cross view and (b) Evolution of dynamic Ron (10 µs) under increasing reverse voltage for three cathode field plate configurations (b) Evolution of dynamic Ron (10 µs) under increasing reverse voltage for three cathode field plate configurations.

We determined that the traps related to this effect were located in the buffer layers and in the SiN underneath the field plate. It is hence needed to shorten the field plate as much as possible. Capacitance DLTS was also used to point out the existence of ICP-RIE induced damages under the Schottky contact (Fig. 3).

FIG 3. Arrhenius plots extracted from C-DLTS measurements showing ICP-RIE induced traps below the anode contact in partial recess.

The traps properties (Ea, σ) were extracted and revealed the presence of deep level states underneath the anode. These latter states can be related to dynamic instabilities under operating conditions of the diode.

Perspectives
The advanced electrical characterization methodologies can give precious information on the parasitic effects arising in GaN based devices. This work will allow us to initiate further improvements on the device itself and on the epitaxial buffer. Novel characterization setup such as thermal recovery transients after a reverse/blocking state will be developed.
New Thin Film Electrode Materials for Lithium(-ION) Solid-State Microbatteries with Customized Voltage

RESEARCH TOPIC:
All-solid-state lithium(-ion) microbatteries

AUTHORS:
F. Le Cras (B. Pecquenard)

ABSTRACT:
New thin film positive electrode materials for microbatteries were developed as alternatives to the ‘4 V’ LiCoO₂ material in order to meet particular specifications in terms of output voltage. Thus, Nasicon-type iron molybdate Feₓ(MoO₄)₂ and Li₁ₓMn₂₋ₓO₃ spinels undergoing a two-phase reaction upon lithium intercalation, were prepared as thin film electrodes in order to produce a very flat discharge profile at ~ 3V. Lithiated titanium oxysulfides, delivering high volumetric capacities at ~2.5 V thanks to an unusual dual cation- and anion-based redox process were studied as low-voltage cathodes for solder-reovable Li-ion microbatteries.

SCIENTIFIC COLLABORATIONS: ICMCB, IPREM

Context and Challenges
All-solid-state thin film batteries, manufactured by sequential deposition of thin films using vacuum deposition techniques such as sputtering, are particularly attractive when a reduced footprint, a very low thickness, a thermal and mechanical resistance, and/or a high integration with microelectronic components is required. Up to now, all microbatteries available on the market are based on the (Li)/LiPON/LiCoO₂ tripych which has a sloppy discharge curve at ~ 4 V. In order to fulfill new needs in terms of voltage profiles for specific applications, and particularly needs for a lower nominal voltage and/or flat discharge curves, different positive electrode materials had to be designed and synthesized to replace the LiCoO₂ intercalation compound.

Main Results
A particular demand for a lithium cell able to deliver a stabilized voltage at 3 V during operation has motivated the study of metal oxides systems undergoing a two-phase reaction during lithium intercalation. Two systems were identified: (i) Feₓ(MoO₄)₂-LiₓFe(xMoO₄)₂ with a NaSICON-type structure and (ii) Li₁ₓMn₂₋ₓO₃-LiₓMn2₋ₓO₃ spinel-type materials. Amorphous thin films of stoichiometric Feₓ(MoO₄)₂ and Li₁ₓMn₂₋ₓO₃ were deposited from targets manufactured in-house, and crystallized at moderate temperatures (~ 600°C). The voltage profile obtained for these thin films electrodes was actually a flat plateau at 2.95-3.05 V/Li/Li, with a delivered capacity of 62 and 30 µAh.cm⁻².µm⁻¹ respectively for Li₁ₓMn2₋ₓO₃ and Feₓ(MoO₄)₂. Finally, due to limitations of the Li⁺ and electronic transport to structural fatigue related to the two-phase process itself, the capacity retention was found to be quite limited. Besides, a new system has been developed with the aim to obtain a low-voltage, high-capacity lithiated positive electrode material for solder-reovable Li-ion microbatteries. Amorphous lithium titanium oxysulfide thin films were synthesized from Li-Ti-S targets. Their operation in all-solid-state cells has highlighted the contribution of two reversible redox systems upon delithiation, Ti⁺³/Ti⁺² and S₂⁻/S₂⁻, with a capacity ratio depending on their initial composition. As an example, Li₁ₓTi₀.₃S₂.₁ electrodes were found to deliver a very high and stable capacity of 80 µAh.cm⁻².µm⁻¹ [1.5-2.8V/Li/Li] in solid-state µ-batteries and proved to be perfectly resistant to the solder-reflow.

![Graph of charge/discharge curves and capacity retention of a Li/UPON/Li₁ₓTi₀.₃O₁₀.₁ microbatteries using a dual sulphide- and titanium-based redox process](image)

Perspectives
The output voltage, but also other features of the solid-state microbatteries are highly dependent on the composition and the structure of the thin film electrode materials. The proper design and synthesis of the latter, although not straightforward, are key elements to adapt the performance of these micro-power sources to specific needs and offers numerous capacities.

RELATED PUBLICATIONS:
III-V on Si Multi-Junction Solar Cells by Wafer Bonding

RESEARCH TOPIC: Multi-junction photovoltaics, III-V materials, silicon, wafer bonding


ABSTRACT: We have developed III-V on Si multi-junction solar cells with high photovoltaic power conversion efficiency. The silicon subcells were produced by diffusion or implantation doping processes in collaboration between CEA Leti and CEA-LITEN. III-V subcells, grown by epitaxy on GaAs substrates by our partners (III-V Lab, Fraunhofer ISE or IQE), were reported on Si cells by direct wafer bonding between GaAs and Si materials, which allows for a permanent, electrically conductive and optically transparent interface. After removal of the GaAs substrates, III-V on Si solar cell devices were fabricated, and characterized with a methodology developed in collaboration between CEA Leti and CEA-LITEN. We produced 2-terminal dual-junction (2J) AlGaAs/Si and triple junction (3J) GaInP/GaAs/Si solar cells with power conversion efficiencies under 1-sun beyond 21% and 25%, respectively.

SCIENTIFIC COLLABORATIONS: CEA-LITEN (INES), LTM, III-V Lab, Fraunhofer ISE, IQE

Context and Challenges
Multi-junction solar cells combining high bandgap materials with a Si bottom subcell offer the potential to increase the solar energy conversion efficiency beyond the 30% single-junction theoretical limit, and are predicted to enter the market by 2021. III-V solar cells are known to be highly efficient and have excellent proven reliability, which makes them a good high bandgap material candidate. However, the development of III-V on Si solar cells has historically proven to be challenging. The 4.1% difference in lattice constant between Si and GaAs and the non-polar to polar interface lead to threading dislocations and anti-phase domains, respectively. Wafer bonding has attracted growing interest as it enables the electro-mechanical combination of lattice and thermal expansion mismatched materials with electrically conductive, transparent bonds.

Main Results
We have studied three different bonding approaches:
(i) The most straightforward, direct GaAs/Si wafer bonding, leads to a defective bonding interface and poor solar cell performance;
(ii) An innovative approach combining epitaxy of GaAs bonding layer on Si cell followed by GaAs/GaAs direct wafer bonding under secondary vacuum leaves a nearly defect-free bonding interface. The hetero-epitaxy defects were advantageously confined to the bonding layer and did not propagate into the III-V layers. However solar cell performance was limited, probably by the presence of oxide at the interface.
(iii) Best solar cell performance was obtained using ultra-high vacuum Surface-Activated GaAs/Si wafer bonding (SAB), which gives an oxide-free low defective GaAs/Si bonding interface (Fig. 1, left). We have optimized the power conversion efficiency of two-terminal III-V on Si multi-junction solar cells prepared with Surface-Activated Bonding. The implementation of a new III-V cells design, a double layer anti-reflective coating and the reduction in GaAs bonding layer thickness allowed more photons to be absorbed in the Si bottom subcell, thereby increasing the photocurrent and improving the current match between the different subcells.

We have developed a fast and low cost new I-V characterization methodology. We measured power conversion efficiencies under 1-sun beyond 21% and 25% for 2-terminal dual-junction (2J) AlGaAs/Si and triple junction (3J) GaInP/GaAs/Si solar cells, respectively. Under low concentration illumination conditions, the 3J solar cell efficiency was over 28%.

Perspectives
SAB tool hardware upgrade would be needed for further development in order to improve the 100mm bonding condition into the 200mm Leti SAB binder. Further optimization of the anti-reflective coating layer, Si and III-V subcells design is needed in order to improve the current matching and devices performance. Optimization of Si subcell should take into account these two requirements: (i) good quality bonding interface and robust bonding process; (ii) highly doped emitter in order to have a field effect passivation / low effective surface recombination velocity at the III-V/Si interface. The development of implantation doping processes, allowing more flexibility to tune the doping profiles, and lower surface roughness, is promising for increasing the performance of wafer bonded III-V on Si solar cells.

RELATED PUBLICATIONS:
EMERGING MATERIALS AND PROCESSES

- GeSn epitaxial growth optimization for light emitting devices
- A versatile CVD route towards WS₂ monolayers
- DNA-templated conductive metallic nanowires (NWS)
- Area selective plasma enhanced atomic layer deposition
- Full control of Ge epitaxy processes and substrate design open paths to innovative devices
- Technological enhancers for CMOS-compatible contacts on III-V and Ge
- Low temperature CVD materials for 3D and sensing
- Methodologies development for advanced chemical planarization processes
GeSn Epitaxial Growth Optimization for Light Emitting Devices

RESEARCH TOPIC:
Germanium tin, low temperature epitaxial growth, step-graded structures, photonics

AUTHORS:
J.M. Hartmann and J. Aubin

ABSTRACT:
Germanium, a column-IV semiconductor, can be alloyed with tin, a semimetal, in order to obtain a direct bandgap semiconductor. For that, the Sn content should be high (> 12%, typically) and the residual compressive strain low (such layers are indeed grown on Ge-buffered Si substrates). However, the epitaxy of thick, high Sn GeSn layers is far from being trivial given the low solid solubility of Sn in Ge (< 1%), the 14% lattice parameter difference between Ge and Sn and the surface segregation of tin. To overcome these hurdles, we have used really low growth temperatures (in the 300°C–350°C range) and dedicated precursors (GeH₄ and SnCl₄) to deposit step-graded GeSn heterostructures on Ge buffers. Such high quality stacks enabled us to fabricate suspended GeSn micro-disks that lased at 3.1 μm up to 180K under optical pumping.

SCIENTIFIC COLLABORATIONS: CEA-INAC, Grenoble, Paul Scherrer Institute - Villegen, ETH - Zürich and Applied Materials

Context and Challenges
The race is on for the fabrication of electrically pumped GeSn lasers operating at room temperature with a reduced threshold since the demonstration in 2015 of (i) a direct bandgap in thick, high Sn content GeSn layers and (ii) optically pumped lasers monolithically integrated on Ge Strain-Relaxed Buffers (SRBs), themselves on Si(001) substrates. In the following, we will show how optimized heterostructures gave us the means of obtaining state-of-the-art GeSn 16% micro-disks that lased at 3.1 μm up to 180K [1].

Main Results
We have started this optimization by investigating the low temperature epitaxy of high Sn content GeSn alloys in a 200 nm industrial Reduced Pressure - Chemical Vapor Deposition tool from Applied Materials. Gaseous digermane (Ge₂H₆) and liquid tin tetrahalide (SnCl₄) were used as the Ge and Sn precursors. The impact of temperature (in the 300–350°C range), GeH₄ and SnCl₄ mass-flows on the GeSn growth kinetics at 100 Torr was thoroughly explored [2]. Be it at 300°C or 325°C, a linear GeSn growth rate increase, together with a sub-linear Sn concentration increase occurred as the SnCl₄ mass-flow increased, irrespective of the GeH₄ mass flow (fixed or varying). We otherwise studied the impact of temperature, in the 300–350°C range, on the GeSn growth kinetics. The GeSn growth rate exponentially increased with the temperature, from 15 up to 32 nm min⁻¹. Meanwhile, the Sn content decreased linearly as the growth temperature increased, from 15% at 300°C down to 6% at 350°C.

We have then grown various thickness GeSn layers (in the 30 - 480 nm range) on Ge SRBs. Growth temperature was changed in order to probe various Sn contents: 325°C for 10%, 313°C for 12% and 300°C for 15% of Sn. A dramatic degradation of the film was evidenced when the Sn concentration and layer thickness were too high, resulting in rough/milky surfaces and significant Sn segregation [3]. The epitaxy of really high Sn content (i.e. 16%) GeSn alloys was investigated in [4]. First of all, a specific GeSn strain relaxation mechanism was evidenced in a 465 nm thick, nominally single Sn content GeSn layer. Although growth conditions did not change, X-Ray Diffraction and cross-sectional Transmission Electron Microscopy measurements showed the presence of a lower Sn content (~12%) GeSn layer in the highly defective region close to the Ge/GeSn interface and a higher Sn content (~16%) GeSn layer on top. This structure was compared to a step-graded one, with a 180 nm thick GeSn 16% layer on top. The benefit of using a step-grading in terms of crystalline quality and surface morphology was conclusively demonstrated. A gradual strain relaxation in the grading occurred, minimizing Sn segregation/precipitation and confining misfit dislocations in it, as shown in Figure 1. This very structure was used to fabricate [1] optically pumped laser.

Sn content GeSn layer. Although growth conditions did not change, X-Ray Diffraction and cross-sectional Transmission Electron Microscopy measurements showed the presence of a lower Sn content (~12%) GeSn layer in the highly defective region close to the Ge/GeSn interface and a higher Sn content (~16%) GeSn layer on top. This structure was compared to a step-graded one, with a 180 nm thick GeSn 16% layer on top. The benefit of using a step-grading in terms of crystalline quality and surface morphology was conclusively demonstrated. A gradual strain relaxation in the grading occurred, minimizing Sn segregation/precipitation and confining misfit dislocations in it, as shown in Figure 1. This very structure was used to fabricate [1] optically pumped laser.

Perspectives
Thick, constant composition or step-graded GeSn layers with SiGeSn claddings are nowadays being used to the fabrication of even higher performance micro-disks, photonics crystals, suspended micro-bridges (with corner cube mirrors and strain tuning Ge arms), p-i-n photodetectors and so on.

RELATED PUBLICATIONS:
A Versatile CVD Route towards WS$_2$ Monolayers

RESEARCH TOPIC:
2D materials, transition metal dichalcogenides, chemical vapor deposition, precursor chemistry.

AUTHORS:

ABSTRACT:
A novel CVD approach for the synthesis of 2D WS$_2$ layers was developed using tungsten hexacarbonyl and 1,2-ethanedithiol (EDT) as precursors. This inexpensive and relatively safe “cocktail” allowed to deposit an ultrathin (ca 1 to 2 nm thick) organometallic layer, able to decompose into a 2D WS$_2$-layer upon thermal annealing. After preliminary studies allowing to get more insight into the decomposition mechanisms of this intermediate organometallic layer, further investigation have been performed on sapphire substrate, leading to a better understanding of growth mechanisms.

SCIENTIFIC COLLABORATIONS: CPE Lyon (C2P2), CEA INAC, “2D Factory project

Context and Challenges
The growth of 2D dichalcogenides (MoS$_2$, WS$_2$ and others disulfides) by scalable deposition methods, compatible with wafer manufacturing, is a great challenge for the introduction of disruptive nanoelectronic devices. Therefore, we have collaborations with chemists (at CPE Lyon) aiming to develop "green" chemistries for 2D disulfides synthesis, like new sulfur-containing molecules as alternative to the highly toxic H$_2$S. More broadly, we show here the added value of molecular engineering to bring new solutions for emerging materials.

Main Results
Previous studies performed at CPE Lyon had shown the relevance of 1,2-ethanedithiol as sulfur source in the atomic layer deposition of 2D MoS$_2$ layers. Since this process is not directly transposable to WS$_2$, a CVD approach based on the thermal activation of a W(CO)$_6$/1,2-ethanedithiol (EDT) vapor mixture on silica surface was implemented.

Reacting W(CO)$_6$ with 1,2-ethanedithiol at 220°C on a silica surface lead to the formation of a smooth and amorphous organometallic film [1] that can be converted into WS$_2$ upon thermal annealing at 800°C (Fig. 1).

Using this approach, we were able to obtain a uniform and oriented WS$_2$ bilayer over amorphous SiO$_2$ substrate (cf. Fig.2 for in-plane TEM and Raman spectrum).

Perspectives
Work is in progress to further optimize the annealing step in order to suppress defects in the lattice (sulfur vacancies) and improve the grain size of 2D dichalcogenides.

FIG 1. Proposed decomposition mechanism leading to WS$_2$ by thermal decomposition of a 1,2-ethanedithiolate intermediate.

FIG 2. (a) In-plane TEM view (b) Raman spectrum of the WS$_2$ bilayer obtained on SiO$_2$ substrate after annealing at 800°C.

FIG 3. (a) Monitoring of the W(CO)$_6$ adsorption plateau on SiO$_2$ substrate by WDXRF between 150°C and 220°C; (b) Infrared study of the deposition mechanisms (in the C≡O vibration range).

RELATED PUBLICATIONS:

DNA-Templated Conductive Metallic Nanowires (NWS)

ABSTRACT:
Metallic conductive nanowires (NWs) with DNA bundle core are prepared thanks to a process relying on DNA strand alignment on patterned electrodes followed by a physical vapor deposition (PVD) metallization. Bundles of DNA are suspended between 2 μm high parallel electrodes with separating gaps ranging from 800 nm to 2 μm. The suspended bundles are then metallized with Ti/Au bi-layers leading to NWs having a width ranging from a few nanometers up to 80 nm. The electrical behavior of the 60 and 80 nm width metallic NWs is ohmic and a resistance of about few ohms was established for the 80 nm width NWs, opening exploration fields for applications in microelectronics.

SCIENTIFIC COLLABORATIONS: CEA A3DN flagship (Leti/INAC)

Context and Challenges
DNA (Deoxyribonucleic Acid) is a nanometer-scale biomaterial with two main properties, that are self-assembly and possibility to be functionalized, which is also well known through its origami. Since the first attempt by Erez Braun in 1998 to achieve a metallic NW with doubled-strand DNA (ds-DNA), many researches, mainly involving a reduction of metallic cations around ds-DNA, have been attempted [1]. However, this approach uses a specific chemistry for each deposited metal and is so limited to some metals. In this work, we developed a versatile process relying on two steps: first ds-DNA are aligned and suspended between electrodes, second DNA bundles are covered with metallic layers deposited by PVD e-beam evaporation [2].

Main Results
DNA bundles were suspended between electrodes patterned within a 2 μm thick photoresist on a silicon substrate. A droplet of solution containing DNA was positioned on an electrode set followed by an evaporation step leading to suspended DNA bundles anchored to the top of electrodes. The deposition process involves two metal deposition steps: a titanium layer is deposited first to insure attachment of the gold following layer to the biomaterial. Different stacks were so realized with Ti and Au layer thicknesses ranging from 2 to 10 nm and 2 to 100 nm respectively. The NWs width was measured by SEM and was ranging from 16 nm to 80 nm leading to an estimated average DNA bundle core of about 10 nm. The process has demonstrated a good repeatability and sets of regular spaced NWs were obtained by this method (Fig. 1).

Electrical characterizations of the NWs have shown that NWs with diameter lower than 50 nm were burned during the test, while NWs with greater diameters exhibited an ohmic behavior (Fig. 2). For 80 nm diameter NWs, the electrical resistances were in the range of few ohms, however contact resistances between the suspended NWs and the electrodes were generally greater.

Perspectives
This last point is the main way of process improvement. Moreover, NWs cross-section must be observed by TEM to refine the NWs shape model that will permit to calculate resistance of the NWs accurately.

FIG 1. SEM images of NWs: 60 nm width (left), 80 nm width (right).

FIG 2. I/V curve for 80 nm width NWs.

RELATED PUBLICATIONS:
Area Selective Plasma Enhanced Atomic Layer Deposition

RESEARCH TOPIC:
Area selective deposition (ASD), plasma enhanced Atomic Layer Deposition (PEALD), Atomic Layer Etching (ALE)

AUTHORS:
R. Gassilloud, R. Vallat, C. Vallée

ABSTRACT:
Area Selective Deposition (ASD) process is currently developed to reduce the manufacturing cost of microdevices fabrication. Here, the ASD process used is based on the Atomic Layer Processing concept: ALD + ALE embedded super cycles. We propose a selective deposition process for bottom-up construction using transition metal oxides deposition by plasma enhanced atomic layer deposition (PEALD). We demonstrated for the first time the potential of this technology by the selective deposition of TiO$_2$ at nanometer scale on a metal surface TiN versus silicon based surfaces (Si, SiN and SiO$_2$) for a 3D Vertical RAM integration. This process has the advantage of being simple, easy to integrate, readily useable in fablines.

SCIENTIFIC COLLABORATIONS: CNRS-LTM

Context and Challenges
In advanced micro-devices, lithography starts to dominate the wafer cost (EUV, managing multiple mask passes and pattern placement error...). Therefore complementary techniques are needed to extend Moore’s law, such as selective deposition, a bottom-up technique, able to enhance patterning capabilities at nanometer scale and very low cost. This also reduces energy impact through limiting the numbers of process steps. Among all the various deposition processes, atomic layer deposition (ALD) is the more suitable solution to develop a selective process due to its high surface sensitivity. Hence ALD may allow to overcome lithography limits, being currently used for self-aligned double and quadruple patterning.

Main Results
At Leti in collaboration with CNRS-LTM, we propose a new pathway, based on nucleation delay of thin oxide deposition by plasma enhanced ALD (PEALD mode) coupled with an etching step, such as ALE (Atomic Layer Etching). This process has the advantage of being simple, easy to integrate, readily useable in fablines. (Fig. 1) [1].

![Fig. 1. Selective deposition principle](image1)

The different nucleation delay observed either on metal or oxide substrate induces a few nanometers thickness difference between both surfaces. After several cycles, an etching gas is added to the oxygen plasma in order to remove the deposited material on the surface with longer nucleation delay. The etching gas composition is chosen for passivating the surface after material etching, subsequently creating a new nucleation delay. Then the PEALD mode is restarted again with several cycles followed by a new plasma etching step. These PEALD + ALE supercycles can be repeated many time, depending on the thickness targeted [2].

We demonstrated the capability of this technology, by selective achievement of Titanium oxide deposited at the nanometer scale on the edge of metal Titanium nitride plans embedded in silicon oxide and nitride in a 3D vertical RAM integration (Fig. 2) [3].

![Fig. 2. Selective deposition of Titanium oxide in 3D VRAM.](image2)

Perspectives
Beyond the demonstration, we further continue to study the deposition of broad range of different oxides (TiO$_2$, Ta$_2$O$_5$, HfO$_2$) versus metal surface, and we extent the work on selective deposition of metals versus insulating surface.

RELATED PUBLICATIONS:
Full Control of Ge Epitaxy Processes and Substrate Design Open Paths to Innovative Devices

RESEARCH TOPIC:
Germanium, Smart Cut™, GeOI substrates, photonics, spintronics

AUTHORS:
J.M. Hartmann, J. Widiez, V. Reboud, (M. Jamet)

ABSTRACT:
Germanium, a column-IV semiconductor, has many uses in photonic and spintronic devices, because of (i) its compatibility with the mainstream silicon technology, (ii) its near-direct bandgap, which overcomes some of the limits inherent to standard Si photonics, (iii) its suitability for MIR sensing applications, (iv) its long spin lifetime and (v) the possibility its offers of using optical methods for spin injection/detection. To reach the targeted performances, the quality of intrinsic and doped Ge is critical. In the following, we show that a full control of Ge epitaxy and Ge transfer processes yield optimized germanium-on-insulator substrates which have many applications in innovative devices.

SCIENTIFIC COLLABORATIONS: Politecnico Di Milano, CEA-INAC, Paul Scherrer Institute - Villegen and ETH - Zürich

Context and Challenges
The Smart Cut™ technology used for the mass-production of Silicon-On-Insulator (SOI) substrates, can also be used to fabricate GeOI substrates. Germanium donor wafers can be bulk substrates, which offer a crystalline quality comparable to that of Si wafers, or epitaxial Ge on Si bulk, which enables 300 mm (and higher) wafer diameter scalability. In the following, we will focus in the second type of donors and see what are their specifics.

Main Results
Originally, Smart Cut™ GeOI substrates were targeting microelectronic applications. The Ge layers sitting on top of the buried oxide were typically less than 100nm thick. In contrast, the GeOI process flow used to fabricate photonic and spintronic-grade GeOI substrates was such that 1 µm-thick Ge layers were transferred on oxidized Si wafers. Integration started with the epitaxial growth of 2.5-µm-thick intrinsic Ge layers on 200 mm bulk Si wafers. The Low Temperature / High Temperature process used to grow at Reduced Pressure those layers yielded, in combination with short duration Thermal Cycling, really flat Ge layers with a state-of-the-art Threading Dislocations Density around 10^5/cm². High resolution X-Ray Diffraction profiles showed that these Ge layers were slightly tensely strained; such a strain state resulted from differences in thermal expansion coefficients between Ge and Si which caused in the GeOI sample, which was mechanically speaking more robust [1].

Photonic: The high crystalline quality and the slight built-in tensile strain of such GeOI substrates can be put to good use in dedicated structures that use strain redistribution. Very high amounts of tensile strain (up to 1.9% for biaxial stress and 4.9% for uniaxial stress) were induced in the central part of suspended micro-crosses and micro-bridges such as the one shown in Figure 1. A direct bandgap behavior was evidenced at cryogenic temperatures in such bridges, which can be landed onto Si if need be [2].

Spintronics: The spin diffusion length is much higher in Ge than in GaAs, opening the possibility of designing multi-terminal spintronic devices. We studied the spin-to-charge conversion at room temperature in highly n- and p-doped GeOI substrates. Electrical spin injection and detection at room temperature were achieved in highly doped n-Ge using a micrometer scale lateral spin valve. We found a spin diffusion length of the order of 2 µm. We also studied spin-to-charge conversion by inverse spin Hall effect measurements at room temperature in highly doped n-GeOI and p-GeOI. We showed that the conversion efficiency could be one order of magnitude higher with hot electrons [3].

Perspectives
Besides growth on blanket wafers, selective epitaxy can be used to deposit Ge in cavities at the end of optical waveguides for photo-detection. An original PIN photodiode architecture calling upon lateral double Silicon/Germanium/Silicon (Si/Ge/Si) heterojunctions was recently evaluated. The fabrication complexity was reduced and high-performance optical characteristics obtained at 1.55 µm [4].

FIG 1. 3D scanning electron microscopy image of a suspended Ge<100>-micro-bridge with a corner-cube cavity etched in the stretching arms. The parabolic mirrors confine light in the bridge.

RELATED PUBLICATIONS:
Technological Enhancers for CMOS-Compatible Contacts on III-V and Ge

RESEARCH TOPIC:
Contacts, metallization, Ni, Ni₃P, InP, InGaAs, Ge, Molecular Layer Doping, Sb organo compounds, Si Photonics

AUTHORS:

ABSTRACT:
For the development of silicon photonics, various technological modules are under development. For contact applications, performance enhancements have been developed for obtaining ohmic contacts with a low specific contact resistivity. In this way, we proposed the direct sputtering of Ni₃P material instead of the classical solid-state reaction of Ni thin films with InP layers. For Ge-based devices, the interest of MonoLayer Doping (MLD) without defects by using heavy atom like antimony is presented.

SCIENTIFIC COLLABORATIONS: STMicroelectronics, CPE Lyon (C2P2), ETH Zurich, IEMN Lille

Context and Challenges
In the field of optoelectronics, various devices based on III-V or Ge materials are currently developed. In order to enable their processing in Si cleanrooms, CMOS-compatible modules are under consideration. To ensure the electrical pumping of lasers or photodetectors, Si CMOS-compatible contact technologies (metallization, Integration) have been proposed [1-3] for forming low resistivity and Si CMOS-compatible contacts to n-InP and p-InGaAs.

Main Results
In a comprehensive study of the Ni/InP system [1], we have highlighted that the classical solid-state reaction between a Ni thin layer and InP material leads to the coexistence of binary and ternary phases - Ni₃P, Ni₃P, and Ni₃(InP) - the formation of which must be associated with some In partitioning and clustering at high temperatures (Fig. 1a). Although the Ni₃P phase has been reported to be responsible for the lowering of the contact resistivity in this system, it could thus hardly be isolated. Therefore, a Ni₃P target was specially designed to deposit this compound directly on InP (and InGaAs) surfaces. It appears that the Ni₃P metallization combined with an in-situ Ar preclean represents the most suitable available solution for the formation of ohmic contacts with a specific contact resistivity as low as 4.3 x 10⁻⁶Ω·cm² on n-InP [3]. This value is one order of magnitude lower than the one obtained for the classical Ni solid-state reaction for which the concomitant presence of various phases seems to be deleterious (Fig. 1b). This metallization additionally presents the advantage of being stable at least up to 350 °C. For p-InGaAs, Ni is the metallization of reference [4,5]. Nevertheless, Ni₃P metallization, originally designed for InP, provides satisfactory results and ohmic contacts.

Molecular Layer Doping (MLD) is introduced on Germanium to control n+ surface doping by heavy antimony species. A "self-capped" POSS-Sb molecule is grafted on deoxidized Ge substrate (Fig. 2).

FIG 1. (a) TEM picture of Ni / InP system after rapid thermal annealing at 450 °C and (b) specific contact resistivities of Ni-based metallizations to n-InP (Nᵥ = 3 x 10¹⁸ cm⁻³). However, Si-O-R ligands do not protect antimony against evaporation during drive in annealing as previously shown with phosphorus. After capping by an optimized low temperature deposited PEALD SiO₂, four probe STM and photoconductivity experiments coupled with Auger and SIMS evidence defect free surface doping of Germanium by antimony (Fig. 2) [6].

Perspectives
The technological enhancers developed in this study will be integrated on 200 mm CMOS-compatible hybrid III-V / Si laser. In parallel, 300 mm processes are under development. Finally, the development of contact technology for Ge(Sn) materials are under investigation.

RELATED PUBLICATIONS:
Low Temperature CVD Materials for 3D and Sensing

RESEARCH TOPIC:
Polymer and organosilicate thin films, iCVD, Low-k dielectrics, Porous materials

AUTHORS:

ABSTRACT:
Polymer and organosilicate thin films have numerous applications in microelectronics and Microsystems. In some cases, one challenge is to find adequate deposition technique allowing their conformal deposition at low temperature on complex geometries, by keeping intact chemical functionality of the precursor. In this work, we study the growth of polymer thin films using low temperature CVD techniques. By coupling thin films and polymer characterizations, we propose a model for the iCVD growth of polymers. In parallel, we use filament-assisted CVD for the insulation of TSV and for the functionalization of chemical and biochemical sensors. The proofs of concept shown here open new ways to progress on CVD techniques for emerging devices.

SCIENTIFIC COLLABORATIONS: Tokyo Electron Limited, CPE Lyon-C2P2, IRT 3D, CLINATEC

Context and Challenges
Many applications such as low-k dielectrics for interconnects or chemical sensitive layers for chemical or biochemical sensors require the conformal deposition of hybrid organic-inorganic or polymeric coatings onto a large variety of supports without use of solvents [1]. Within this work, we study filament assisted chemical vapor deposition methods for the deposition of polymer thin films at low temperature.

Main Results
Among the different CVD techniques to deposit polymer thin films, initiated-CVD (iCVD) involves the vapor phase delivery of at least two precursors (a free radical initiator and a monomer) into a vacuum chamber. We have studied the iCVD growth on Si wafers of different poly(methacrylates) that can be used as chemical layers in hydrocarbon gas sensors. For the first time, we show that the iCVD growth follows surprisingly two regimes.

This behavior can be interpreted by taking into account, as the iCVD growth progresses, that the synthesized polymer chains act as a reservoir that locally increases the concentration of monomers available for the polymerization and thus the growth rate (Fig. 1). This behavior consistently correlates with the formation of polymer chains with higher molar mass [2].

From an application point of view, filament-assisted CVD was used to grow organosilicate thin films for the insulation of high aspect ratio Through Silicon Vias (TSV). By using Methyltriethoxysilane as precursor, SiOCH with good dielectric properties were obtained after annealing the films at 400 °C (with or without UV-assist). The conformal insulation of TSV was demonstrated: conformity is higher than 70% for 10×80 μm TSV (see Fig. 2) and higher than 50% for a 10×140 μm TSV [3].

FIG 1. Growth kinetic of polymer thin film in iCVD

To avoid the use of thermal annealing, iCVD deposition of organosilicate films from vinyl-based precursors has been studied recently. We have shown that thin films deposited at low temperature (<60°C), can present very good dielectric properties (<3) without the need of a post-deposition treatment [4].

Perspectives
Current research is focusing on the insulation of high aspect ratio TSV using iCVD. Work aims also to demonstrate that this deposition technique is suitable for the development of new applications in microelectronics and micro-nanotechnologies.
Methodologies Development for Advanced Chemical Planarization Processes

RESEARCH TOPIC:
CMP, Hybrid Bonding, 3D devices, STI, Cu damascene

AUTHORS:
C. Euvrard, C. Perrot, R. Yim, V. Balan

ABSTRACT:
In order to obtain zero topography, perfect planarization should be realized at every CMP level. This asks for careful development of CMP processes with the goal to chase every remaining nanometer of topography. New methodologies for qualifying advanced processes combined with new protocols for fine characterization of whole die topography but also with full CMP consumables characterization allowed to fine tune performances of our CMP steps with direct impact on bonding quality. This is highlighted in 2 recent examples: the development of CMP for Cu hybrid bonding, the qualification of polishing processes for STI and the identification of correlation between CMP pad microstructure and polishing performances.

SCIENTIFIC COLLABORATIONS: STMicroelectronics, Ecole Centrale Lyon, ENISE, Applied Materials

Context and Challenges
Developed in 1980s in order to overcome problems with multi-layer metallization Chemical-Mechanical Planarization (CMP) become an indispensable technology for modern semiconductor fabrication. The effective topography planarization by CMP of the inter-level dielectric layers allowed the fabrication to increase the number of metal layers in modern logic devices up to 12 metal layers but also opened the door of stacking devices by direct hybrid bonding for 3D integrations. Thus, CMP is one of the enabling technologies of today’s ubiquitous electronics. Successful realization for these stacked devices asks therefore to chase every nanometer in topography deviation at die scale and at all stack level, from STI to the Cu inter-connect levels. Final improvement of global chip flatness needs, of course, use of careful choice of advanced consumables and fine tuning of the different CMP processes, but, also, adapted technique to quantify topography gain and consumable signature on topography evolution. Work done at Leti showed that interferometry is an adapted technique for die-scale topography characterization.

Main Results
Advanced process control of CMP step as well as advanced nanotopography characterization methodology are mandatory for the fabrication of a 3D Imager. Using different techniques (wafer scale interferometry, die scale, Interferometry, local high-resolution profilometry as well as by atomic force microscopy), investigation of multiscale nanotopography over the different technological step has been performed with success (see Fig.1).

Regarding STI processes, based on a simplified Striebeck curve using torque data versus sliding velocity [2], we proposed a new methodology that can be used to select CMP process that meets process control specifications required for qualification in mass production and the nanotopography specifications required for advanced technology nodes. (Fig.2).

Concerning the consumables, in-depth studies of CMP pad by means of asperities properties, contact area, volume parameters and pad surface temperature allowed to make correlations between pad microstructure and CMP performances [3]. Pad microstructure fine tuning by control of conditioning process allowed us to reduce final Cu pads dishing and erosion for the direct hybrid bonding step (see Fig.3).

Perspectives
Pad microstructure impact on post CMP topography, tribology-based protocol for process optimization as well as die-level nanotopography characterization methodology will be broaden to other CMP processes in order to control final CMP topography and obtain complete flatness needed for advanced semiconductor device nanofabrication.

REFERENCES:
3D INTEGRATION & PACKAGING

- 3D silicon interposer for power devices
- Electromigration-related failure in 3D interconnects: from advanced characterization to predictive modeling
- Fine pitch 3D interconnection with hybrid bonding
3D Silicon Interposer for Power Devices

RESEARCH TOPIC:
Through Silicon Vias (TSV), Copper pillars, Silicon interposer, Small power devices, wafer level chip scale package.

AUTHORS:
J. Charbonnier, M. Assous, A. Plihon, D. Bergogne

ABSTRACT:
Electronic power systems follow the general trend of miniaturization and functional density. 3D technologies provide an interesting response if adapted to power specifications. A new type of device has been proposed consisting of an H bridge of power transistors and a Si interposer. This study presents an H bridge of four power MOS transistors (DMOS) assembled to a passive silicon interposer which includes Through Silicon Vias (TSV). The full conception to meet power specifications of 10 A and 600 W has been reported from the interposer design strategy to the integration process flow and mounting operations at the wafer level. Moreover, electrical characterizations of various types of interconnection chains and in operating conditions thanks to the development of a dedicated test board highlight the possibilities of applications.

SCIENTIFIC COLLABORATIONS: AMS & Infineon Technologies

Context and Challenges
For future car electronics, a market with one of the highest growth rates, including electric or hybrid cars, 3D integration will become of importance, just as it has been for the handheld terminals such as smartphones. 3D technologies provide short contacts with low parasitic effects, improved energy efficiency, as well as excellent possibilities for circuit design. In this paper, MOSFET power chips capable for 10A applications are combined with Si interposer technology to study a full 3D integrated H bridge module capability for power electronic applications.

Main Results
A new complete 3D integrated H bridge device has been proposed, designed and processed through the collaboration of Infineon, AMS and Leti (Fig. 1).

FIG 1. Technology global cross section of Infineon DMOS chips after stacking on AMS/Leti Si interposer, WL molding and balling

Dedicated process modules and design rules have been developed and applied for this power application in the kilowatt range, including thick copper rerouting, wafer level molding, wafer level balling and screen printing on thin substrate (Fig. 2).

FIG 2. Wafer level molding (front side) and wafer level balling on thin substrates (wafer/module total thickness: 300µm)

The good electrical performances of the setup are reflected for example in the very low Kelvin Copper TSV on Aluminum pad contact resistance of 2.1mΩ as well as by fully functional DMOS devices. Demonstrator modules have been mounted on application PCB with passives and drivers. The board provides gate drivers and voltage probe connectivity. It was observed clean commutations with 6ns rise times for 40VDC power supply with an inductive load (Fig. 3).

FIG 3. Waveforms of the H Bridge under full load - Top trace, Blue, 3D-stack’s DC bus voltage: 27VDC - Bottom trace, Yellow, Leg output voltage: 100kHz - Bottom trace, Red, load current: 11A average

Perspectives
Prototype operating and reliability are currently under evaluation. These results already confirm the path for new types of 3D applications in the field of small power devices and has already lead to new projects.

FIG 4. Single Modules (left) and module mounted on application printed circuit board (right)

RELATED PUBLICATIONS:
[2] Low pitch screen printed SnAg bumps versus electroplating techniques for power 3D integrated flip chip device at MiNaPAD 2017, 17–18 May, Grenoble
Electromigration-Related Failure in 3D Interconnects: from Advanced Characterization to Predictive Modeling

RESEARCH TOPIC:
3D interconnects, hybrid bonding, TSV, electromigration, reliability, failure, modeling, simulation, failure analysis

AUTHORS:
S. Moreau, J. Jourdon, N. Bresson, (V. Sukharev ,S. Lhostis)

ABSTRACT:
Many demonstrations were done these past years about 3D stacking using either TSV, micro-bumps or direct bonding. Facing a need of performance increase, a higher number of interconnections is required. Thus, the electromigration (EM) phenomena remains a major reliability concern for interconnects, due to the aggressive scaling of their dimensions and consequently the ever increasing current densities. This topic is addressed from an experimental point of view and modeling one. The first one consists in the study of the effect of the final passivation annealing on the electromigration resistance of a simplified BEOL stacked involving a hybrid bonding interface correlated with deep morphological and chemical analysis. The second one consists in the development of a physics-based model to predict EM-related issues at chip level during the design phase.

SCIENTIFIC COLLABORATIONS: STMicroelectronics, Mentor Graphics

Context and Challenges
3D interconnects technology has reached a level of maturity high enough for mass production but reliability issues, like EM-related ones, must be addressed. Electromigration (EM) – an atomic flow driven by the electrons and enhanced by temperature and mechanical stresses – remains a major reliability concern for interconnects, due to the aggressive scaling of their dimensions and the ever increasing current densities. This topic is addressed from an experimental point of view and modeling one. The first one consists in the study of the effect of the final passivation annealing on the electromigration resistance of a simplified BEOL stacked involving a hybrid bonding interface correlated with deep morphological and chemical analysis. The second one consists in the development of a physics-based model to predict EM-related issues at chip level during the design phase.

Main Results
We have shown [1] that no specific failure mode is induced by hybrid bonding (HB) process whatever the bonding annealing temperature. EM tests performed on a HB stack before final passivation annealing leads to typical values of Black’s parameters (E_a=0.99 eV, n=1.36) for a Cu BEOL. However, significant influence of the final passivation annealing conditions is observed on EM lifetime as described in figure 1. In the case of an annealing with a high pressure of deuterium, the degradation is attributed to the presence of deuterium accumulated at the barriers and capping layers as evidenced by physico-chemical characterizations (Fig. 2). Simultaneously, a novel EM assessment method based on a finite-difference (FD) approach has been implemented to study EM degradation in 3D integrated circuit (IC) supply current ports [2]. A dual damascene copper through-silicon via (TSV) based EM test structure was used (Fig 3). The mean-time-to-failure (MTF) obtained with FD simulation agrees well with the MTF found using a finite-element analysis (FEA) method as well as with the measured MTF. The results demonstrate that the EM induced MTF in 3D IC structures can be correctly predicted with FD simulations (Fig. 4), by representing them as combinations of 1D interconnect branches with suitable boundary conditions (BC) for the branch junctions.

Perspectives
Copper diffusion at the bonding level and the impact of pitch (down to ~1 µm) on the HB interconnects reliability are the current topics of interest for the experimental part. Regarding the modeling approach, validation with other 3D interconnects is required before trying to have a predictive modeling at a full chip level.

RELATED PUBLICATIONS:
Fine Pitch 3D Interconnection with Hybrid Bonding

RESEARCH TOPIC:
3D integration, water-to-wafer direct bonding

AUTHORS:
A. Jouve, L. Arnaud

ABSTRACT:
This document presents the work recently achieved at Leti in the field of direct hybrid bonding technology for the fabrication of vertical interconnects thanks to wafer-to-wafer bonding. Process robustness is analyzed through morphological and electrical results. Demonstration of 1µm pitch bonding feasibility is done. Furthermore, the electrical characterizations are discussed versus hybrid bonding pad dimensions and pitches. Finally, electromigration study is carried out on different test vehicles with hybrid bonding interconnect dimensions below 5 µm.

SCIENTIFIC COLLABORATIONS: IRT Nanoelec, ENIAC (POLIS), DEMO3S consortium

Context and Challenges
The continuous race to performance and density has led to the introduction of 3D integration in CMOS ICs. Among the different schemes to obtain 3D devices, the last decade has shown that wafer to wafer bonding was a key enabler for 3D high density integration. In this case, the wafers are processed separately and bonded together with direct hybrid bonding at room temperature. This technique is foreseen to address 10^2 to 10^6 interconnections/mm² but nobody knows today what could be the smallest dimension reached with such process. The challenges to ensure the success of hybrid bonding are the following: the flatness of the wafer surface should be low enough to ensure a perfect bonding interface. Also the bonding tools should present alignment performance matching with reduced interconnection dimensions. Finally, the electrical performance of the connection should be highly reliable in order to match the product specifications.

Main Results
Leti started the development of hybrid bonding in the early 2000 years demonstrating the 1st electrical test vehicle done with 200mm wafers. More recently, the work focused on 300mm process development. This work has been achieved in collaboration with STMicroelectronics and EVG partners. The hybrid bonding level is composed of dual damascene interconnects. The connecting pad dimension range from 1 µm to 10 µm pitch and a large variety of wafers presenting only 1 level of damascene to complete 3D test vehicles representative of imager technology are used for stacking. After CMP process optimization, it is confirmed with AFM and Infra-Red Interferometry that roughness and topology are in specification for wafer-to-wafer direct bonding. No interfacial bonding defects are observed with Scanning Acoustic Microscopy technic (SAM) for bonding levels with 7-9 µm pitch or for bonding levels with 1.5 µm pitch.

At pad scale, bonding performance is assessed with cross sections of Cu-Cu interface (see Fig. 1). Both 4.4 µm Cu pad and 0.5 µm Cu pad show perfect interfaces. No voids and excellent copper grain growth after anneal have been observed [1]. To ensure perfect alignment between top and bottom wafers, these bondings are achieved with EVG EVG®40NT equipment which has demonstrated +/-200nm alignment accuracy.

Finally, electrical performances of the bonded wafers is confirmed with a 100% connection yield observed on 300mm bonding surface [2]. Measured contact pad resistance and leakage current of various length daisy chains are very low and consistent with theoretical measurements. Leti also develops innovative structures which enables electrical measurement of wafer-to-wafer misalignment [3]. Reliability analysis shows that direct Cu-Cu bonding interface is very robust against electromigration (EM) failure and humidity storage. EM failures always occur at the weakest interface for Cu diffusion, with respect to electron flow (i.e BEOL level of stacked CMOS wafers).

Perspectives
Work is in progress at Leti with the fabrication of bonding interconnections with pitch smaller than 1µm and the application of the process to functional wafers. Moreover, work is scheduled to address 3D interconnections with direct wafer bonding including 3 substrates.

RELATED PUBLICATIONS:
• In-situ electrical biasing and thermal annealing of resistive memory devices in a transmission electron microscope

• Organic depth profiling using time-of-flight secondary ion mass spectrometry

• Hard X-ray photoemission with synchrotron radiation for buried interfaces in device technology

• Toward a full 3D structural and chemical characterization of materials by correlating transmission electron microscopy with atom probe tomography

• Raman-strain relations in highly strained Ge

• Fast chemical depth profiling in a cleanroom environment

• Synchrotron tomography as a routine tool for 3D integration failure analysis
In-situ Electrical Biasing and Thermal Annealing of Resistive Memory Devices in a Transmission Electron Microscope.

RESEARCH TOPIC:
In-situ electron microscopy, Resistive memory, Phase Change Memories

AUTHORS:
D. Cooper and R. Berthier

ABSTRACT:
There is a need to be able to observe nanometer and atomic scale changes in nanoscaled electronic devices in working conditions. This allows the study of the exact mechanisms behind the properties of the devices and as such improvements can be made from these direct observations. Here methods have been developed such that specimens can be electrically biased or annealed in a transmission electron microscope and examined with atomic scale resolution. Transmission electron microscopy is an attractive characterisation technique as many different approaches can be used to measure the structure, composition, bonding and fields in the same specimen during the same experiment.

SCIENTIFIC COLLABORATIONS: Forschungzentrum Julich, Laboratoire des technologies de la Microélectronique (LTM)

Context and Challenges
The last 10 years has seen a revolution in transmission electron microscopy (TEM) due to both the development of aberration correctors for improving the spatial resolution and the improvement of their stability. In this time experimental methods have also significantly improved in order to profit from these powerful tools. TEM can be used to acquire images with atomic resolution and we can simultaneously measure the composition, bonding and fields. Now we would like to be able to see how nanoscaled devices work and to measure how their properties are linked to the materials and structure, in-situ in an electron microscope.

Main Results
In the frame of the ERC starting project « Holoview » we have developed different methods of performing in-situ experiments including annealing and electrical polarisation. Specimen preparation is key to success and we have developed protocols for electrically connecting nano-scaled structures that are either analysed on patterned chips or using a piezo electrical contact to probe different regions of the specimens.

A range of different specimens have been examined, including the study of resistive memories, such as TaOx, HfOx and phase change memories. Here, we present a study on SrTiO3 memory devices that has been supplied with FZG Julich. By controlling the experiment we have been able to measure the movement of oxygen vacancies under the top electrode. In this work we were able to form and then reversibly switch a specimen from a high resistive state (insulator) to a low resistive state (conducting) whilst simultaneously mapping the concentration of Ti-O bonds using electron energy loss spectroscopy (EELS). Different specimens were observed and we were able to show that area switching is more likely in perfect specimens whereas filaments were formed in regions containing many grain boundaries. The figure (a) shows a high resolution image of an examined specimen and (b) electrical cycling in the eightwise direction suggesting area switching. The maps of the oxygen vacancies confirm this with (c) a homogenous distribution when the device is in an insulating state and (d) a concentration of oxygen vacancies under the top electrode when the device is conducting. Until these experiments were performed there were competing explanations about where the oxygen vacancies accumulated during cycling and this knowledge has led to the use of a blocking layer under the Pt top contact to prevent the loss of oxygen in the devices and increase their endurance.

Perspectives
We intend to use these methods to study a range of different materials that change their properties after electrical or thermal stimulus. These could include different resistive memories, piezoelectrics, ferroelectrics and magnetic specimens. In addition we will be able to study III-V materials and different photovoltaic materials to measure how the local electrical properties are linked to defects, dopants and interface states.

FIG 1. In situ study of STO performed using EELS.

RELATED PUBLICATIONS:

RESEARCH TOPIC:
Elemental and molecular depth profiling of organic films

AUTHORS:

ABSTRACT:
Time-of-flight secondary ion mass spectrometry (ToF-SIMS) is a high performance tool for molecular depth profiling of polymer films, in particular when they are structured in microphases. However, a major issue is the degradation of polymer materials under ion irradiation in reactions such as cross-linking, chain breaking, or reorganization processes of polymers which have been demonstrated for materials such as polystyrene (PS) and poly(methyl methacrylate) (PMMA). Recent work at the Leti has shown that Argon cluster sputtering allows to avoid such effects and obtain TOF-SIMS profiles of technologically relevant systems such as block copolymer films for lithography, organic light emitting diodes (OLEDs) and iCVD grown thin films.

SCIENTIFIC COLLABORATIONS: University of Lyon, University of Catania, University of Bordeaux

Context and Challenges
TOF-SIMS depth profiling has been shown to be pertinent to address some of the major challenges in the analysis of thin film organic multilayers. For example the composition (including elemental and molecular doping, molecular degradation and organization) can be followed as a function of film thickness for applications such as organic electronics, organic photovoltaics and photosensitive block copolymers such as those used for advanced lithography. Several ion sources are now available such as Ar clusters, Cs+ and Cs. The challenge is to successfully depth profile the layers in question with minimum damage so that any change in the mass spectra can be attributed to the material itself and not ion to beam damage.

Main Results
A study was carried out on PS-b-PMMA block copolymer films used as model systems for the assessment of three different ion beams. These are Arn+, Cs60++ and Cs+ where n is between 500 and 5000 argon atoms per cluster.

FIG 1: Diagram of the model PS-b-PMMA layer used and an example depth profile for PMMA.

The use of argon cluster sputtering was shown to give the best profiles and allow the organization of block copolymer films to be evaluated. These protocols were also used to depth profile one-step solution processed OLED layers for which TOF-SIMS depth profiling was also used to investigate the 2-step growth process of iCVD grown poly(3-ethyl-4-hexyl) (PEIE) and 1,3,5-tris(N-phenylbenzimidazol6-yl) benzene (TPBi).

FIG 2. TOF-SIMS depth profile of a PEIE:TPBi blend deposited in one step on an ITO/ZnO substrate

TOF-SIMS depth profiling was also used to investigate the 2-step growth process of iCVD grown poly(neo-pentyl methacrylate) (nPMA) thin films on silicon substrates. The spectra confirm that although the composition is constant with depth, the molecular weight varies with thickness.

Perspectives
Correlative approaches combining TOF-SIMS with XPS and AFM are being developed to look at hybrid structures (e.g. inorganic/organic interface in OLEDs) and the use of tandem MS/MS spectrometers for TOF-SIMS is under evaluation.

RELATED PUBLICATIONS:
Hard X-Ray Photoemission with Synchrotron Radiation for Buried Interfaces in Device Technology

RESEARCH TOPIC:
Chemical analysis and non-destructive elemental depth profiling at buried interfaces, in-situ biasing of devices

AUTHORS:

ABSTRACT:
Photoemission using hard X-rays (HAXPES) in the 3-12 keV range available at synchrotron sources enables to look deeper below the surface of materials and gives access to critical interfaces in devices. Conventional methods such as core-level spectroscopy provide information regarding local chemistry. However, novel methodologies such as inelastic background analysis or in-situ biasing of device structures are needed in order to get the full benefits of HAXPES in device technology. We highlight here the implementation of these methodologies to analyze multi-layer systems used in a wide range of devices: resistive memories (CBRAM), high electron-mobility power transistors (HEMT) and multi-MIM (metal-insulator-metal) capacitors.

SCIENTIFIC COLLABORATIONS: CEA-IRAMIS/SPEC, NIMS (Japan), Synchrotron SOLEIL, University of Southern Denmark, INL (Lyon).

Context and Challenges
As recalled by Kroemer in his Nobel Lecture in 2000, "the interface is the device". This statement highlights the pressing needs to implement innovative analytical methods for characterizing in a reliable way critical interfaces in device technology. Hard X-ray photoelectron spectroscopy (HAXPES) has shown to increase the information depth of laboratory XPS by a factor of 3, getting access to the chemistry of weakly buried interfaces (20 nm). Reliability is increased because invasive deprocessing is no longer required and subtle changes at buried interfaces can be revealed. Other methods addressed here enable such analyses either while the device is being biased in-situ (operando conditions), or in the case of much deeper interfaces up to 70 nm (inelastic background analysis).

Main Results
A first application of HAXPES to CBRAM structures is shown in Fig. 1. The increased probing depth provides sensitivity to chemical changes at the ZrTe/Al2O3 interface upon ex-situ forming as a result of oxygen upward diffusion from Al2O3. [1]

FIG 1. Interface chemical analysis in CBRAM structure by HAXPES.

Changes at critical interfaces in devices are better probed by so-called operando measurements, using, e.g., in situ bias application during analysis. Fig. 2 illustrates a result obtained on lead zirconate-based MIM capacitors. When compensating for the applied bias on the spectra (inset), a residual energy shift due to the PZT/Ru/Pt interface polarization is evidenced [2].

FIG 2. Operando HAXPES of MIM structures

The two last examples show that information depth is still limited to 15-25 nm in core-level HAXPES. To this end, we have developed innovative approaches based on the quantitative analysis of the inelastic background, providing depth sensitivities up to 70 nm [3].

Perspectives
Recently, hard X-ray sources suitable for performing HAXPES with laboratory instruments have become available. The measurements shown here should be feasible soon using accessible instruments for better supporting device technology.

RELATED PUBLICATIONS:
Toward a Full Structural and Chemical Characterization of Materials by Correlating Transmission Electron Microscopy with Atom Probe Tomography

RESEARCH TOPIC:
Atom probe tomography, transmission electron microscopy, II-VI and nanoporous materials

AUTHORS:
A. Grenier, I. Mouton, T. Printemps, (B. Bonef, C. Bougerol, D. Blavette, G. Mula)

ABSTRACT:
The correlation of transmission electron microscopy to atom probe tomography is a powerful method to characterize structure, morphology and chemistry from layered stacks to complex devices. Recent experimental and data treatment developments have opened the way to the chemical analysis of nanoporous materials.

SCIENTIFIC COLLABORATIONS: INAC, Institut Néel, Univ Cagliari, GPM (Rouen)

Context and Challenges
The field of semiconductor science has grown exponentially for the past decades. Semiconductors can now be found in a multitude of devices such as transistors, light emitting diodes, laser diodes, solar cells... The efficiency and physical properties of these devices often rely on the structure of the active regions at the nanometer scale. Consequently, the use of nanometer scale characterization techniques is essential to push forward the conception and the development of devices for the future.

Atom probe tomography (APT) is one of the major techniques that provides composition information with nanometre resolution in 3D. It has now been extensively applied for the investigation of interfaces, defects, or composition fluctuations in semiconductors. However, atomic resolution often cannot be achieved on such materials and, more importantly, calibration of the APT evaporation parameters are required to get reliable reconstructions and quantifications. Moreover, the reconstructed volumes from APT analysis can be optimized using information on the sample structure and geometry which can be obtained from other techniques. Nowadays, the correlative use of APT with transmission electron microscopy in 2D and 3D is a way to overcome both these limitations. Such an approach has been successfully applied for the structural characterization of nanoporous Si, III-V and II-VI devices.

Main Results
The correlative use of APT and scanning transmission electron microscopy (2D-STEM) allowed to characterize the structure of ZnTe/CdSe superlattices at the nanometre scale (Fig.1). Both techniques reveal the segregation of zinc along [111] stacking faults in CdSe layers, which is interpreted as a manifestation of the Suzuki effect. Quantitative measurements reveal a zinc enrichment around 9 at. % correlated with a depletion of cadmium in the stacking faults [1].

Coupling electron tomography (3D-STEM) with APT (Fig.2), allowed to obtain both structural information and reliable chemical quantification of complex materials. Recent developments have allowed to investigate the morphology and chemical structure of nanoporous Si filled with nickel [2].

Perspectives
The correlation between 3D-transmission electron microscopy and atom probe tomography is still in progress and will be applied to FEOL devices.

RELATED PUBLICATIONS:


Raman-Strain Relations in Highly Strained Ge

RESEARCH TOPIC:
Nano-characterization, 2D materials, Photonic

AUTHORS:
D. Rouchon, V. Reboud, (V. Calvo, A. Gassenq)

ABSTRACT:
The application of high values of strain to Ge considerably improves its light emission properties and can even turn it into a direct band gap semiconductor. Raman spectroscopy is routinely used for strain measurements. Typical Raman-strain relationships that are used for Ge were defined up to 1% strain using phonon deformation potential theory. In this work, we have studied this relationship at higher strain levels for different stress configurations. Since differences were shown between the usual phonon deformation potential theory and ab-initio calculations, we highlight the need for experimental calibrations.

Context and Challenges
Strain engineering has become a widely used strategy to alter the properties and the performance of semiconductor materials. The prospect of accessing entirely new regimes of material behavior using extreme applied strain creates exciting new scientific and engineering opportunities. In order to characterize applied strain at the microscale, a widely used method is Raman spectroscopy in conjunction with an empirical model. However, such empirical models were initially defined only for the low strain regime (<1%) and no calibration has been made for the extreme strain values. In this work, we have simulated and measured the Raman-strain relationship for several stress configurations: the uniaxial stress along <110>, <100> and the (001) biaxial stress.

Main Results
To measure the Raman-strain relationships for different stress configurations, we have used micro-crosses and micro-bridges fabricated from optical Ge-On-Insulator (GeOI) wafers. Figure 1 presents the measured strain as a function of the Raman spectral shift for the three measured stress configurations. Experimental data are plotted as dots, the usual linear models are plotted as straight lines, ab initio calculations are plotted as dashed lines, and empirical data fitting as dotted lines. For the biaxial stress, we found a good agreement between the experimental, semi-empirical, and ab initio Raman shift-strain relations. For the uniaxial stress along <100>, a deviation of the linear coefficient is shown. For the uniaxial stress along <110>, we also report a non-linearity of the Raman-strain relationships for both measured LO and TO2 phonon modes. In order to provide the new Raman-strain relationships, we have fitted our experimental data with polynomial equations (2). The resulting experimental coefficients \( a \) and \( b \) in equation 2 are compared in Table I to the inverse of the linear coefficients \( k \) resulting from equation 1.

\[
\Delta \omega = k \times \varepsilon (1) \quad \varepsilon = a \times \Delta \omega + b \times \Delta \omega^2 (2)
\]

Figure 2 presents the measured strain as a function of the Raman spectral shift for the three measured stress configurations. Experimental data are plotted as dots, the usual linear models are plotted as straight lines, ab initio calculations are plotted as dashed lines, and empirical data fitting as dotted lines. For the biaxial stress, we found a good agreement between the experimental, semi-empirical, and ab initio Raman shift-strain relations. For the uniaxial stress along <100>, a deviation of the linear coefficient is shown. For the uniaxial stress along <110>, we also report a non-linearity of the Raman-strain relationships for both measured LO and TO2 phonon modes. In order to provide the new Raman-strain relationships, we have fitted our experimental data with polynomial equations (2). The resulting experimental coefficients \( a \) and \( b \) in equation 2 are compared in Table I to the inverse of the linear coefficients \( k \) resulting from equation 1. \( a \) and \( b \) coefficients have 5 and 10 % standard errors, respectively coming from the fit deviation. Given those uncertainties, we found a good agreement between \( 1/k \) and \( a \), because the linear coefficient \( 1/k \) has been defined only for low levels of strain (e.g. where the \( b \) coefficient does not significantly impact the Raman-strain relationship).

Perspectives
This strain engineering methodology can be extended to GeSn alloys. This is the subject of intense research activities as these group IV semiconductors possess a direct bandgap for high Sn contents.

RELATED PUBLICATIONS:
Fast Chemical Depth Profiling in a Cleanroom Environment

RESEARCH TOPIC:
Metrology, elemental depth profiling, mass spectrometry, material analysis

AUTHORS:
Y. Mazel, E. Nolot, J.-P. Barnes

ABSTRACT:
Time-of-flight secondary ion mass spectrometry (TOF-SIMS) is routinely used for depth profiling of microelectronic materials but interpretation of results can sometimes be hampered by artifacts such as matrix effects. Plasma profiling time-of-flight mass spectrometry (PP-TOFMS) provides direct measurement of the elemental composition of materials as a function of depth, with nanometer resolution and higher sputter rates than for TOF-SIMS. The optimization of both Horiba PP-TOFMS instrument and measurement protocols allows fast process feedback based on semi-quantitative chemical depth-profiles, accessible to a wide userbase by virtue of easily interpretable results. The efficiency of these inline metrology strategies has been demonstrated on various materials such as indium-free TCO for lighting and PV, or GaN-based stacks for power electronics, RF and lighting.

SCIENTIFIC COLLABORATIONS: Horiba France S.A.S.

Context and Challenges
The development and process control of innovative structures studied in both More Moore and More than Moore approaches require methods to depth profile the chemical composition of complex multi-material stacks. Currently, secondary ion mass spectrometry (SIMS) is often used for this purpose, but instruments are costly, require a highly skilled operator (both for running the instrument and analyzing the results), and are also in high demand. To allow rapid process feedback, there is a need for a rapid chemical depth profiling technique that can be used by a wide userbase with easily interpretable results. Plasma profiling time-of-flight mass spectrometry (PP-TOFMS) is an innovative chemical depth profiling technique that can fulfill these criteria. First, PP-TOFMS sputtering and ionization mechanisms mostly form monoatomic ions, leading to a much simpler mass spectrum when compared to TOF-SIMS (Fig.1). In addition, decoupling between the sputtering and the ionization processes makes PP-TOFMS much less matrix dependent than TOF-SIMS. Lastly, measurement time (including sample introduction) is ~5 min. Consequently, fast and reliable chemical depth-profiling of complex materials using PP-TOFMS is easily accessible by non-experts [1].

Main Results
The performances of PP-TOFMS to reveal depth-dependent distributions in Indium-free transparent conductive oxides such as ZnO:Al and ZnO:Ga were established and compared to TOF-SIMS and grazing incidence X-ray fluorescence [2].

Plasma profiling time-of-flight mass spectrometry was also extensively used to support the development of Mg-implantation and innovative InAIN and InAlGaN barrier layers in GaN-based stacks. The lattice mismatch between InAIN and GaN can be drastically reduced by fine-tuning the In/Al ratio and the depth-dependent profile in the barrier layer. PP-TOFMS allowed fast characterization of these layers, with SIMS-like ability to reveal depth-dependent chemical distribution, even close to the surface (Fig.2). In addition, semi-quantitative information based on intensity ratios were aligned within 10 rel. % to composition deduced from calibrated wavelength-dispersive XRF. PP-TOFMS is now routinely used in self-service operation for the development of these materials [3].

Perspectives
Future work will focus on the quantitative analysis in complex materials (including determination of relative sensitivity factors), and on the improvement of PP-TOFMS capability for light elements (C, N, O…) using Ar/He dilution instead of pure Ar plasma.

FIG 1. TOF-SIMS and PP-TOFMS mass spectra of SiGe layer grown by epitaxy

FIG 2. Depth-dependent chemical distribution in 30 nm (left) and 200 nm (right) thick InAlGaN barrier layer deposited on GaN

RELATED PUBLICATIONS:
Synchrotron Tomography as a Routine Tool for 3D Integration Failure Analysis

**RESEARCH TOPIC:**
X-ray tomography for 3D integration

**AUTHORS:**

**ABSTRACT:**
Synchrotron tomography is a characterization technique that is perfectly suited to the analysis of defects in 3D integrated devices. It is also a rather heavy technique to implement. In this work we have developed and tested new strategies for sample preparation, measurement methodology and post-processing that make this technique compatible with a statistical analysis of defects in devices, making synchrotron tomography a routine tool for 3D integration failure analysis.

**SCIENTIFIC COLLABORATIONS:** ESRF, FEI, STMicroelectronics

Context and Challenges
3D integration is increasingly important in the microelectronics industry. In order to image the three-dimensional objects created for wafer or die bonding processes, new tools must be developed. Tomography is a technique based on the successive acquisition of sample projections, at different angles. An algorithm then allows for the reconstruction of a 3D volume representing the original sample. Synchrotron-based X-ray tomography performed on recent beamlines can offer resolutions down to several tens of nanometers. However, as the experimental setup is still quite heavy, strategies must be found to increase the throughput of samples, in order for the technique to require little human intervention and to provide statistical information.

Main Results
In this study, we present three strategies that allow for such features. First, adapting the sample preparation scheme allows to make the most of the sample preparation and drastically decreases the human intervention needed during the data acquisition. The sample installation is made individually for each sample. The idea is to make the most out of the sample preparation, by placing several samples on one given support.

Secondly, reducing the number of projections by a factor 4 is made possible by the use of iterative reconstruction algorithms with little loss of information. Finally, the post-processing of the data is now fully automated and directly renders the reconstructed volume. The algorithm performs the whole post-processing, including the radiographs alignment for each angle, the phase retrieval, the projections alignment and the calculation of the actual rotation axis.

**FIG 1.** Two different sample organizations for x-ray tomography. a) Classic lift-out sample, on an aluminum pin. b) 12 samples on a single aluminum support. The inset shows a composite radio of all the samples together.

**FIG 2.** Reconstructions of the same copper pillar slice using two different reconstruction algorithms. a) FBP using 2000 projections. b) CGLS using 500 projections (and 23 iterations)

The workflow proposed and illustrated here allows for statistical studies, and makes synchrotron tomography a possible routine tool for failure analysis and 3D integration characterization.

Perspectives
Using a dedicated sample preparation, automatic scanning and post-processing has been shown to be possible to obtain "ready to process" reconstructed volumes at the end of the beamtime. The next ESRF up-grade will also open new opportunities by improving the horizontal emittance, thereby improving the brilliance. The brilliance of the X-ray beam is indeed a critical property for such research, and pushing 3rd generation synchrotron performances to the limit will make tomography even faster and open new possibilities for materials science research.

**RELATED PUBLICATIONS:**

09

PHD DEGREES AWARDED
PELLOUX-PRAYER Johan  
Université Grenoble Alpes (France)

Study of strain and electrical properties in Si nanowire transistors

This document is the result of my thesis work at the CEA-Leti Grenoble. It covers the evolution of the piezoresistive effect and the electrical transport properties of field effect transistor device against several variable such as geometry, temperature, internal stress... The focus of this work is to understand the effect brought by extreme reducing of channel and gate dimensions in MOSFET transistors. A special attention is given on electrical data modeling. Different algorithms are used to extract key parameters of devices and their viability against the device dimensions considered is discussed. A new piezoresistive coefficients model is drawn from a known mobility model, it allows to draw a reliable tendency of piezoresistive variation against the cross section (channel width and thickness) of a given multigate device. An effect not accountable by standard theory for small cross section was shown by the measurements, and some hypothesis are made and discussed to explain whose results. Integration process are elaborated to realize In0.53Ga0.47As trigate transistors on silicon: the molecular bonding of an InGaAs layer grown on a InP substrate, and the direct epitaxy of InGaAs on a silicon substrate. The fabrication steps for InGaAs transistors were developed, taking into account the clean room contamination restriction. InGaAs surface treatment and high-permittivity dielectric deposition by ALD are studied in order to reduce the density of interface states (Dit) and to optimize the EOT. XPS analysis and C(V) measurement are performed at the scale of a 300mm Silicon substrate.

BORREL Julien  
Université Grenoble Alpes (France)

Innovative contact technology for CMOS FDSOI 10 nm and below

As we reach the ultimately scaled digital logic CMOS nodes, the scaling is more and more reflected on the contact length decrease rather than on that of the gate length in order to preserve well-behaved MOSFET characteristics. As a consequence, meeting the performance requirements for the upcoming devices generations implies to drastically decrease the contact resistivity value. However, due to Fermi level pinning, most of the metals used in the microelectronics today feature an effective metal work function almost independent from their reference value when contacted to silicon. This phenomenon hinders the optimization of the Schottky barrier height at the interface and thus of the contact resistivity. An innovative approach consists in inserting a dielectric layer between the metal and the semiconductor of the contacts thus forming Metal/Insulator/Semiconductor (MIS) junctions. Recently, studies of sub-nanometric TiOx insertions have shown promising results on n-type Si. Nevertheless, most of the studies of the state-of-the-art were performed in a non-industrial environment and were more focused on achieving a proof of concept rather than implementing MIS contacts in existing manufactured products with all their constraints. The work of this thesis consists in i) analyzing the optimal co-integration scheme of MIS contacts on n- and p-type semiconductors presenting relatively high doping concentration; ii) Evaluating the impact of such contacts on advanced MOSFETs nodes; iii) Implementing MIS contacts in a semi-industrial environment using the materials commonly found in advanced microelectronics; iv) Gauging the effective electrical properties of MIS contacts.
The replacement of the silicon channel by III-V materials is investigated to increase the electron mobility in the channel and reduce the power consumption. In order to decrease the cost and to take advantage of the microelectronic silicon platform, III-V transistors must be built on Silicon substrates. However, the lattice parameter mismatch between Silicon and the III-V layers leads to a high defects density in the channel and reduces the carrier mobility. This thesis aims to realize III-V transistors on silicon substrate in the CEA-Leti microelectronic clean room. In the frame of this PhD work, two integration process are elaborated to realize In0.53Ga0.47As trigate transistors on silicon: the molecular bonding of an InGaAs layer grown on a InP substrate, and the direct epitaxy of InGaAs on a silicon substrate. The fabrication steps for InGaAs transistors were developed, taking into account the clean room contamination restriction. InGaAs surface treatment and high-permittivity dielectric deposition by ALD are studied in order to reduce the density of interface states (Dit) and to optimize the EOT. XPS analysis and C(V) measurement are performed at the scale of a 300mm Silicon substrate.

The 3D sequential integration is a smart alternative to planar device scaling. In this integration, the stacked transistors are processed sequentially, thus implying the reduction of the top thermal budget processes in order to preserve the bottom levels. For the FDSOI technology, the maximum thermal budget is set at 500 °C, 2 h. Despite the work done to reduce the thermal budget of the FDSOI processes, it is difficult to comply with this limit, as for example for the epitaxial raised source and drain which would need a thermal budget limit relaxation. In these conditions, the dielectric lifetime is estimated at 1016 years. Despite its reduction due to thermal budget at 600 °C, 2 h (107 years), the tungsten lifetime estimation remains higher than the one obtained with copper lines without thermal budget.

The replacement of the silicon channel by III-V materials is investigated to increase the electron mobility in the channel and reduce the power consumption. In order to decrease the cost and to take advantage of the microelectronic silicon platform, III-V transistors must be built on Silicon substrates. However, the lattice parameter mismatch between Silicon and the III-V layers leads to a high defects density in the channel and reduces the carrier mobility. This thesis aims to realize III-V transistors on silicon substrate in the CEA-Leti microelectronic clean room. In the frame of this PhD work, two integration process are elaborated to realize In0.53Ga0.47As trigate transistors on silicon: the molecular bonding of an InGaAs layer grown on a InP substrate, and the direct epitaxy of InGaAs on a silicon substrate. The fabrication steps for InGaAs transistors were developed, taking into account the clean room contamination restriction. InGaAs surface treatment and high-permittivity dielectric deposition by ALD are studied in order to reduce the density of interface states (Dit) and to optimize the EOT. XPS analysis and C(V) measurement are performed at the scale of a 300mm Silicon substrate.

The future of the transistors currently used in Microelectronics is still uncertain: shrinking these devices while increasing their performances always remains a challenge. In this thesis, stacked nanowire transistors are studied, fabricated and optimized. This architecture embeds gate all around which is the ultimate solution for concentrating always more current within a smaller device. Simulations have shown that silicon nanosheets provide an optimal utilization of the space with providing increased performances over the other technologies. Crucial process steps have also been identified. Subsequently, two process flows have been suggested for the fabrication of SNWFETs. The first approach consists in minimizing the number of variations from processes already in mass production. The second alternative has potentially better performances but its development is more challenging. Finally, the fabricated transistors have shown improved performances over state-of-the-art especially due to mechanical stress induced for improving electric transport.
The junction fabrication involve numerous technological challenges as the devices shrink. To alleviate issues brought by the aggressive device scaling, Fully Depleted SOI substrates as well as strained silicon-germanium (SiGe) have been introduced in advanced nodes. They however require a highly-activated abrupt junction achievable with solid phase epitaxial regrowth (SPER) and a low thermal budget (500°C-5h). In this manuscript, the SPER of silicon, germanium and SiGe alloys is investigated using Kinetic Monte Carlo (KMC) and Molecular Dynamics (MD) methods. […] The interface roughness could be the link between the strain relaxation and the temperature, as MD simulations exhibit an influence of the anneal temperature on the interface roughness and strain relaxing defects are associated to a rough interface. In summary, the SPER and its several dependencies are investigated in this manuscript with atomistic approaches. The drawn conclusions increase the current understanding of SPER, allowing a better optimization of junction fabrication.

This document is the result of my thesis work at the CEA-Leti Grenoble. It covers the evolution of the piezoresistive effect and the electrical transport properties of field effect transistor device against several variable such as geometry, temperature, internal stress....The focus of this work is to understand the effect brought by extreme reducing of channel and gate dimensions in MOSFET transistors. A special attention is given on electrical data modeling. Different algorithms are used to extract key parameters of devices and their viability against the device dimensions considered is discussed. A new piezoresistive coefficients model is drawn from a known mobility model, it allows to draw a reliable tendency of piezoresistive variation against the cross section (channel width and thickness) of a given multigate device. An effect not accountable by standard theory for small cross section was shown by the measurements, and some hypothesis are made and discussed to explain whose results.

3D Monolithic Integration: Performance, Power and Area Evaluation for 14nm and beyond

3DVLSI integration, also known as monolithic or sequential integration is presented and evaluated in this thesis as a potential contender to continue the scaling for CMOS logic circuits. The main advantage of this technology compared to the already existing 3D parallel integration is its high alignment among tiers, enabling small size and pitch with the inter-tier contacts (3DCO). Another great 3DVLSI feature is its improved capability to place and route circuits, compared to the planar approach: the interconnections can be shorter as the design has an additional degree of freedom in the Z direction. For instance, long wires in planar circuits can be cut thanks to 3DCO contacts, lowering the interconnection parasitic elements and speeding up the circuit as well as reducing the power. In this framework, the thesis has been divided into two parts: the first part is dedicated to the evaluation of Performance, Power and Area (PPA) of 3D circuits and gives design guidelines. The second part treats the variability in 3D circuits by using a 3D unified statistical model and propose an approach for the multi-tier variability.
Low thermal budget CMOS processing for 3D Sequential Integration

As the scaling of transistors following Moore’s law seems to slow down due to physical, technological and economical barriers, it becomes mandatory to find alternatives to cope with the increasing demand in electronics: computing and telecommunication, smart and interconnected objects, medical and biological fields... To that end, the use of the third dimension, in opposition to the planar processing of electronic devices, appears to be a promising option. Indeed, 3D integration allows incorporating more devices per area by stacking them at a lower technological and economical cost than scaling. More specifically, 3D sequential or CoolCube™ at CEA-Leti allows benefiting fully from the third dimension by processing successively one on top of each other each level of a die, allowing an optimal alignment of single transistors at each layer. However, several technological barriers specific to 3D Sequential Integration need then to be alleviated.

In this work, we will study the reduction of thermal budget for the transistors fabrication, which is required to not damage bottom levels during the processing of top devices. Modules impacted during the fabrication of a transistor.
Spiking neural networks based on resistive memory technologies for neural data analysis

The central nervous system of humankind is an astonishing information processing system in terms of its capabilities, versatility, adaptability and low energy consumption. Its complex structure consists of billions of neurons interconnected by trillions of synapses forming specialized clusters. Recently, mimicking those paradigms has attracted a strongly growing interest, triggered by the need for advanced computing approaches to tackle challenges related to the generation of massive amounts of complex data in the Internet of Things (IoT) era. This has led to a new research field, known as cognitive computing or neuromorphic engineering, which relies on the so-called non-von-Neumann architectures (brain-inspired) in contrary to von-Neumann architectures (conventional computers). In this thesis, we explore the use of resistive memory technologies such as oxide vacancy based random access memory (OxRAM) and conductive bridge RAM (RAM) for the design of artificial synapses that are a basic building block for neuromorphic networks. Moreover, we develop an artificial spiking neural network (SNN) based on OxRAM synapses dedicated to the analysis of spiking data recorded from the human brain with the goal of using the output of the SNN in a brain-computer interface (BCI) for the treatment of neurological disorders. The impact of reliability issues characteristic to OxRAM on the system performance is studied in detail and potential ways to mitigate penalties related to single device uncertainties are demonstrated. Besides the already well-known spike-timing dependent plasticity (STDP) implementation with OxRAM and CBRAM which constitutes a form of long term plasticity (LTP), OxRAM devices were also used to mimic short term plasticity (STP). The fundamentally different functionalities of LTP and STP are put in evidence.

Investigation of degradation mechanisms and related performance concerns in 40nm NOR Flash memories

Flash technology still represents the preferred storage memory in many portable consumers and computer applications. However, the conventional Flash cell is now facing technological barriers and needs to be optimized pushing its working condition to the intrinsic physical limit. Such an optimization has to be done mainly focusing on reliability concerns, i.e. data retention and endurance, since representing the main limiting factors of technology down-scaling. For this reason, several works dealt with data retention concerns analyzing, characterizing and modeling the Stress Induced Leakage Current (SILC) with the final aim of limiting or control such an issue. However, there is no work which accurately explored the overall cell evolution during Program/Erase (P/E) cycling from a microscopic physical standpoint, especially in NOR technology, whose intrinsic 2D degradation nature makes complex the modeling and the analysis of the combined aging mechanisms. In this thesis, an in-depth investigation of P/E degradation mechanisms in 40nm NOR Flash technology issued from STMicroelectronics is conducted. With the help of advanced electrical characterization and proper TCAD simulation, this thesis provides an accurate understanding, evaluation and modeling of the different aging mechanisms involved during P/E cycling. In particular, the respective roles of Hot Carrier Degradation (HCD) and Fowler-Nordheim Stress (FNS) are pointed out, and their impact on memory cell characteristic drifts and on memory lifetime is assessed. The main challenge is to build a physically-based model which reproduces the Flash cell wear out during P/E cycling. This enables to push the memory lifetime towards its maximum intrinsic performance, as for example by correctly managing the P/E electrical operations. In addition, such an approach allows to assess the limiting physical mechanism factors for memory cell degradation and consequently to take action for some specific process step optimizations.
Embedded Non-volatile 1T floating-gate memories: technological and physical challenges for augmenting performance towards the 28 nm node

Flash memory circuits are embedded in almost every aspect of modern life as their ones and zeros represent the data that is stored on smart cards and in the sensors around us. In floating gate flash memories this data is represented by the amount of charge stored on a poly-Si gate, isolated by a tunneling oxide and an Inter Gate Dielectric (IGD). As the microelectronics industry’s researchers and engineering continuously push the scaling limits, the ability of the devices to hold their information may become compromised. Even the loss of one electron per day is too much and would result in the failure to retain the data for ten years. At such low current densities, the direct measurement of the leakage current is impossible. This thesis presents a new way, Oxide Stress Separation, to measure these currents by following the changes in the threshold voltage of the flash cell. The novelty of the technique is that the biasing conditions are selected such that the stress occurs entirely in the IGD, allowing for the reconstruction of an IV curve of the IGD at low biases. This thesis also describes the process changes necessary to integrate the world’s first 40 nm embedded flash based on an alumina IGD, in replacement of the standard SiO2/Si3N4/SiO2. The interest in high-k materials comes from the motivation to make an IGD that is electrically thin to increase coupling while being physically thick to block charge transport. As embedded flash at the 40 nm node nears production, the approach to be taken in future nodes must also be discussed. This provides the motivation for the final chapter of the thesis which discusses the co-integration of the different IGDs with logic devices having the high-k metal gates necessary at 28 nm and beyond.

Evaluation and characterization of security robustness of OxRAM technology against fault injection attacks

The first semi-conductor memories appeared in the 1960s. Since then, memories that are embedded on integrated circuits have evolved significantly. An important downsizing of these memories has been performed and they are still able to store more and more data. However, Flash technology - which is the most spread non-volatile memory technology nowadays - is facing scaling and power consumption issues. Numerous alternative solutions have emerged (emerging technologies) to replace Flash or to be integrated in smart objects, whose one of the main features is low power consumption. In the years to come, billions of devices connected to each other will exchange personal data that need to be secured. Flash technology has already been the subject of many studies, allowing it to be considered secured. Nevertheless, nothing has been performed yet as far as emerging memories are concerned. This thesis proposes an evaluation of the secure character of one of these technologies, whose performances are promising: OxRAM. The first chapter of this manuscript will deal with the state of the art of the different kind of existing memory technologies. It will also list the different means that can be used to assess the security of a memory technology. This allowed to experiment attacks on an integrated circuit which embeds OxRAM. However, the results showed that more accurate studies are necessary to understand the observed effects. Chapters 3 and 4 will then demonstrate the vulnerabilities noticed on OxRAM memory cells through different LASER attacks. The source of these vulnerabilities has also been investigated, which allowed to propose tracks for countermeasures in order to protect integrated circuits that are to embed such memories.
In this thesis, an in depth memory stack optimization is done to make up the OxRAM memory cell in order to be integrated into a matrix of memories. Thus, various top and bottom electrodes and various switching oxides have been studied in order to better control and improve the variability of the resistive states of the OxRAM memory cell. An evaluation of the reliability and the main memory performances in terms of Forming voltage, memory window, endurance and thermal stability were performed for each memory stack through electrical characterizations. These assessments highlighted efficient memory stacks which have been integrated into a 16Kb demonstrator. Finally, a study of the variability of the resistive states as well as their degradation mechanisms during the endurance and thermal stability were carried out through simple models and atomistic simulations (ab-initio calculations).
SARRAZIN Aurélie
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**Development of advanced techniques for patterning sub-10 nm CMOS processes**

For sub-10 nm CMOS technologies, the semiconductor industry is facing the limits of conventional lithography. Several alternative techniques have been proposed to allow 20 nm patterns. In this thesis, we have proposed to focus on spacer patterning technique and Directed Self-Assembly of block copolymers (DSA). We have developed a spacer patterning integration which allows to pattern 20 nm-wide lines. A study has been carried out with materials available at CEA-LETI. Thus, we have studied the different challenges induced by this integration for the following technologic nodes. Concerning Directed Self-Assembly of block copolymers (DSA) technique, one of the main challenge concerns the mask creation by removing a polymer selectively to another. For our study on PS-b-PMMA, we have studied PMMA removal selectively to PS by plasma etching. Plasma chemistries have been developed for removing PMMA selectively to PS on cylindrical and lamellar patterns.

BOUANANI Shayma
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**Towards the industrialization of directed self-assembly of block copolymers: development of lithographic processes compatible with sub-10 nm technology nodes for contact applications**

The competitiveness-chasing in which industrial manufactures are involved, leads to an exponential increase in the number of functionalities per chips, as well as reducing their unit cost, which results in a continuous decrease of their size. To achieve this, DSA (Directed Self-Assembly) of block copolymers, combines conventional lithography techniques with the molecular-scale organizational properties of copolymers. In this framework, the overall objective of this thesis is to evaluate the industrialization potential of the DSA process by graphoepitaxy for contact hole shrink and contact multiplication applications. In particular, it is necessary to demonstrate the ability of this technique to meet the ITRS specifications in terms of CD uniformity, misalignment and hole open yield. A first study on contact shrink, based on the impact of material properties, surface affinity and guiding feature size, allows us to understand the mechanisms involved in the appearance of defects. A second part of the study deals with contact multiplication. To address this application, two types of guides have been studied: elliptical guiding patterns and more complex ones called “peanut”. The study of the process window in terms of process parameters such as annealing time and temperature, but also commensurability was conducted. Particular attention was paid to guide size variation and its impact on DSA final pitch. Experimental data from this study were correlated with simulations. The success criteria are based on the lithographic performances that must be judged through advanced metrology. The development of a specific metrology to measure the placement error of contacts as well as their pitch was conducted, which allowed to propose tracks for countermeasures in order to protect integrated circuits that are to embed such memories.
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Study of an innovative line/space directed self-assembly lithography of block copolymers for the conception of sub 20nm CMOS devices

There is a fixed limit to the maximum resolution the photolithography can provide in the context of the integrated circuit's size reduction encouraged by the microelectronic industry. The Directed Self-Assembly (DSA) of block copolymers (BCP) can be used as a complementary technique enabling smaller critical dimensions of features (CD) obtained by density multiplication of initial, loose i193 lithography patterns. These materials can undergo specific phase separation to self-assemble into periodic, sub-20nm ordered nanostructures. Fast, cost-efficient and highly compatible with equipment and techniques already in use in the industry for line/space (L/S) applications, the different DSA processes found in literature still suffer from defectivity, roughness and CD uniformity (CDU) issues. Most successful solutions are made possible at the loss of some of the most appealing DSA features, mainly its compatibility with current i193 lithography. In this context, the work of this thesis studied and proposed innovative solutions to the problematics posed when using graphoepitaxy […]

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Study of plasma processes for stripping of implanted photoresist for CMOS and photonics applications

Stripping photoresist after High Dose Implantation (HDI) is becoming a critical step with the increase of both implantation acceleration energy and dose. During this step, the photoresist is bombarded by the ions and a modified layer called “crust” is formed at the surface. This layer is difficult to remove with current processes and plasma chemistries without leaving residues and damaging the materials in presence. This study focuses first on the implanted photoresist characterization to understand the photoresist modifications induced by the implantation on the setting of robust experimental protocols. The major phenomenon observed is the resist crosslinking with a decrease of the oxygen and hydrogen content which results in an increase of photoresist density and hardness. Thanks to this understanding, the dry strip process using standard or alternative chemistries has been studied in terms of residues removal efficiency, impact on substrate and ashing rate. The oxidative chemistries allow to achieve the highest ashing but some SiO2 residues coming from substrate sputtering remain. On the contrary, the reductive chemistries are efficient to remove residues but the ashing rate is lower. Besides with such chemistries containing hydrogen, two phenomena are observed: photoresist popping and blistering in the silicon substrate. These issues are studied and solutions are proposed.
Developement of 3D structuring process for silicon

This thesis deals with the development of a patterning process for silicon substrates. Based on ion implantation through a resist pattern to locally modified the underneath layer. Wet etching processes have been developed to reveal the shapes transferred into the silicon substrate. Thanks to morphological, physical and chemical characterizations, modifications induced by ion implantation have been identified and understood. Two ion species (argon and hydrogen) were used in this thesis in order to assess either physical or chemical modifications in silicon substrate. Several wet chemistries: alkaline, acid and dissolution by anodization, were investigated to reveal the final shape. The optimization of the implantation and wet etching processes allowed to obtain 2D and 3D structures with silicon substrate. Moreover, our approach has been successfully implemented to pattern 2D shapes in SiOCH and silicon nitride.
GHEGIN Elodie
Université Grenoble Alpes (France)

Integration of innovative ohmic contacts for heterogeneous III-V / Si photonic devices

Since the 2000s, the requirements in terms of data exchange never stopped rising owing to a multitude of emerging communication means. These extensive modifications lead the signal processing and electrical technologies to switch towards optical devices and interconnections. Among others, these new technologies require the use of III-V-based emitters and receptors. In order to miniaturize these devices, to optimize the performances and to minimize the fabrication cost of such a technology, an innovative manufacturing model consists in integrating directly the III-V laser source onto the 200 mm Si photonics circuit. To enable the development of contacts meeting the constraints of a front-end / middle-end Si-environment along with those of an operating laser, one of the keys lies in the development of contacts on n-InP and p-InGaAs which are necessary to electrically pump the III-V laser.

This Ph.D thesis therefore deals with the development of an innovative contact architecture fulfilling the requirements of a front-end / middle-end Si-dedicated clean room environment while optimizing the performances of the III-V laser [...]. Thanks to these studies, the metallizations and processes allowing an optimization of the electrical performances of the integrated contacts while ensuring their stability are finally identified to reveal the final shape. The optimization of the implantation and wet etching processes allowed to obtain 2D and 3D structures with silicon substrate. Moreover, our approach has been successfully implemented to pattern 2D shapes in SiOCH and silicon nitride.

MORCOS Bishoy
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Development of a process for the synthesis of magnetic metal nanoparticles in ionic liquids

Metallic nanoparticles (NPs) exhibit unique physical and chemical properties. However, their use is conditioned by the ability to control their size and structure. The decomposition of organometallic (OM) precursors under H2 is efficient to generate metallic NPs in organic solvents, but also in ionic liquids (ILs). We have shown that in the latter media, the size can be finely tuned without adding stabilizing agents. Moreover, the resulting “naked” metallic NPs are suitable for catalysis or further reaction with a second OM precursor to form bimetallic NPs.

In this work, we applied this knowledge to the synthesis of mono- and bimetallic NPs in imidazolium-based ILs C1CnImNTf2. Co-NPs with a diameter of ca. 4 nm were successfully synthesized by decomposition of [Co(η3-C8H13)(η4-C8H12)] under H2. Structural analysis and magnetic characterizations demonstrated that these NPs are metallic and, as expected for this size, superparamagnetic. This approach was extended to the synthesis of bimetallic CoPt and CoRu-NPs. It turned out that the best strategy is probably to simultaneously decompose the Co and Pt (or Ru) precursors. This reaction provides monodisperse suspensions of NPs, a good indication that they are bimetallic. Further structural characterizations, in particular using anomalous SAXS, are also considered to elucidate their structure.
ROYAL Aurélie  
Université Grenoble Alpes (France)

Study of implanted hydrogen trapping and application to thin Silicon layer transfer

The development of the advanced microelectronics requires the manufacturing of SOI (Silicon-On-Insulator) wafers with a very thin top Si layer (around 10 nm) and drastic uniformity specification (<=+/- 0.5 nm on 300 mm wafers). An interesting way to raise this challenge would be to integrate, in the Smart Cut™ technology, modified donors substrates in order to “force” hydrogen to precipitate, during the annealing, in a plane parallel and close to the surface.

In this work, we study the potential benefits of the incorporation of thin buried layers of boron doped silicon (Si:B) or SiGe alloy in the donor substrate. We show that Si:B is particularly interesting: fracture is obtained for a lower implanted hydrogen dose and for a lower thermal budget than when using a SiGe buried layer. Moreover, the layer roughness after transfer is obviously lower than that obtained with the reference process. We have shown, using TEM and SIMS, that the mechanisms leading to hydrogen trapping are different in these two types of buried layers. Then, we have studied the hydrogen redistribution after implantation and annealing (by SIMS) and the platelets evolution (by TEM) during isothermal annealing in the Si/Si:B/Si structure. During annealing, the platelets formed outside of the Si:B buried layer dissolved in favor of the ones, larger, formed in the doped layer, which grow and finally form microcracks. This growth results in the transfer of implanted hydrogen towards the trapping layer. Nevertheless, this diffusion is slow and all implanted hydrogen is not finally “pumped” by the trapping layer. A simple numerical model makes it possible to understand then to reproduce qualitatively the redistribution phenomenon observed by SIMS.

This work shows that the incorporation of Si:B buried layer in the donor substrate is a very promising technique for the manufacturing of ultrathin SOI. This process was optimized in an industrial environment and transferred films with a post fracture roughness a decade lower compared to the reference process were obtained.

BECHE Elodie  
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Hydrophilic direct bonding study of dielectric layers

Direct wafer bonding refers to the spontaneous establishment of attractive forces between two surfaces at ambient temperature without any additional polymer material. Available at ambient pressure or under vacuum, this technology is attractive for monocrystal-amorphous stacks, perfectly illustrated by SOI (Silicon On Insulator) substrate elaboration widely used nowadays in microelectronics or microtechnologies. Electronic device performance and multidisciplinarity needs require this technology on many different materials. In this context, a precis understanding of bonding mechanism is paramount. The aim of this work is to study the hydrophilic bonding mechanisms for alumina, nitride silicon and ultra-low k thin films.

In this study, hydrophilic bonding of deposited dielectric films prepared by chemical treatment were analyzed as function of post-bonding annealing temperature. Chemical and mechanical bonding interface closure has been analyzed from mechanical and chemical point of view via several characterization techniques: anhydrous bonding energy measurement, acoustic microscopy, X-Ray reflectivity and infrared spectroscopy. Each material demonstrates interesting behaviors embedded at the bonding interface compared to the deposited film free surfaces. Throughout the studies, correlations between bonding and free surface evolution have led to their bonding mecanisms and some recommendations for efficient and high quality bonding elaboration.

Key words: Direct bonding, aluminum oxide (alumina) bonding, nitride silicon bonding, ultra-low k bonding surface preparation, hydrophilic surface.
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Water management at direct bonding interface

The direct bonding is microelectronic technic which allow to bond two materials without adding adhesive materials. This technic is well known and used to create SOI substrate with the Smart Cut® technic. The chemical affinity, the roughness and the cleanness of the materials are the mains controlled parameters to achieve the bonding. Among the most studied bonding, the Silicon to Silicon hydrophilic direct bonding is the most classical. Studies have shown that the water is able to go through the native oxide layers and to oxide the raw material before 300°C. So this water is accountable of the quality of the bonding and his management study is fundamental in this particular case.

By using many chemistry and bonding atmosphere we were able to create samples with multiples defects density spectrum. With different characterization technics like acoustic scanning microscopy, blade introduction bonding energy measurement, IR and mass spectroscopy and X rays and neutrons reflectivity, we have shown that water is able to penetrate and go out of the bonding by diffusion along the interface. Collaborations with the Laue-Langevin Institute and the European Synchrotron Radiation Facility were necessary to access to some key characterization equipment proving this phenomena. The study of the kinetical movement have shown that it follow a quadratic laws as predicted by the Lucas-Wahsburn equations or an alternative model based on a diffusion law which describe more precisely the evolution of water front shape. Finally, by precisely controlling the water quantity at the bonding interface, before and after the bonding, we manage to obtain silicon to silicon direct bonding with almost no defects regardless of the annealing temperature. It seems that the control of the native silicon oxide nature is determinant factor to obtain this result. We have clearly shown that it is necessary to have a good bonding energy at the moment of the dihydrogen production to prevent the growing of potential existing defects. Therefore the interfacial waters is necessary but so are the nature of the bonding and the control of the generated dihydrogen quantity.

BOUVEYRON Romain
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Development and understanding of III-N layers for the improvement of high power transistors

In order to produce very high performance transistors using GaN based materials, an interesting approach is to replace the AlGaN barriers on a GaN channel with InAlN barriers. This alloy can be lattice matched to the GaN, and has a high piezo-electric coefficient, enabling the generation of a 2-dimensional electron gas with sheet resistance less than 300 Ohm/sq, which is not possible using AlGaN barriers. The objective of this PhD was to develop these layers to be integrated onto the GaN on silicon layers currently used at LETI for high power transistor and diode devices. However, the growth and characterisation of these layers is not simple, especially when grown on silicon substrates, and a large part of this PhD was devoted to the development of appropriate characterisation of these layers. In addition, although the desired layers are ternary (InAlN), the growth frequently has a contamination of gallium from the walls of the chamber, resulting in a quaternary layer which is even more difficult to accurately characterise. A final difficulty of this alloys is the instability of the surface meaning that a capping should be applied within the growth chamber.

The initial work examined the effects of different parameters on the properties of the InAlN layers, and in particular the gallium contamination within them. It was found that regardless of other conditions, the gallium incorporation was strongly related to the flow of the indium precursor (TMIn). The only way to avoid this was shown to be the growth of a GaN channel layer followed by removal of the wafer from the chamber, a chamber clean, and then the regrowth of the InAlN barrier layer on the GaN channel.

The study of the capping layers examined the use of SiN and GaN, finding that although it is difficult to grow the GaN at the low temperatures required to protect the InAlN layers, it was possible to grow thin layers which had good morphology and did not strongly impact the sheet resistance. By combing these steps, a high electron mobility transistor (HEMT) structure was grown with pure ternary layers and GaN cap with a resulting 2DEG showing a resistance of 270 Ohm/sq.
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**Low temperature epitaxy of Si, Ge, and Sn based alloys**

(Si)GeSn is very promising for use in Mid Infra-Red (MIR) group-IV optical components on chip. During this PhD, I have studied the Reduced Pressure Chemical Vapor Deposition of GeSn alloys. The very low temperature epitaxy of pure Ge, heavily phosphorous doped Ge and Ge-rich SiGe alloys have first of all been investigated. Using digermane (Ge2H6) instead of germane (GeH4) enabled us to dramatically increase the Ge growth rate at temperatures 425 °C and lower. Very high electrically active P concentrations were obtained at 350 °C, 100 Torr with a Ge2H6 + PH3 chemistry (at most 7.5x1019 cm−3). We have then combined digermane with disilane (Si2H6) or dichlorosilane (SiH2Cl2) in order to study the GeSi growth kinetics at 475 °C, 100 Torr. Definitely higher Ge concentrations (77-82%) and smoother surfaces have been obtained with SiH2Cl2. We have then explored the low temperature epitaxy of high Sn content GeSn alloys in our 200 mm industrial RP-CVD tool. Digermane (Ge2H6) and tin tetrachloride (SnCl4) were used to investigate the GeSn growth kinetics and strain relaxation mechanisms. Large range of Sn concentrations, i.e. in the 6-16% range, was probed and data points used to grow thick, partially relaxed GeSn layers. The benefits of using Step-Graded structures, in terms of crystalline quality and surface morphology, was conclusively demonstrated for thick GeSn layers with high Sn contents. Such a stack, with 16% of Sn in the top part, was direct bandgap and led to a laser operation (in micro-disks) up to 180 K at an emission wavelength of 3.1 μm and with a lasing threshold of 377 kW/cm² at 25K.

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**Characterization of oxygen vacancies in high-k dielectrics used in HKMG stacks**

The presence of oxygen vacancies in high-k oxides is foreseen to have detrimental effects in high-k metal gate MOS transistors. To validate this hypothesis, we investigate the possibility of using electron energy loss spectroscopy in an electron transmission microscope (EELS) and the cathodoluminescence (CL) calibrated by the positron annihilation spectroscopy (PAS) to analyze these defects in thin HfO2 layers.

To develop this methodology, HfO2 films have been deposited both by ALD and PVD on silicon substrates. To make the samples adapted to the PAS depth resolution, the layers thicknesses (10 to 100 nm) are higher than those used in microelectronics. According to XRD, RBS/NRA, MEB, TEM results, these layers present a complex structure and a large excess of oxygen.

PAS results depend both on the deposition technique and on the heat treatment. They evidence the presence of electric fields in the oxide layer or at the interface with the substrate. Electrical measurements in the thinnest layers, confirm the presence of charges in the oxide layer as already mentioned in the literature. The sign of these charges changes with heat treatment and is in agreement with the PAS results. EELS improved data acquisition has been developed. The EELS and CL spectra have been analyzed using a systematic methodology allowing to extracting characteristic parameters. They depend on the deposition technique and the heat treatment. However, due to the poor quality of the layers, it has not been possible to isolate the effects of the stoichiometry. This work opens many perspectives to improve knowledge on phenomena occurring in devices.
Towards the industrial use of synchrotron x-ray nano-tomography for 3D integration failure analysis

This PhD thesis aims at developing new characterization techniques for 3D integration in microelectronics. More specifically, the focus is set on recent ESRF (European Synchrotron Radiation Facility) beamlines, both for 3D imaging by tomography and for strain measurements by Bragg diffraction. 3D integration aims at reducing the global microelectronics devices footprint and connections length, by stacking the dies on top of one another instead of setting them one to another. This new geometry however requires new connections, such as copper pillars (CuP) and copper pads, used in hybrid bonding. The monitoring of their fabrication process requires their imaging in three dimensions, and the measurement of the strain inside them. Those measurements must be conducted on large areas (100 m²), with high resolution (500 nm for strain and 100 nm for imaging). Moreover, given the industrial context of this study, the characterization methods must be as routine and automatic as possible.

To answer those needs, several techniques have been developed in this work. Two 3D imaging techniques have been made compatible with the requirements of 3D integration characterization. A Slice and View procedure has been implemented inside a single beam PFIB, leading to large volumes 3D automated imaging. The tomography workflow accessible on the ID6A beamline of the ESRF has been adapted, in order to limit the human intervention and beam times. This leads to possible statistical measurements on this beamline. Strain measurements have been conducted on the ID01 beamline of the ESRF, on silicon and copper stacks meant for direct and hybrid bonding. They allowed for simultaneous local strain measurements in two independent layers of silicon, and in situ measurements in copper.

In this work, we show the possibilities of synchrotron based techniques (here, tomography and Bragg diffraction) for the characterization of 3D integration devices. We show that, provided some adjustments, these techniques can be used routinely for the microelectronics field.

Optimization of LiPON deposit by RadioFrequency magnetron sputtering for micobatteries production. Plasma-surface interaction modeling

The scale reduction of batteries is a real technological challenge for the near future. These micobatteries, about ten micrometers thick, are used to supply the power for small sized systems. LiPON is one of the most suitable electrolytes considered for industrial scale production. It is deposited in thin-film by radiofrequency magnetron sputtering of Li3PO4 in nitrogen plasma. This thesis is focused on particles behavior in plasma and during deposition. Optical emission spectroscopy and electron density measurements have been performed, to provide data used as input or validation for several numerical models. The first model describes plasma kinetics in the magnetron reactor, as 0D global model, and helps to identify the main chemical species and important reactions. This information has been useful to define a simplified kinetics for the second model, 2D, dealing with the charged species behavior in the plasma and describing target sputtering by ion bombardment. It provides the sputtered areas, ion energy and impinging angle onto the target. These obtained results have been employed in a 3D model that simulates sputtered atoms transport from the target to the substrate and predicting the thin-film features. Some characteristics of the target during sputtering have been highlighted and confirmed by the direct comparison between numerical and experimental results.
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New generation of magnetostrictive materials for energy

In recent years, performances of multiferroic materials have considerably improved with two-phase composites: magnetostrictive and piezoelectric. These composites take advantage of the coupling between magnetism and piezoelectricity through magnetostriction. Thus, they allow control of magnetization with electrical voltage, and conversely, to get an electrical polarization depending on the magnetic field (our focus in this case). This drives electronics towards more environmental friendly solutions, namely with lower circuit power consumption (current controls are replaced by voltage controls) and the replacement of batteries, which must be periodically charged, by sustainable energy harvesting systems. Energy harvesting solutions are popular with the Internet of Things (IoT). Despite their performance, these multiferroic composites remain perfectible, especially regarding the magnetostrictive phase. Its optimization is essential. The common material is Terfenol-D because of its giant magnetostriction, used in its massive and monocrystalline form. This material remains rare, expensive, fragile and its growing method is not adapted to the manufacturing of miniature devices. This work focuses on a comparative study of Terfenol-D miniature disk manufacturing pathways for the production of energy harvesters. A benchmark study was carried out on a series of disks cut in commercial alloy ingots (monocrystalline and polycrystalline). Next, the isotropic powder sintering method was investigated with very little background on this material. Conventional sintering led to the first functional disks needing no ulterior machining but with low density and mechanical strength. These defects were then corrected using the SPS technique (Spark Plasma Sintering) but the reproducibility over time has yet to be improved. The Terfenol-D disks (both cut and manufactured) were assembled with the piezoelectric phase (commercial PZT). Electrical characterizations using a contactless method have validated their potential to harvest energy, in lesser amounts than monocrystalline Terfenol-D as expected, but in a large enough quantity regarding most of applications. Finally, an alternative solution has been explored with NiMnGa shape magnetic alloys offering very large deformations. A perspective to a wireless autonomous push button prototype is presented at the very end.

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Study of damage failure mechanisms of thin metallic films deposited on flexible substrates for flexible electronic

Over the past 20 years, new improvements in materials and processes led to the development of printed flexible electronics. Flexible electronics devices subjected to bending, twisting, or stretching during their lifetime, the development of device with high reliability is therefore of great importance for the efficiency of electrical connection. This work investigates the mechanical reliability of inkjet or screen-printed Ag thin films on polyimide substrates dedicated to the electrical interconnection of active components. Expected mechanical failure modes are film cracking and buckling delamination. First of all, in order to characterized the two mechanisms, tensile tests are performed under an optical microscope to follow cracks and under an optical interferometer to follow buckles. In order to obtain crack spacing evolution during deformation, an image processing is realized. Two types of cracks are observed: long and straight cracking for thick films and small and zigzag shape cracking for thin films. The evolution of buckles shape with imposed tensile deformation is characterized. In a second time, in order to understand experimental observations, mechanical failure modes are analysed with finite elements models. The origin of the two types of cracking are explained by a geometrical effect of film thickness. A elastoplastic shear lag bidimensional model gives upper and lower bounds of crack spacing during deformation. A three-dimensional model allows identification of cohesive zone model parameters at film/substrate interface, from experimental buckle shape. An adhesion energy of 2 J.m$^{-2}$, a critical strength of 20 MPa and a mode mixity parameter of 0.4 are determined. These values are in good agreement with literature.
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Optimization of physical chemistry of the Pt/Ru/Pb(Zr,Ti)O3 interface for future high capacitance density devices

The growing need for the integration of an increasing number of functions into the new generation of portable devices contributes to overcrowding of printed circuit boards. In this context, the miniaturization of discrete components is imperative to maintain a manageable size of the printed circuit boards. Decoupling capacitors are one of the most important such discrete components. Miniaturization requires an increase of capacitance density, involving the integration of high-density capacitors. The success of such integration relies on the use of both high dielectric permittivity materials and a suitable stacking architecture. Lead zirconate titanate (PZT) in decoupling multiple metal-insulator-metal (multi-MIM) stacks is a good candidate for the new generation of integrated capacitors. The multi-MIM technology consists in stacking two or more PZT film-based MIM structures connected in parallel in order to increase the density of the capacitance without any effective surface area change. Device performance is heavily affected by the quality of the interface with the electrodes, so it is important to engineer interface chemistry, which does not degrade the multi-MIM performance.

This thesis, supported by the French “Programme de l’économie numérique des investissements d’Avenir” addresses two aspects of development aiming to improve the quality of the Pt/Ru/PZT interfaces: the first one concerns the optimization of Pb excess content in the PZT film, while the second one investigates the Post Metallization Annealing (PMA) done after deposition of electrode/PZT multilayer.

The first part of the thesis presents the capacitance density analysis performed on Pt/Ru/PZT/Pt capacitors as a function of Pb excess in the sol-gel precursor solution (10, 15, 20 and 30% of excess Pb for PZT10, PZT15, PZT20 and PZT30, respectively). Pb excess compensates the lead evaporation during calcination.

An increase of Pb excess from 10 to 20% leads to an increase of the maximum dielectric constant of 8.8%, a decrease of the loss tangent from 4.36 to 3.08% and breakdown field from 1.68 to 1.26MV/cm. PMA favors the enhancement of the maximum of dielectric constant by 7.5%, and the breakdown field increases to 0.5 MV/cm.

The influence of the surface chemistry is studied as a function of Pb precursor excess. X-ray photoelectron spectroscopy demonstrates that low level of Pb excess leads to the presence of a ZrOx surface phase in the form of nanostructures. Higher Pb precursor content allows the PZT synthesis to proceed to its end-point, fully consuming the ZrOx precursor and eliminating the low dielectric constant ZrOx surface phase.

We have then studied the Pt/Ru/PZT interface as a function of Pb excess and PMA. TEM cross-sectional analysis shows that the crystalline ZrOx nanostructures are still present at the electrode interface, constituting a dielectric layer which contributes to defining capacitor performance. Operand hard X-ray photoelectron spectroscopy (HAXPES) analysis using synchrotron radiation highlights a polarization-dependent electronic response, most probably due to imperfect screening of the depolarizing field at the Pt/Ru/PZT10 interface. Furthermore, a new component (PbOx) is observed at the Pt/Ru/PZT30 due to the high Pb excess. This component seems to induce a reduction in breakdown field and capacitance density. Finally, PMA on the PZT10 suggests the creation of interface ZrRuOx and PbRuOx which could be at the origin of the improvement of electrical responses of PZT capacitors after PMA.

In conclusion, this thesis has provided valuable information and methodology on the correlation between surface and interface physical chemistry of PZT and Pt/Ru/PZT and electric characteristics of PZT based MIM capacitors.
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