FRANÇAIS ENGLISH

INTACT

3D TECHNOLOGIES
FOR CHIPLET-BASED ADVANCED SYSTEM

WHAT IS INTACT?

INTACT consists of a 96 core architecture composed of 6 chiplets (FDSOI 28nm) 3D-stacked onto an active silicon interposer (CMOS 65nm), fully processed, packaged and tested.

- The chiplet-based architecture benefits of advanced 3D integration scheme including TSV-middle and ultra-fine pitch die-to-die interconnects,
- The active interposer integrates Network-on-Chip's, DC-DC converters, and System IO's.
- The prototype has been assessed morphologically and electrically. Finally, the structural test of the INTACT prototype was reached and is showing results well within expectations onto the application board.
- These results pave the way to the design of future high efficiency systems for high performance computing.

APPLICATIONS

In the context of HPC (High Performance Computing) and AI (Artificial Intelligence) acceleration, there is an ever increasing demand of computing capacity and solutions for specialization and energy efficiency.

- Partitioning a large single die in a multitude of smaller dice leads to reduced costs in advanced nodes, and also to high level of specialization.
- Chiplets can be highly configurable and optimized using adequate technologies: generic computing cores chiplet, GPU chiplet, FPGA fabric chiplet, AI accelerators chiplet for energy efficient AI kernels, advanced memoires such as HBM.
- Finally, IP and chiplet re-use are also one key advantage of such active interposer integration.

Work performed in the frame of the IRT Nanoelec consortium.

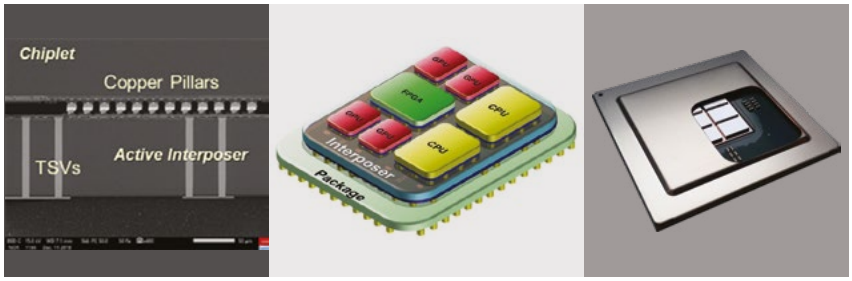
NANOELEC.

WHAT'S NEW?

The main INTACT prototype innovations are related to both technology and architecture:

- **Advanced 3D Technology:** about 150,000 connections between the chiplets and the interposer using ultra fine pitch die to die interconnects (copper pillar 20µm pitch), 14,000 TSVs (10 µm diameter, pitch 40µm) through the active interposer, with 6 chiplets (FDSOI 28nm, 20mm²) 3D-stacked onto the active interposer (CMOS 65nm, 220mm²).

- **Advanced 3D Architecture:** Active Interposer offers Network-on-Chip for chiplet-to-chiplet communication, scalable and configurable cache-coherent L1/L2/L3 architecture, integrated DC-DC converters for chiplet power supplies, system level IO's, Design-for-Test infrastructure, the whole architecture providing a cache coherent 96-core system.



WHAT'S NEXT?

- 3D technology with Chip-to-Wafer Hybrid Bonding technology for ultra-fine pitch chiplet 3D connectivity, and better thermal & mechanical coupling.
- From Active Interposer to Photonic interposer, by using photonic Network-on-Chip, integrated wave guides, E/O conversion chiplets, and 3D technology.
- 3D architecture with dedicated AI accelerators, In-Memory-Computing cubes for energy efficient computing.

MAIN PUBLICATIONS

- P. Vivet et al., "2.3 A 220GOPS 96-Core Processor with 6 Chiplets 3D-Stacked on an Active Interposer Offering 0.6ns/mm Latency, 3Tb/s/mm² Inter-Chiplet Interconnects and 156mW/mm2@ 82%-Peak-Efficiency DC-DC Converters" ISSCC 2020.

- Best session paper award: P. Coudrain, et al., "Active Interposer Technology for Chiplet-Based Advanced 3D System Architectures" ECTC 2019.

- E. Guthmuller et al., "A 29 Gops/Watt 3D-Ready 16-Core Computing Fabric with Scalable Cache Coherent Architecture Using Distributed L2 and Adaptive L3 Caches" ESSCIRC 2018.

INTERESTED IN THIS TECHNOLOGY?

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