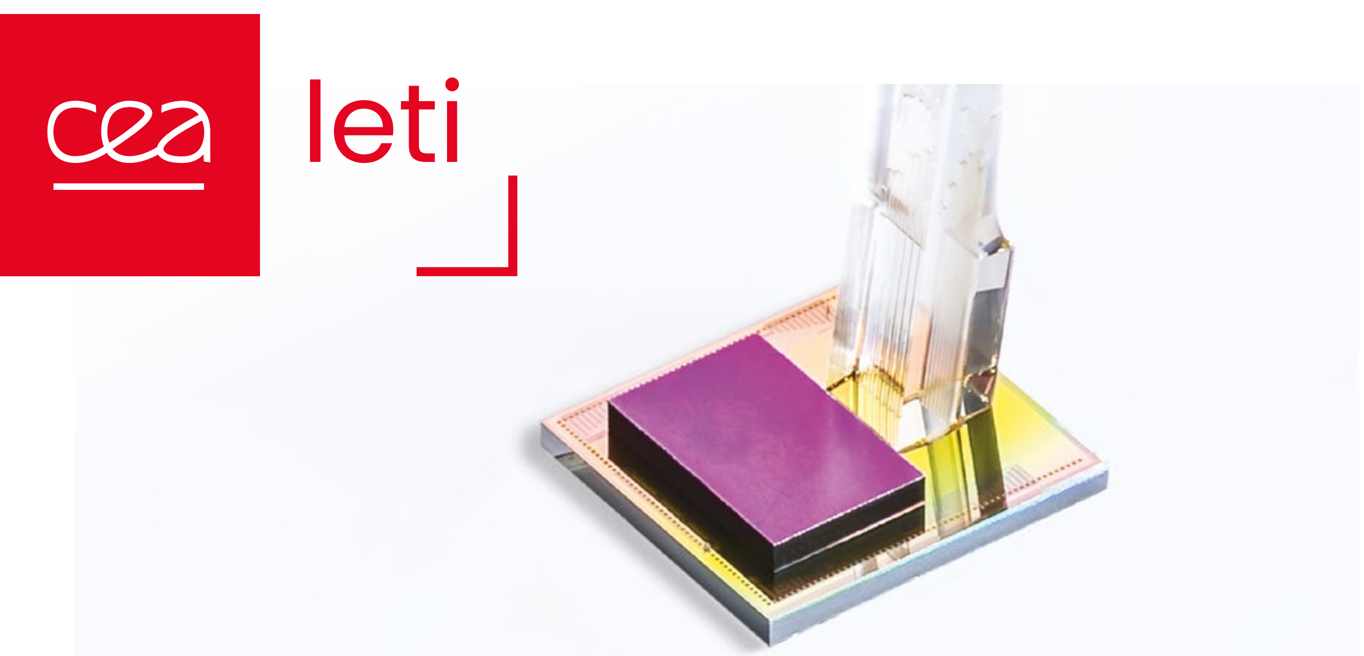


PIC Packaging

High performance packaging towards industrial photonic integrated circuits

What is PIC packaging?

CEA-Leti offers a full set of processes enabling high performance packaging of Photonic Integrated Circuits (PIC). This offer includes:

- Multiple fiber pigtailing leveraging state-of-the-art assembly equipment
- Flip-chip interconnect of the PIC to an Electronic IC (e.g. driver, TIA.); copper pillars or Under Bump Metallization are post-processed on PIC wafers before assembly
- Wire bonding—wedge, ball, or ribbon for RF applications
- Chip-to-package or chip-to-board assembly
- Microoptics assembly (including self aligned processes)
- Photonic Interposer with embedded TSV-mid or TSV-last

The above techniques help package pre-industrial PICs and have them qualified in system environments.
The packaged modules are then tested up to 64 Gbps with state-of-the-art testing & measurement tools.

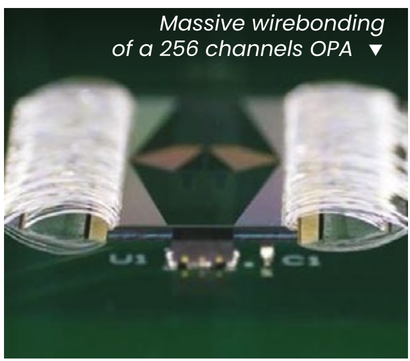
Applications

CEA-Leti packaging technologies have been applied to fiber optic modules targeting the following applications:

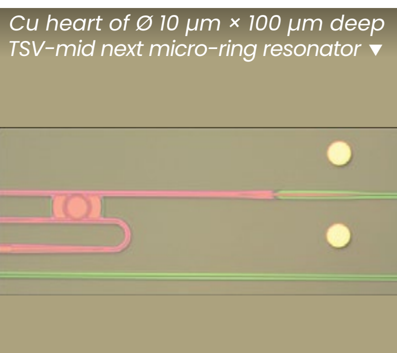
- Fiber Interconnects
  (FTTH,Inter Data Center, Intra Data Center)
- Silicon Photonics based LIDARs
- Quantum computing PICs

How does CEA-Leti's packaging stand out?

CEA-Leti offers a unique integration chain from die to system, including testing and packaging. Our packaging offer leverages all the up-to-date wafer level or die level assembling and all back-end technologies developed at CEA-Leti for years: bumps, copper pillar, micro-tubes, direct die bonding or wafer bonding.

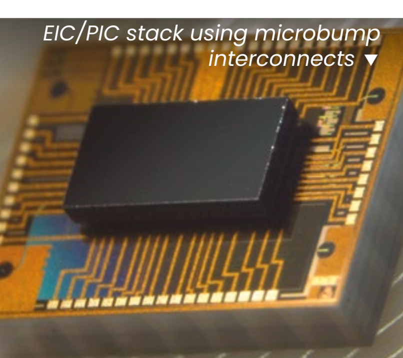


Massive wirebonding of a 256 channels OPA ▼

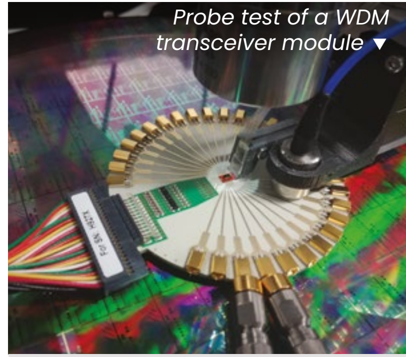


Cu heart of Ø 10 µm × 100 µm deep TSV-mid next micro-ring resonator ▼

Self aligned µlenses array on PIC with sub-micron accuracy ▼



EIC/PIC stack using microbump interconnects ▼



Probe test of a WDM transceiver module ▼

Publications

S.Bernabé et al, "Silicon photonics for terabit/s communication in data centers and exascale computers", JSSC, 2020

T.Mourier et al, "Self-assembly and mass reflow of copper bumps for flip-chip hybridization in photonic applications", ECTC, 2021

T.Mourier et al, "Packaging of a 256 channels Optical Phase array for Autonomous driven vehicles oriented LiDAR", Minapad, 2022

What's next?

For next generation devices (on-board transceivers, photonic interposers), CEA-Leti is currently developing new building blocks:

- Photonic Interposer based HPC architectures (optical network on chip)
- Greyscale lithography optical coupling structures
- Direct laser-PIC passive coupling

Interested in this technology?

Contact:
Eleonore Hardy
eleonore.hardy@cea.fr
+33 438 782 639

CEA-Leti, technology research institute
17 avenue des Martyrs, 38054 Grenoble Cedex 9, France
cea-leti.com

@CEA-Leti

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