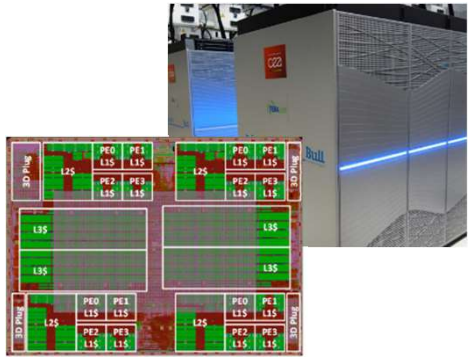
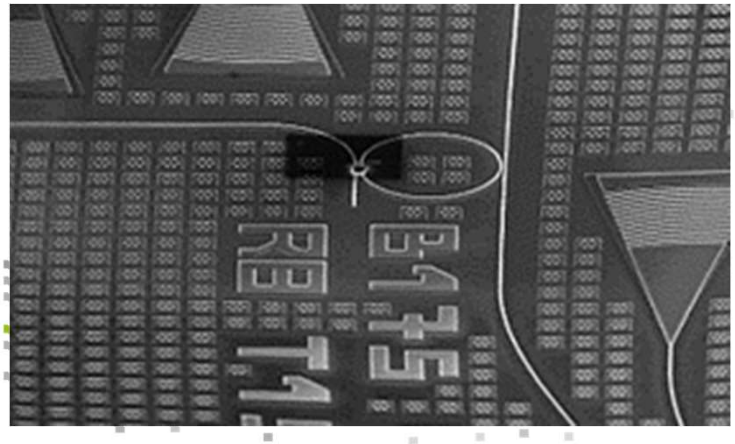




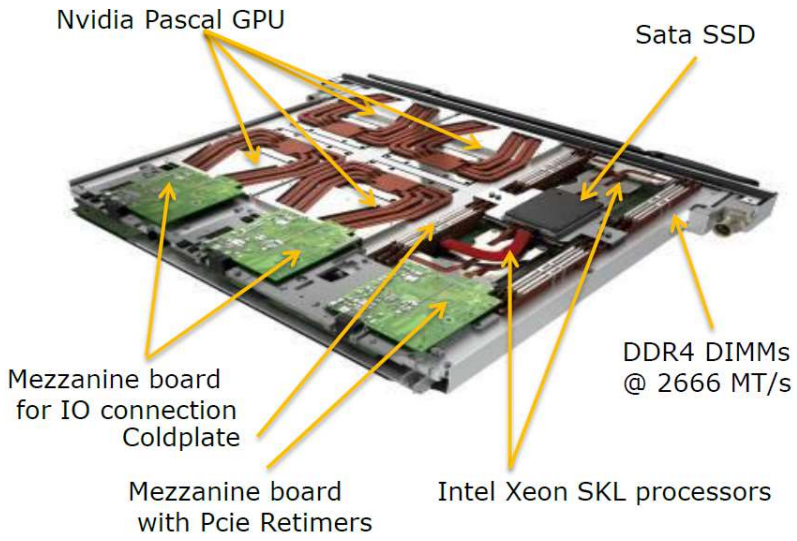
TECHNOLOGIES FOR NEW COMPUTING PARADIGMS

Leti Devices Workshop | Carlo REITA | Dec 2nd, 2018, Nikko Hotel, San Francisco

FUNCTIONS AND CONSTRAINTS

Fundamental functions

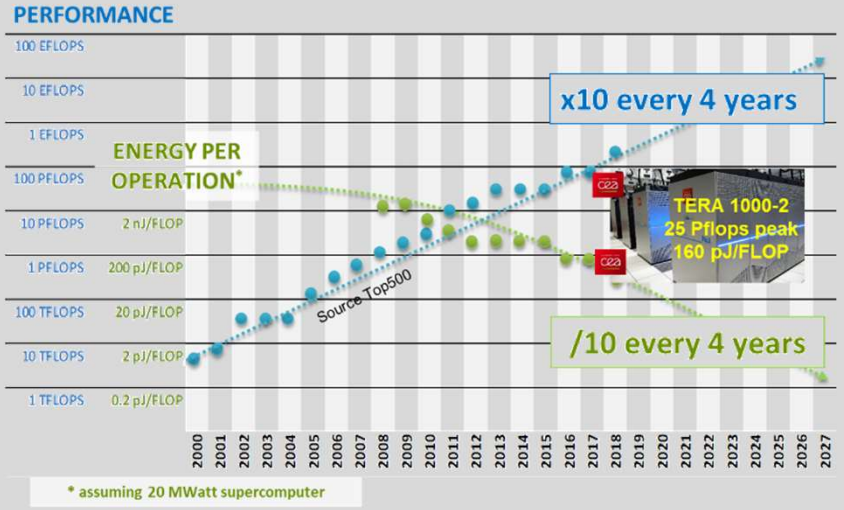
- Compute
- Store
- Transmit



Bull sequana X1125 GPU blade

Constraints

- Power
- Cost
- Performance
- Time to Market



FUNCTIONS AND CONSTRAINTS

Fundamental functions

- Compute
- Store
- Transmit

The on-board computer in Stanford's autonomous Audi TTS. (Image courtesy of Stanford University.)

Constraints

- Power
- Cost
- Performance
- Time to Market

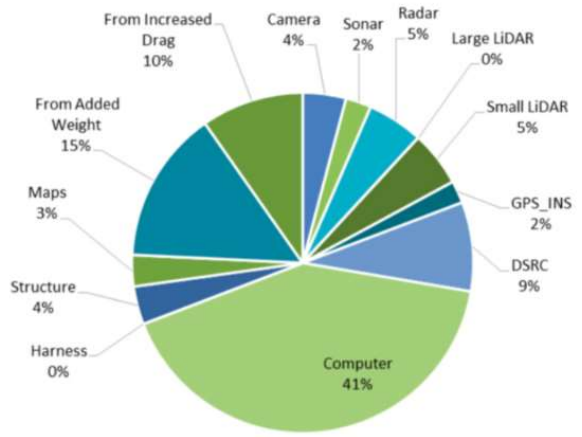


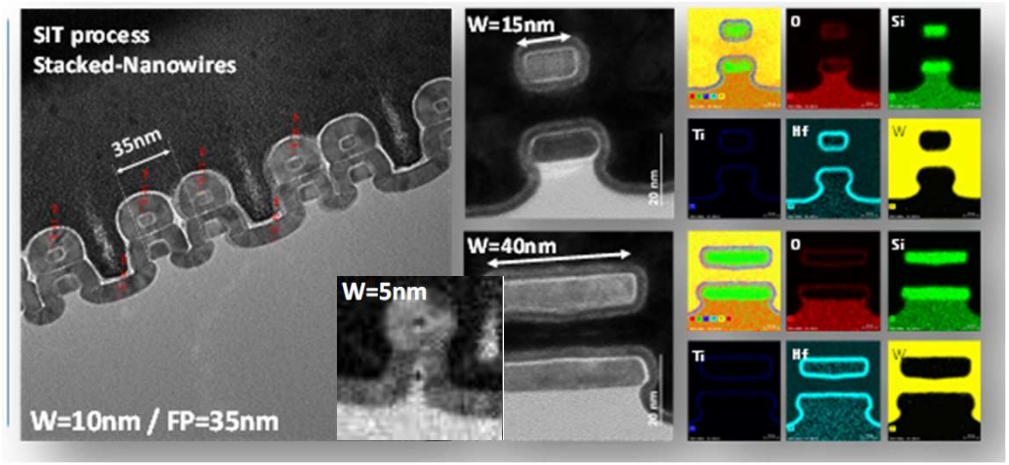
Image: University of Michigan

Sources of added energy consumption from Ford Fusion's autonomy system.

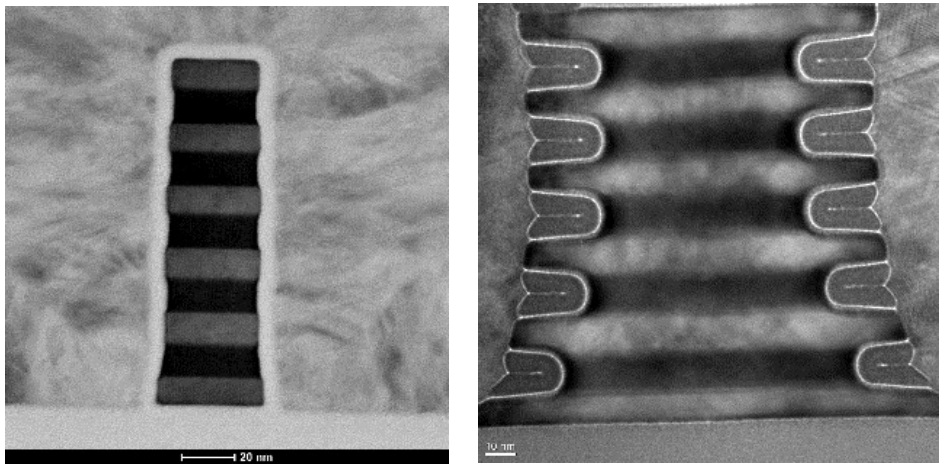
COMPUTE

Performance track

- Scaling of nanosheets for sub 5nm node



Standard gate-last for nanosheets

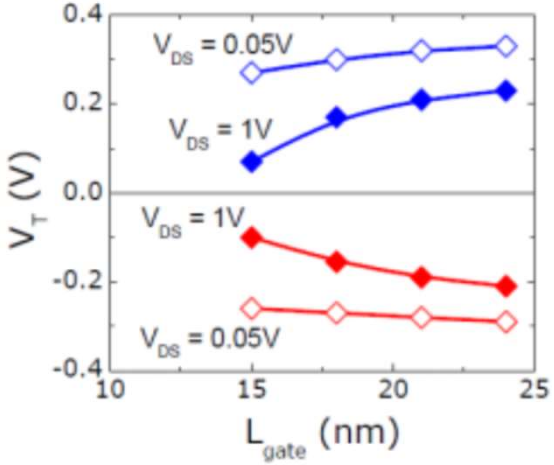


High-aspect ratio (HAR) Gate-last for nanosheets

"Tunability of Parasitic Channel in Gate-All-Around Stacked Nanosheets." S. Barraud et al. this IEDM

COMPUTE

- **Power efficiency track**
  - FDSOI still the best solution and can still be shrinked



O.Faynot, IEDM 2010

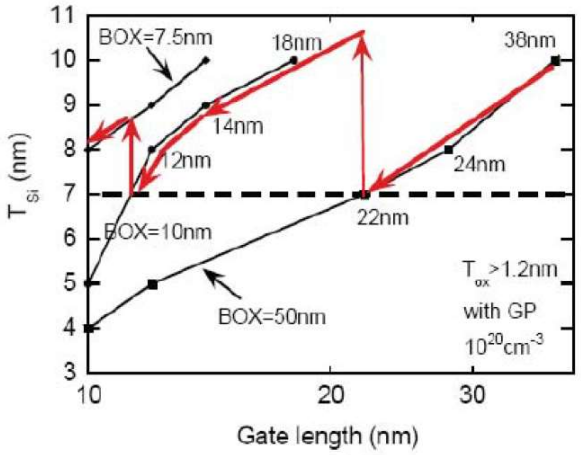
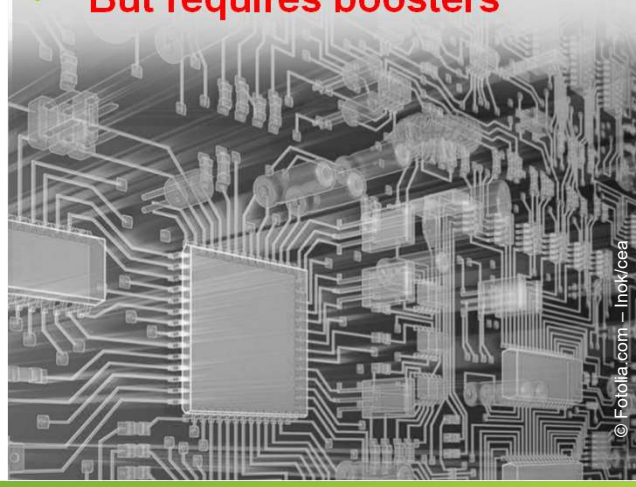


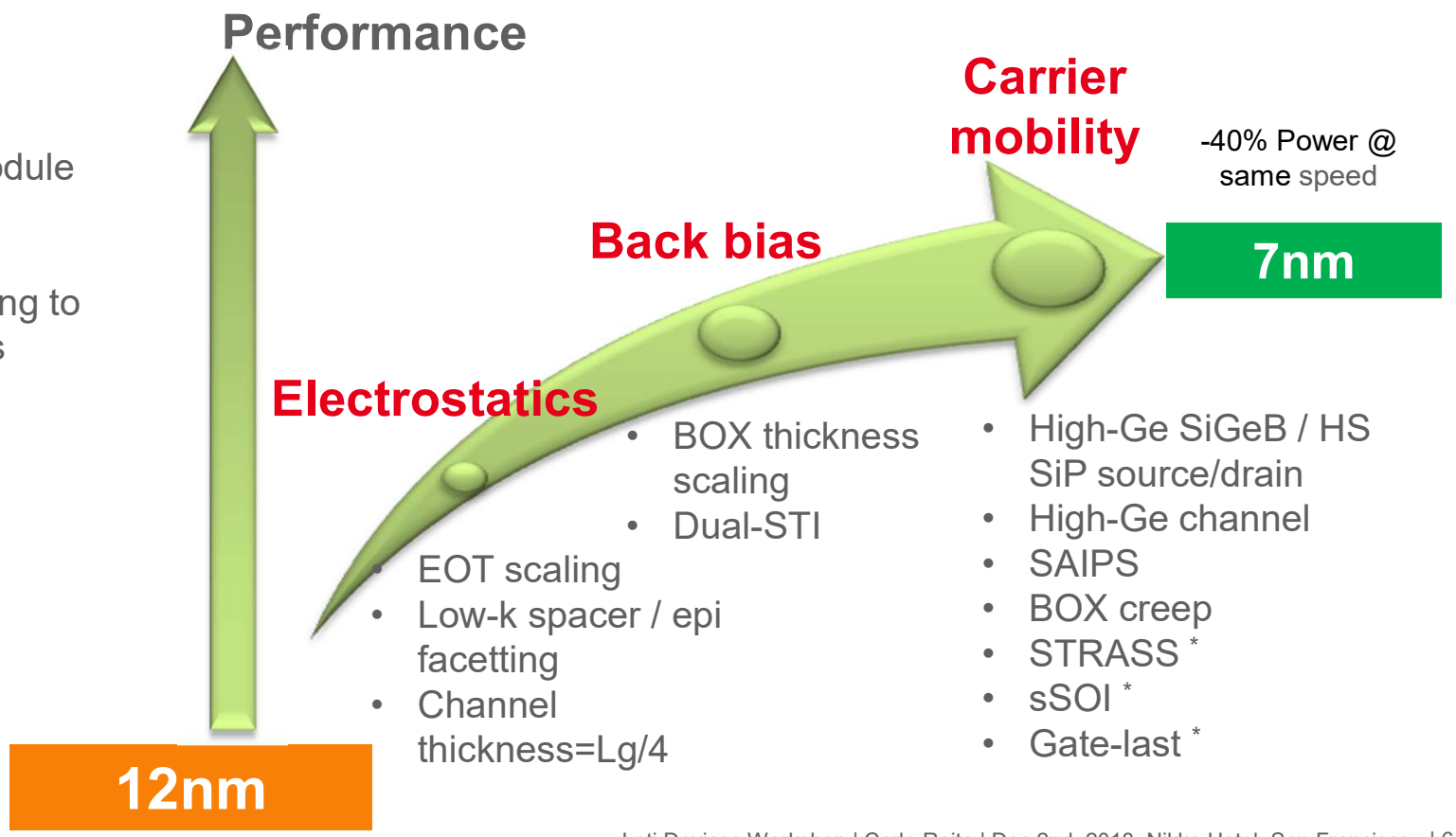
Fig.3: SOI and BOX thicknesses required to achieve a DIBL=100 mV/V as a function of gate length (2)

- **Electrostatic control improved by thinning T_{BOX}**
- **Scalability down to 10nm node**
- **Devices already processed with 3.5nm SOI film**
- **Physical limit L_g=10nm (5nm-3nm node)**
- **But requires boosters**



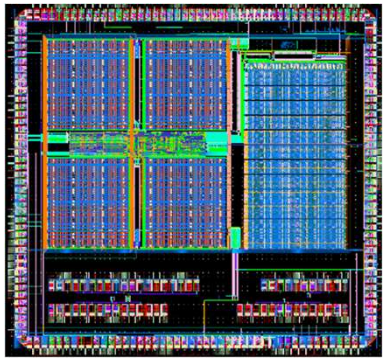
COMPUTE

- **Power efficiency track**
  - Individual boosters validated
  - No roadblock at module level
  - Deployable according to industrial roadmaps



COMPUTE

- **Power efficiency track**
  - Efficiency proven also for new architectures



Chip Name	DynapSEL
Process	ST28FDSOI
Supply Voltage	1V
IO Number	176 + (internal 59)
Chip area	2.8mm x 2.6mm
Core Numbers	4 non-plastic cores 1 plastic core
Neuron Type	Analog AExp I&F
Non-plastic Synapse Type	TCAM based 4-bit
Plastic Synapse Type	Linear 4-bit digital
Throughput of Router	1G Events/second
Scalability	16 x16 chips non-plastic core) 4 x4 chips (plastic cores)

Mixed signal spiking neural network chip in ST FDSOI 28nm technology

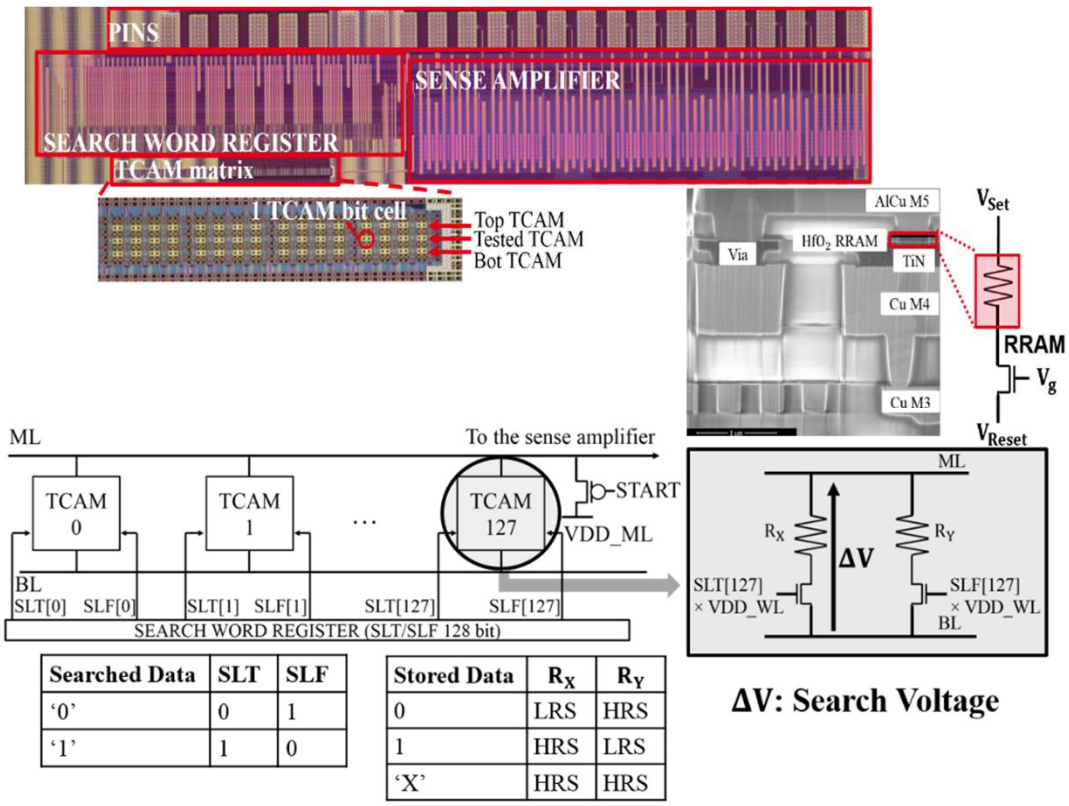
	IBM TrueNorth	Intel Loichi	DynapSEL
Technology	28nm CMOS	14 nm CMOS	28 nm FDSOI
Supply Voltage	0.7-1.05 V	0.5-1.25 V	0.73-1 V
Design Type	Digital	Digital	Mixed-signal
Neurons per core	256	Max 1k	256
Core Area	0.094 mm^2	0.4 mm^2	0.36 mm^2
Computation	Time multiplexing	Time multiplexing	**Parallel processing**
Fan In/Out	256/256	16/4k	**2k/8k**
On-line Learning	No	Programmable	**STDP**
Synaptic Operation / Second / Watt	46 GSOPS/W		**300 GSOPS/W**
Energy per synaptic operation	26 pJ	23.6 pJ	**<2 pJ**

STORE

- **Introduction of resistive memories as replacement for SRAM, embedded flash and stand-alone**
  - Increased density
  - Lower power
  - Better latency
  - New architectures like neuromorphic and more generally In-Memory-Computing

- **One example: OxRAM-based TCAM**

(D. R. B. Ly, et al., “In-depth Characterization of Resistive Memory-Based Ternary Content Addressable Memories”, this IEDM)

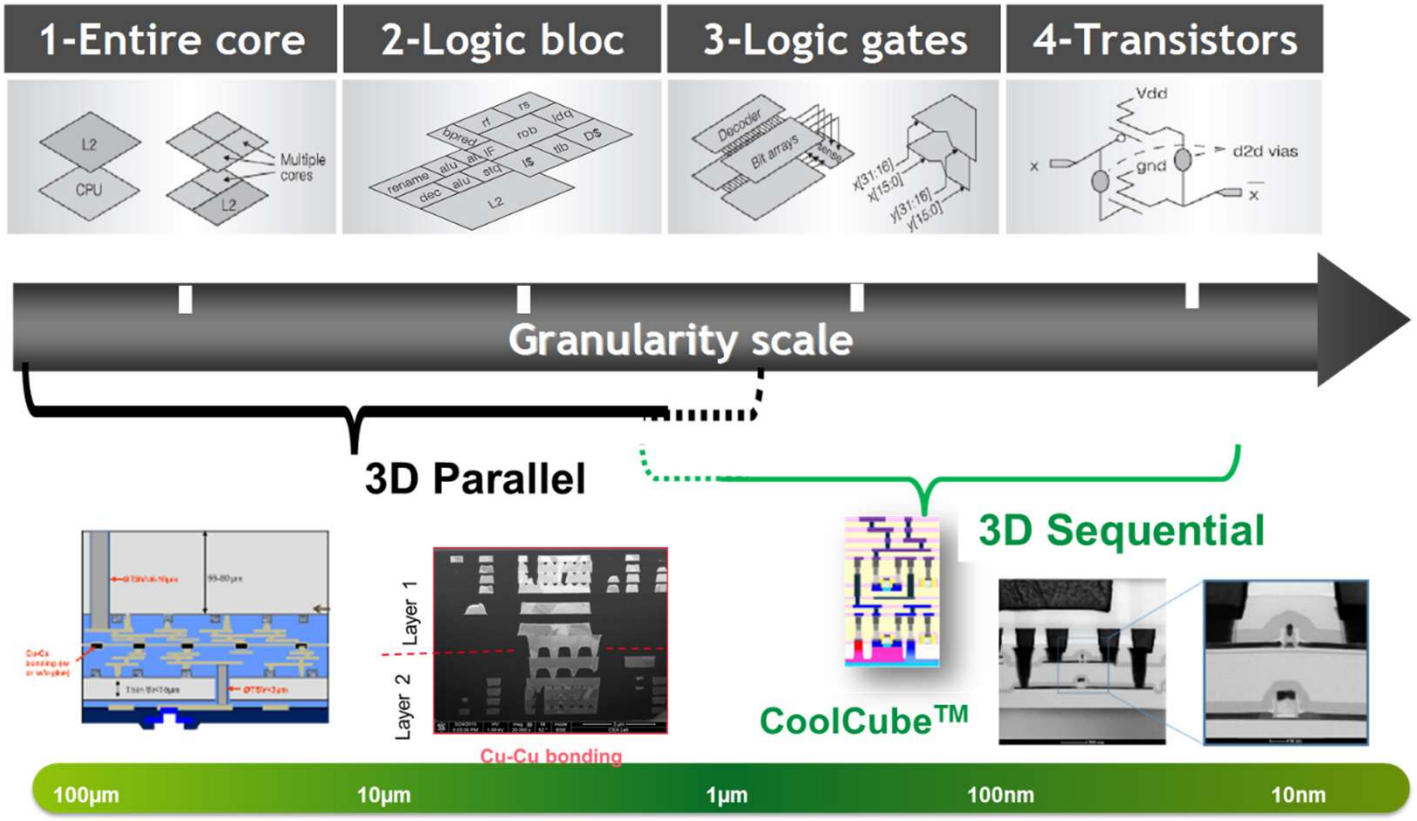


Searched Data	SLT	SLF
‘0’	0	1
‘1’	1	0

Stored Data	R_X	R_Y
0	LRS	HRS
1	HRS	LRS
‘X’	HRS	HRS

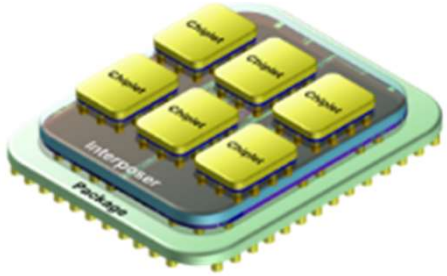
ΔV: Search Voltage

TRANSMIT



- Toolbox of 3D technologies to improve communications between functional blocks
- Heterogeneous integration to make possible new architectures both in HPC (digital-memory) and embedded (digital-memory analog sensors)

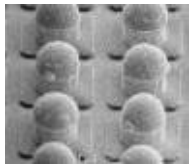
TRANSMIT

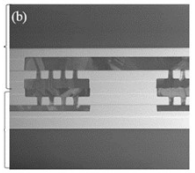


- **Parallel heterogeneous integration, the "chiplet" concept**

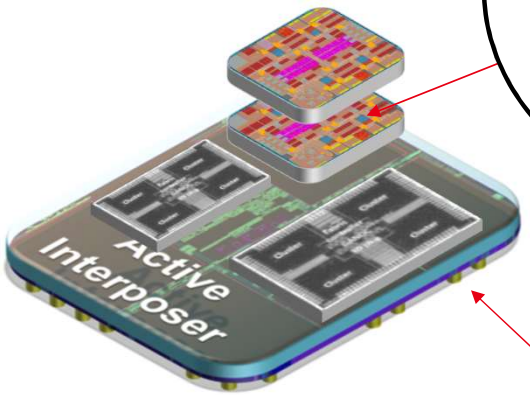
Inter-dies interconnect

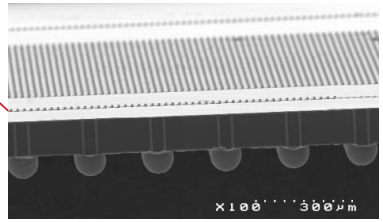
µ-bumps
Ø 10 µm
Pitch 20 µm





Direct Hybrid Bonding
Pitch <10µm
WtW; CtW





Intra-dies interconnect

TSV
Ø 10µm
Height 100µm

28nm FDSOI chiplets (x6)

- Low power compute fabric
- Wide voltage range (0.6V – 1.2V)
- Body biasing for logic boost & leakage ctrl

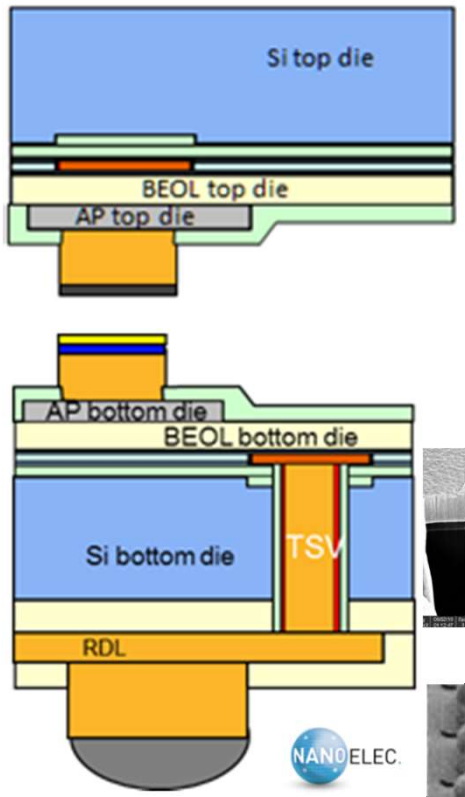
65nm Active Interposer

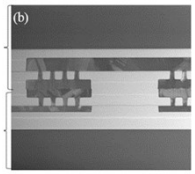
- Power unit (switched Cap DC-DC conv.)
- Interconnect (Network-on-Chip)
- Test, clocking, thermal sensors, etc

This work was funded thanks to the French national program "Programme d'Investissements d'Avenir, IRT Nanoelec" ANR-10-AIRT-05.

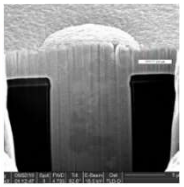
TRANSMIT

- **Parallel heterogeneous integration**

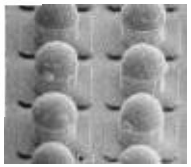




Direct Hybrid Bonding



TSV
Ø 10µm
Height 100µm



µ-bumps
Ø 10 µm
Pitch 20 µm

28nm FDSOI chiplets (x6)

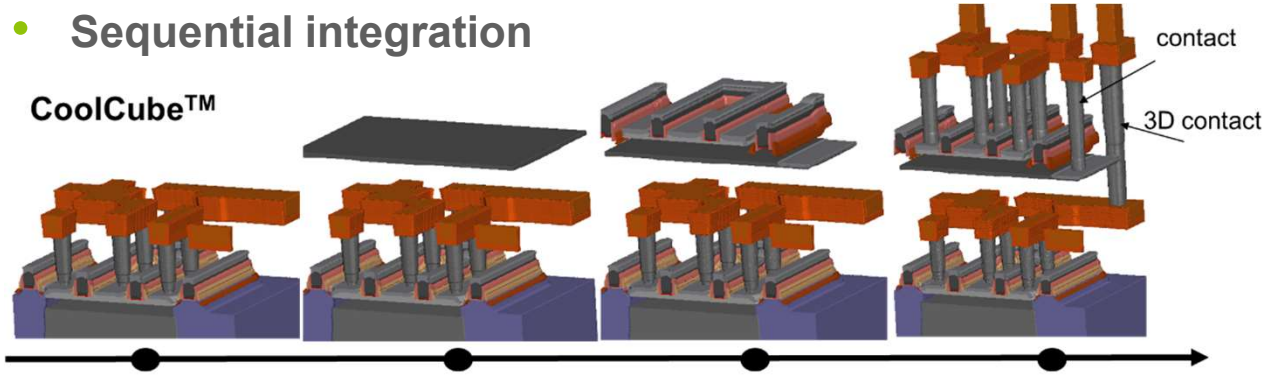
- Low power compute fabric
- Wide voltage range (0.6V – 1.2V)
- Body biasing for logic boost & leakage ctrl

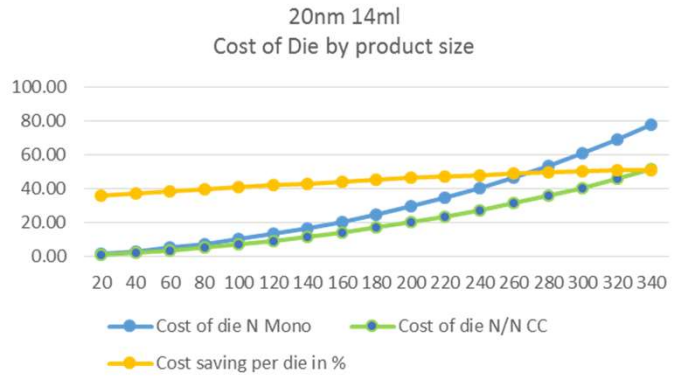
65nm Active Interposer

- Power unit (switched cap DC-DC conv.)
- Interconnect (Network-on-Chip)
- Test, clocking, thermal sensors, etc

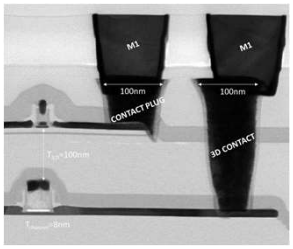
TRANSMIT

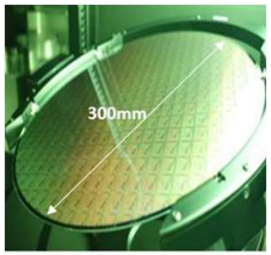
- Sequential integration



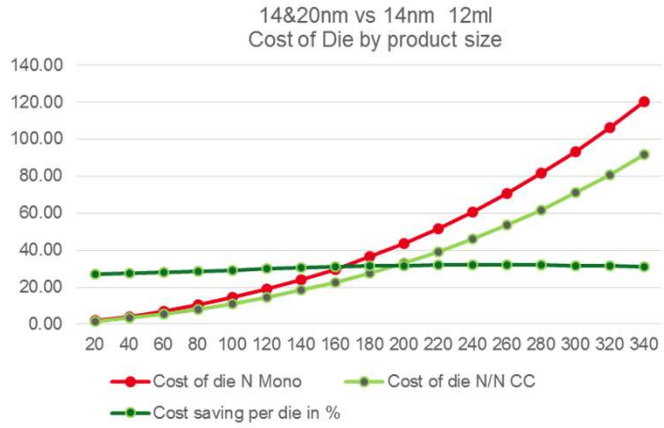


- Extension of FDSOI, but FinFET/FDSOI heterogeneous possible
- 300mm demonstrated
- Reliability demonstrated
- Cost model available



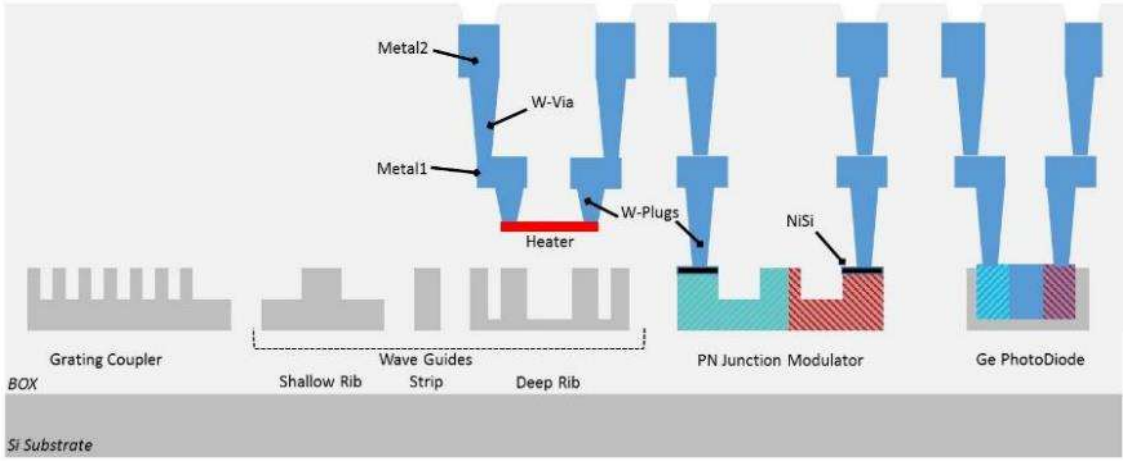


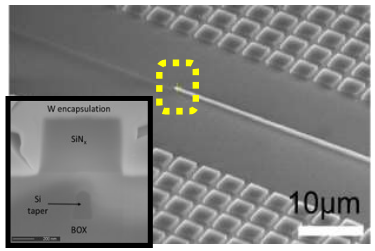
BTI@T=125°C Crit=50mV	VG@10y/3σ, PASS if VG>0.9V
PMOS (TL/BL)	0.98V/1.01V OK
NMOS (TL/BL)	1.26V/1.37V OK



TRANSMIT

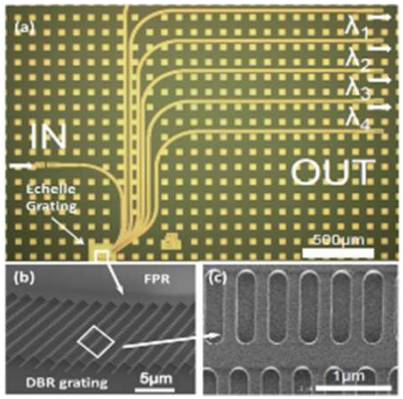
- **Towards 3D Photonics**
  - SOI core photonics process in 300mm
  - SiN layer integrated on top of the Si
  - SiN-based devices:
    + low propagation loss
    + low thermal sensitivity
    - no active device

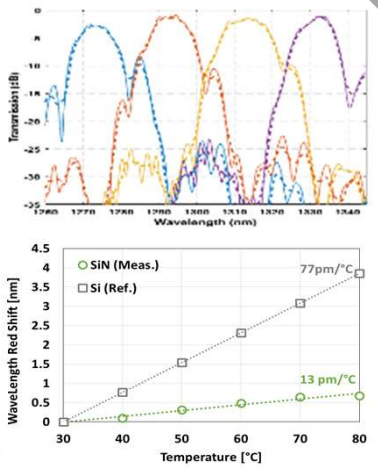




Loss <0.1 dB/transition

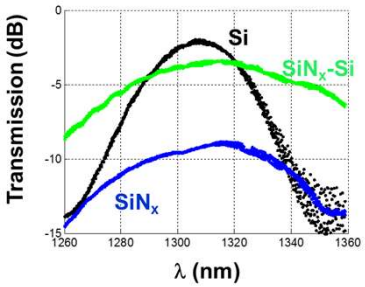
Low thermal sensitive SiN Mux/DeMux

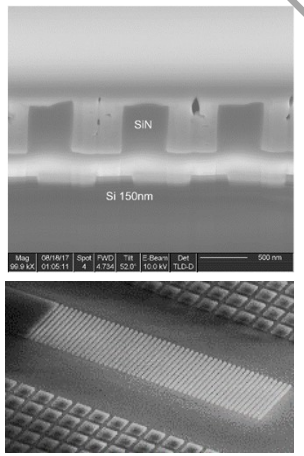




C. Sciancalepore et al., SSDM 2017

High-efficiency & wide bandwidth Si-SiNx grating coupler



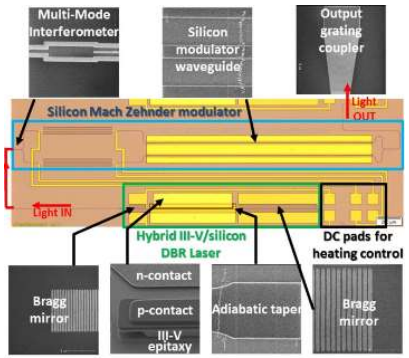


W.D. Sacher, Optical Express, Vol. 22, No. 9, 2014

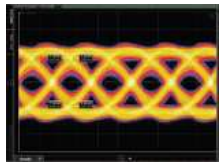
TRANSMIT

- **Heterogeneous III-V on Si integration**
  - Laser
  - Electro-absorption modulator
  - Semiconductor optical amplifier
  - Localize III-V by die-to-wafer bonding:

25Gb/s laser + MZM transmitter



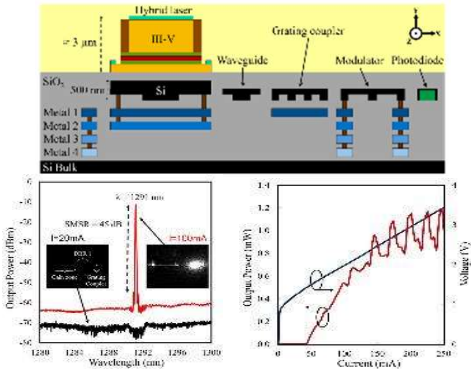
- Co-integration: hybrid IIIV/Si DBR laser + Si Mach-Zehnder modulator.



- 25Gb/s transmission @1.3µm up to 10km.

T. Ferrotti et al. ,1.3µm hybrid III-V on Silicon Transmitter Operating at 25Gb/s SSDM, (2016)

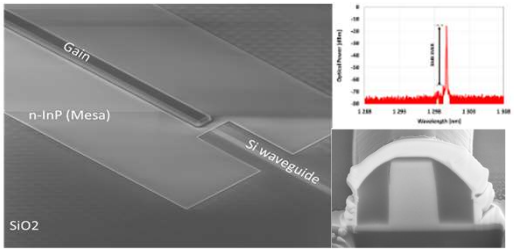
Back-Side integrated hybrid laser



- New back side integration of a hybrid laser compatible with CMOS based photonic platform.
- Single wavelength behavior with SMSR higher than 35dB.
- Lasing threshold around 45mA with an output power >1.15mW at 200mA.

J.Durel et al., First Demonstration of a Back-Side Integrated Heterogeneous Hybrid III-V/Si DBR Lasers for Si-Photonics Applications, IEDM (2016)

CMOS-compatible hybrid laser

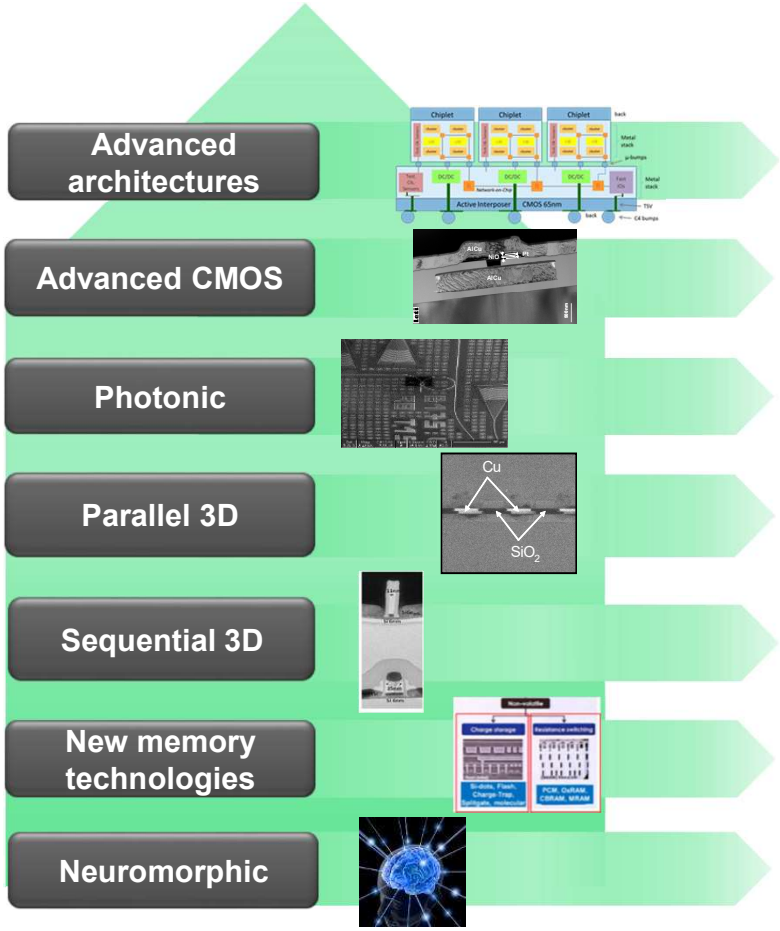


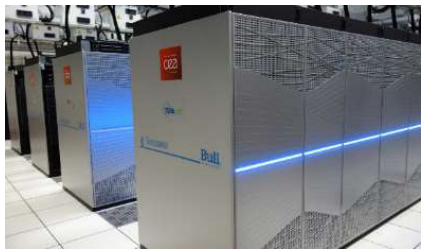
- Front side integration of a hybrid III-V/Si laser in a fully CMOS compatible 200mm technology.
- CMOS compatible metallization (no noble metals) and patterning (no lift-off) processes.
- Single wavelength behavior demonstrated with SMSR higher than 50dB.
- Lasing threshold around 60mA with a 3mW output power at 190mA.

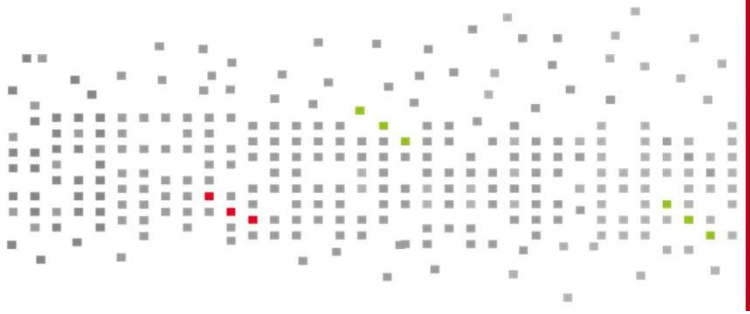
B. Szelag et al., Hybrid III-V/Si DFB laser integration on a 200 mm fully CMOS-compatible silicon photonics platform, IEDM (2017)

CONCLUSIONS

- Leti keeps providing the development of basic technologies to support the needs of data treatment for the mid and long term
- Specific solutions are studied to provide benefits for specific applications as variation on common core elements
- CEA is a major player to support processes and technologies for European Industry and their partners







Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
Minatec Campus | 17 avenue des Martyrs | 38054 Grenoble Cedex | France
www.leti-cea.com