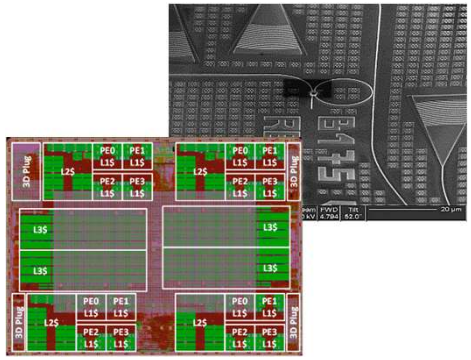


ENABLING HETEROGENEOUS HIGH-PERFORMANCE PROCESSORS

Leti Devices Workshop | Dutoit Denis | Dec 2nd, 2018, Nikko Hotel, San Francisco

TECHNOLOGICAL BACKGROUND

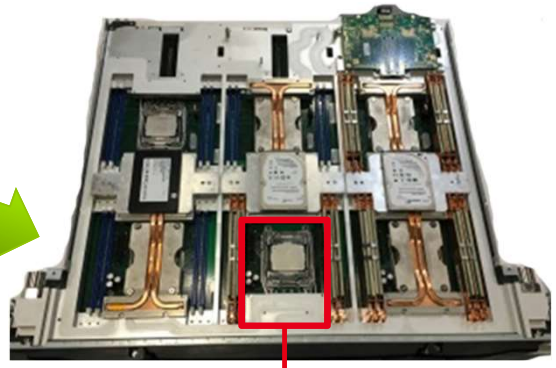
Supercomputer

TERA1000 - CEA

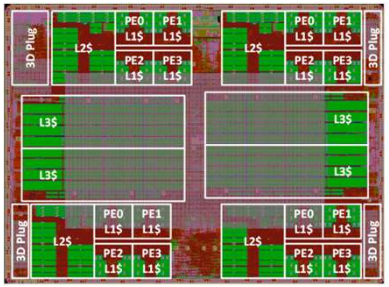
Cluster

ATOS - Sequana

Blade



Processor

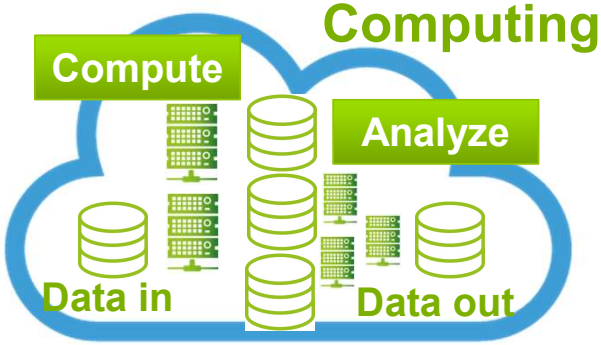


Next to come:
Exascale = 10^{18} Flop/s
a billion billion
operations per second

Leti's technologies to enable heterogeneous high-performance processors

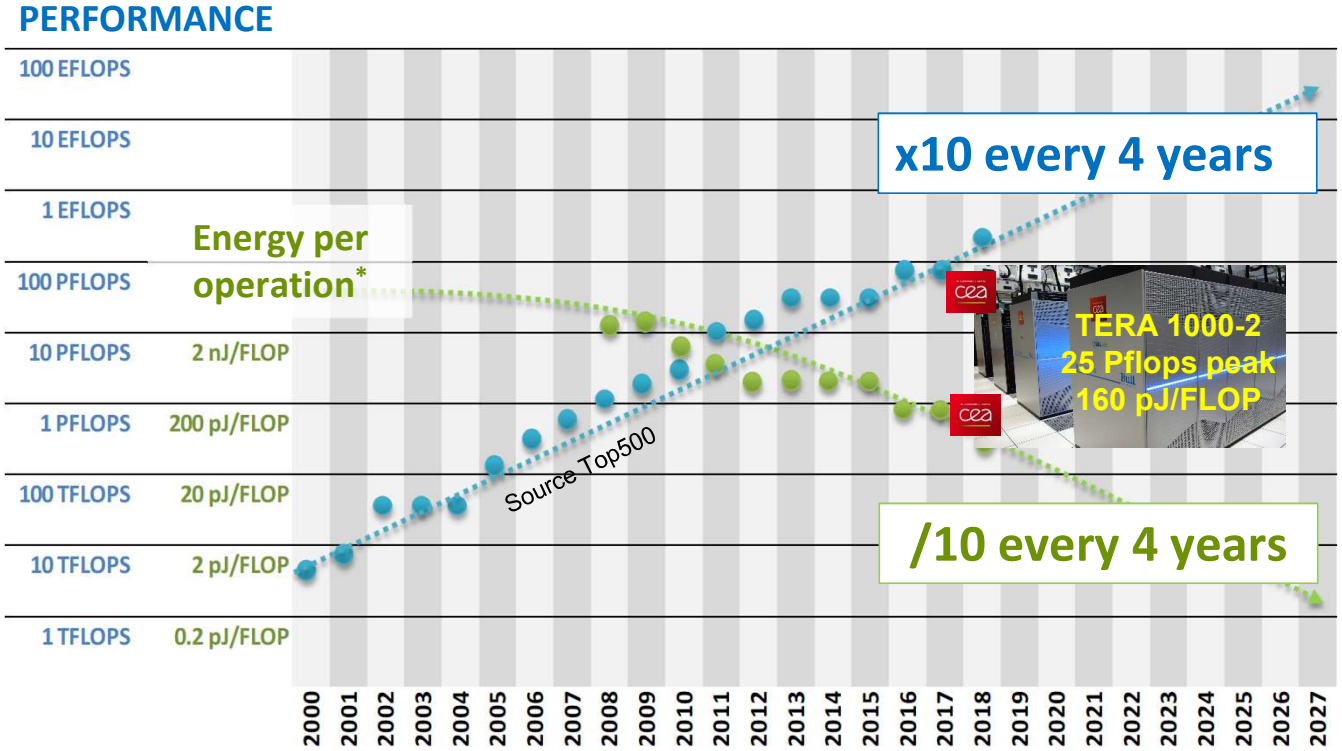
HIGH-PERFORMANCE COMPUTING EVOLUTION

High-Performance Computing



- **Starting from high performance compute only, HPC evolves towards:**
  - New workloads
  - Massive volume of data

10x energy efficiency improvement every 4 years



* assuming 20 MWatt supercomputer

PROCESSOR ARCHITECTURE EVOLUTION

End of Dennard's scaling

End of Amdahl's law

Moore's law slow-down

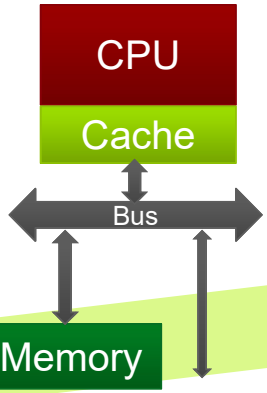
Quantum Computing

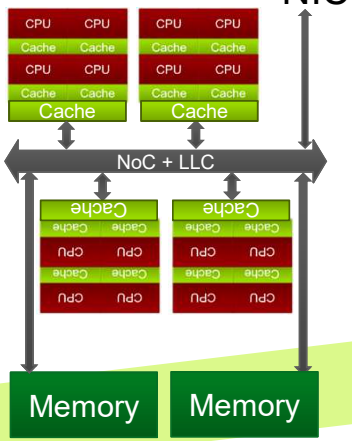
Mono-core architecture for single thread performance

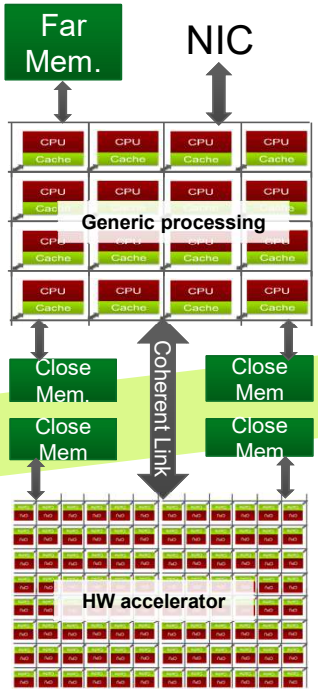
Many-core architecture for parallelism

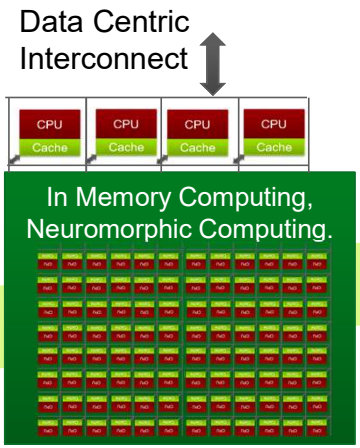
Heterogeneous architecture for energy efficiency

Disruptive architecture for data management









Memory invades logic

~2006

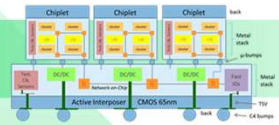
~2016

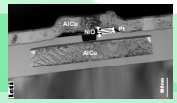
~2026…

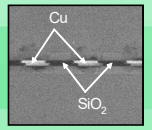
LETI'S TECHNOLOGIES TOWARD HETEROGENEOUS PROCESSORS

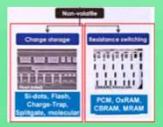
Co-design, co-emulation, co-simulation with use cases

- Advanced architectures
- Advanced CMOS
- Photonic
- Parallel 3D
- Sequential 3D
- New memory technologies
- Neuromorphic



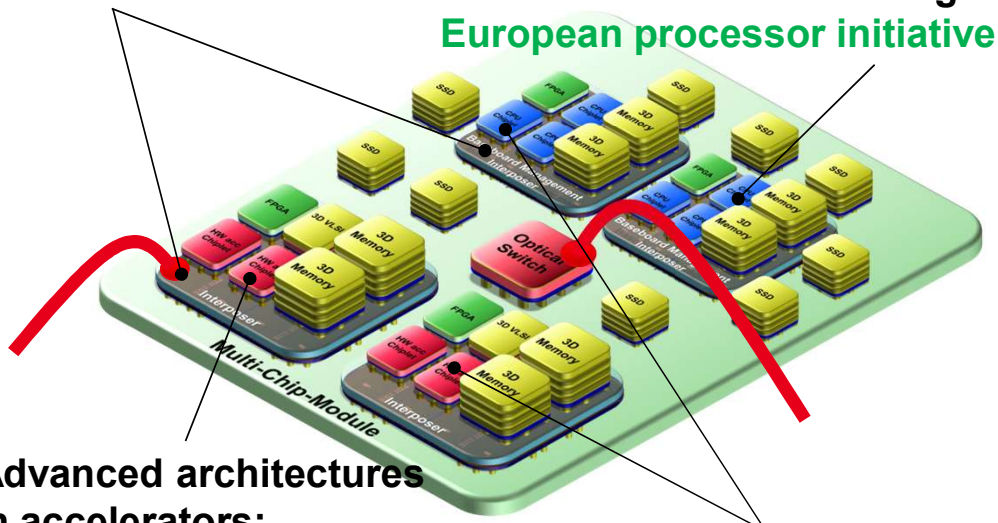






1 - Integration with silicon interposer:
active or photonic

3- Processor design:
European processor initiative

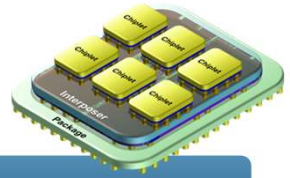


2- Advanced architectures with accelerators:
In-memory computing

Nano-technologies

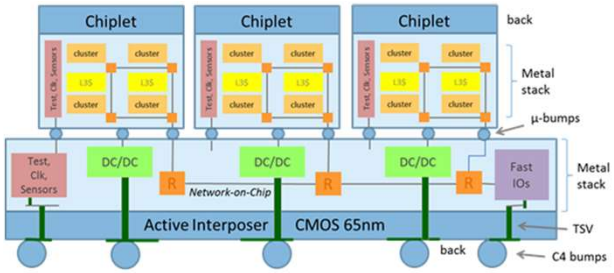
ACTIVE INTERPOSER FROM LETI

Symposium'2016
3DIC'2015
ISVLSI'2015



➡ 96 cores compute fabric with 6 chiplets stacked on an active interposer

System architecture



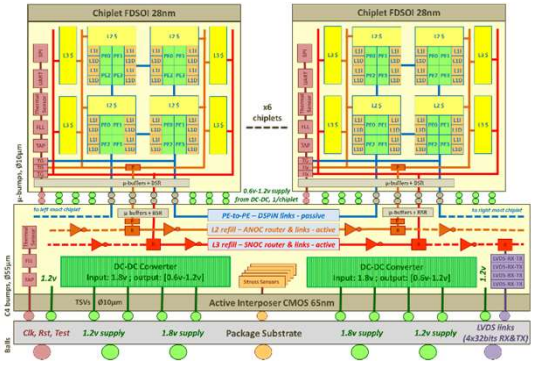
Cache Coherent Compute Fabric with:

- *96 cores (MIPS32),*
- *3 levels of caches,*
- *integrated power management*

Performance targets

- 100 GOPS
- 10 GOPS/Watt
- 25 Watts total

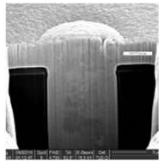
Design

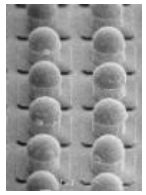


Heterogeneous 3D partitioning with:

- *28nm FDSOI chiplets (x6)*
  - *Low power compute fabric*
  - *Wide voltage range (0.6V – 1.2V)*
  - *Body biasing for logic boost & leakage ctrl*
- *65nm active interposer*
  - *Power unit (Switched Cap DC-DC conv.)*
  - *Interconnect (Network-on-Chip)*
  - *Test, clocking, thermal sensors, etc*

Technology





TSV
Ø 10µm
Height 100µm

µ-bumps
Ø 10 µm
Pitch 20 µm

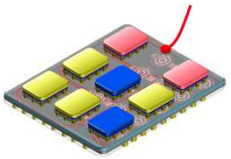
Application

Ongoing validation:

- *To execute full Linux onto 96 cores*

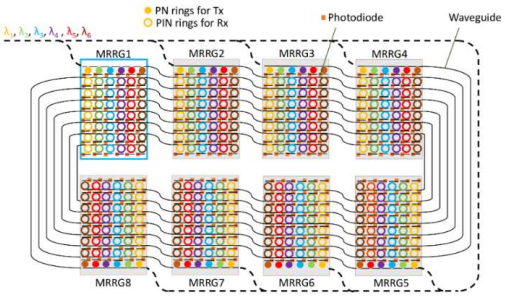
PHOTONIC INTERPOSER FROM LETI

NOCS'2015
ISSCC'2018



➡ Optical network-in-package to interconnect microprocessors and memories

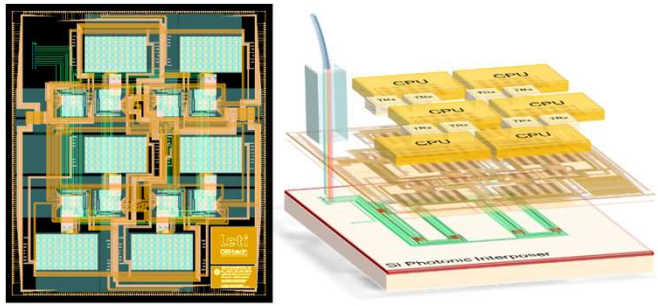
System Architecture



Optical Network-on-Chip topology and power optimization:

- *8-node optical NoC*
- *576 Gbit/s aggregated bandwidth*
- *384 micro-ring resonators*
- *~10 ns electro-optical latency*

Design & integration



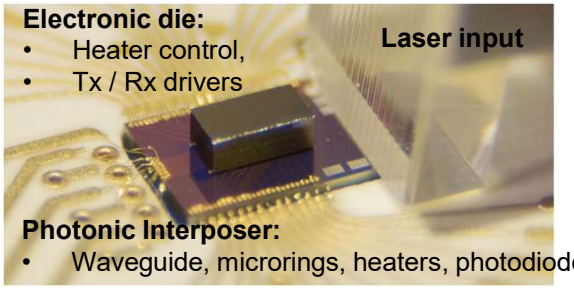
Reference design with 6 chiplets, 8 transceivers:

- *96-core cache-coherent processor*
- *Advanced 3D stack*

Target demonstrator for 2021

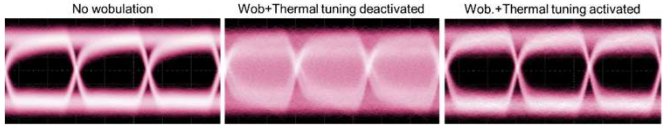
Silicon Photonics

Y. Thonnart & al. ISSCC'2018



Thermal tuning challenges demonstrated on silicon:

- *1Tbps/mm² bandwidth density*
- *Tight technology integration of E/O ring modulators within a 3D stack*
- *Integrated thermal tuning robust to compute fabric heating*

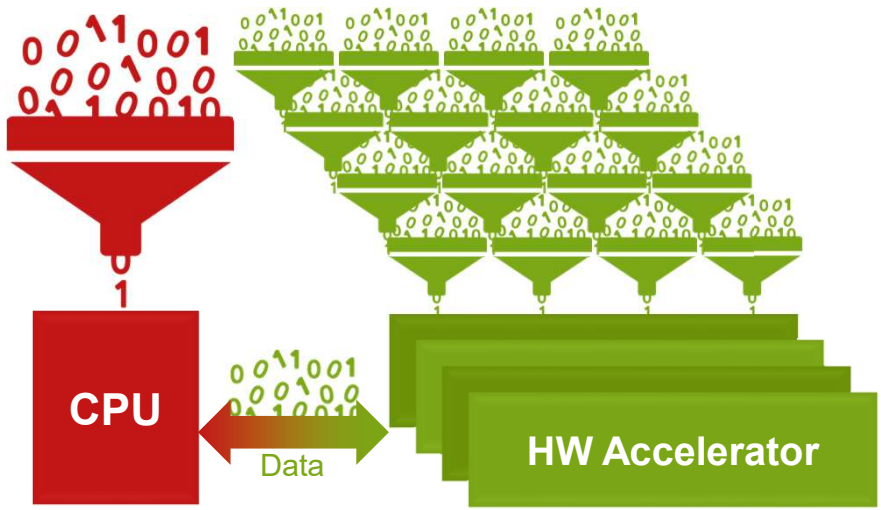


IN-MEMORY-COMPUTING

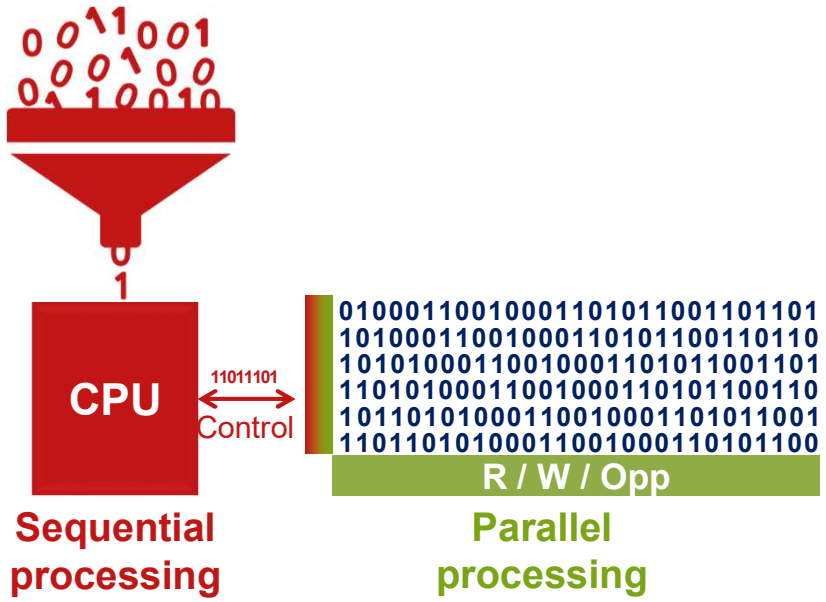
* Preliminary results for kernels of algorithms from Leti's exploration and simulation platform

➡ Expected* gains: ~10x for energy reduction; ~100x on execution time

- **Heterogeneous compute**
  - Complex use of 2 programming languages
  - Data movement power consumption



- **In-memory computing**
  - Single SW environment with compiler for memory operations
  - Drastic reduction of data movement



LETI IN THE HEART OF THE EUROPEAN EXASCALE EFFORT

European Processor Initiative

2018-2021

Processor design

MONT-BLANC 2020

2017-2020

IP design

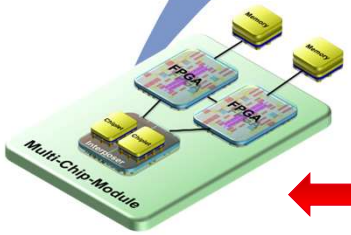
ExaNoDe

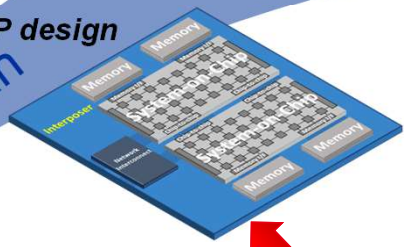
2015-2019

Core technologies

Exascale Effort

European





Novel IPs

3D Integration

23 partners to develop microprocessors for future supercomputers

Advanced Architecture & Designs

Novel Architectures (In-memory-Computing, Neuro)

Novel Integration technologies (Photonics)

EuroHPC Joint Undertaking

2019-2026

Supercomputing Infrastructure research & innovation actions

25 founding members

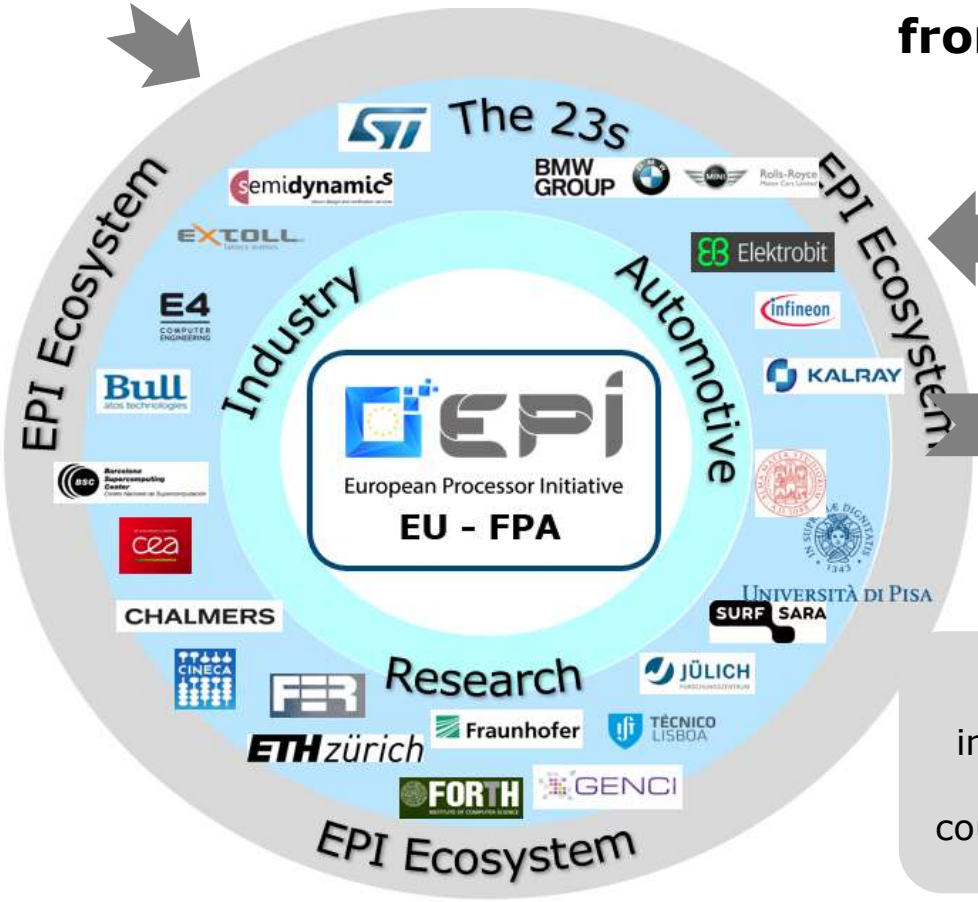
EuroHPC: a new legal and funding entity for deploying in Europe a world-class supercomputing infrastructure

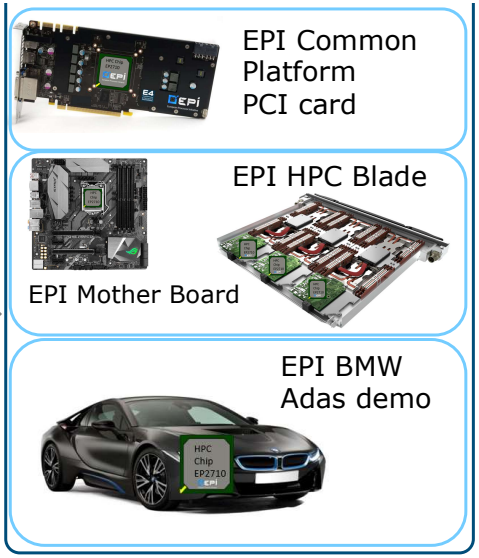
https://eurohpc-ju.europa.eu/

The European Processor Initiative (EPI)

MONT-BLANC
EUROPEAN APPROACH TOWARDS ENERGY EFFICIENT HIGH PERFORMANCE

- **23 partners, from research to industry from consortium to EU high-tech fabless**

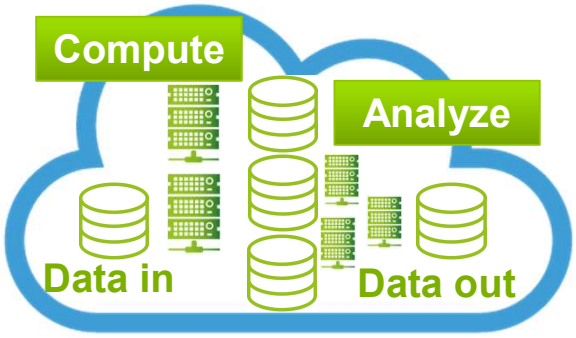




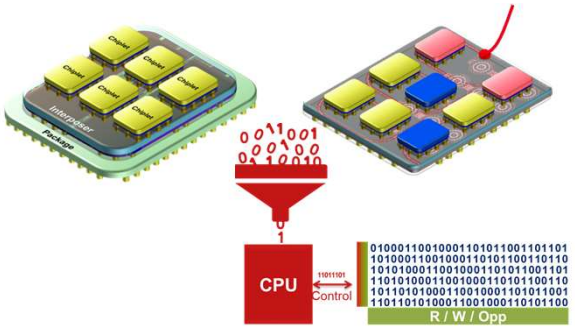
Fabless company industrial hand of EPI incorporated by a couple of EPI members

CONCLUSION

- **A major evolution of high-performance processor architecture is on the way to cope with data deluge and energy efficiency**



- **Leti develops and demonstrates core technologies to enable heterogeneous high-performance processors:**
  - Advanced integration with **active interposer** and **photonic interposer**
  - Disruptive technologies with **In-Memory-Computing**



- **CEA is a major player in the European Processor Initiative to restore processor design in Europe**

European Processor Initiative

Thank you for your attention

Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
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