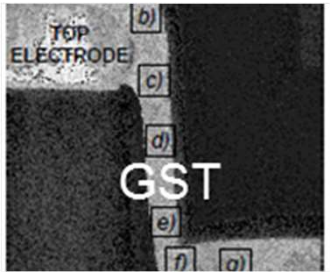
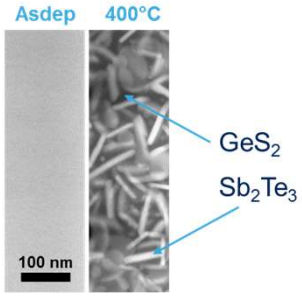
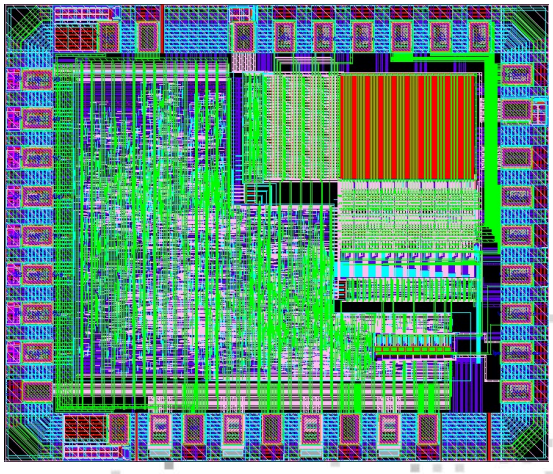
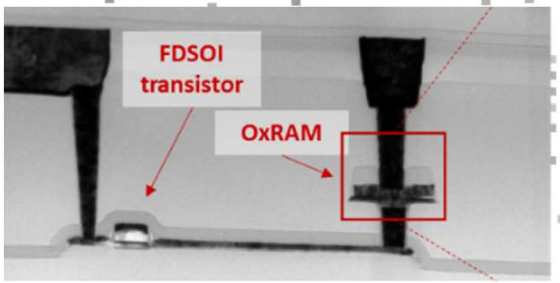








EMERGING NON-VOLATILE MEMORIES FOR COMPUTING

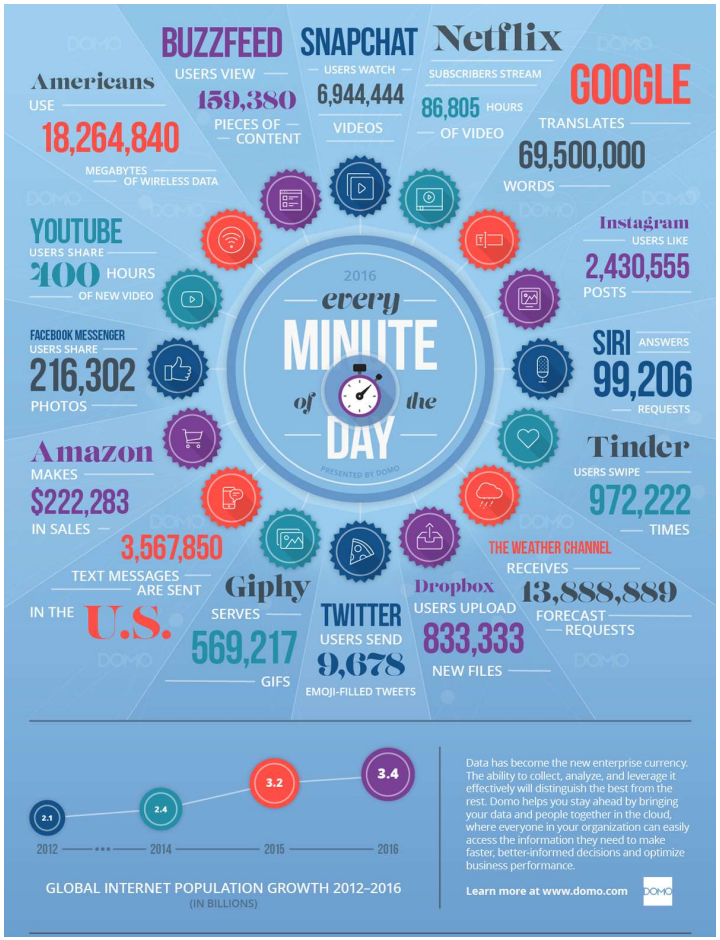
Leti Devices Workshop | Marie-Claire Cyrille| Dec 2nd, 2018, Nikko Hotel, San Francisco

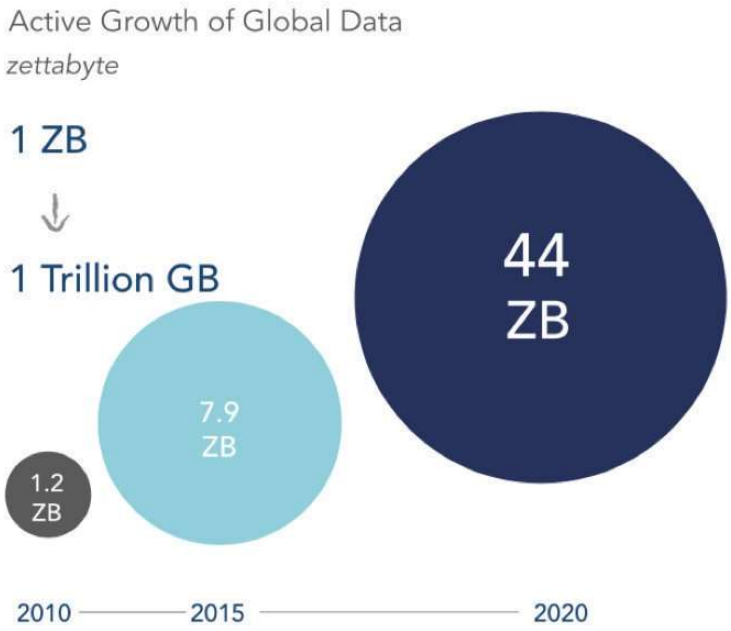
NON-VOLATILE MEMORY (NVM) OPPORTUNITY

No one will need more than 637Kb of memory for a personal computer

— Bill Gates —

AZ QUOTES



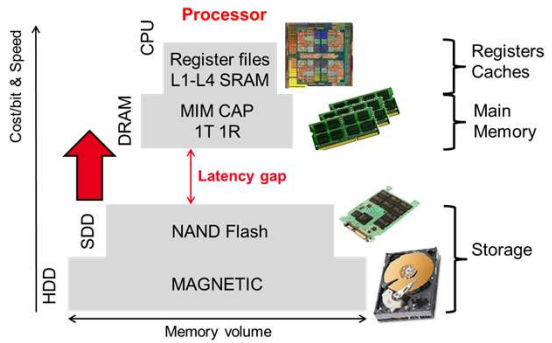


Data generated every minute of the day
Source: Domo. com

NON-VOLATILE MEMORY (NVM) OPPORTUNITY

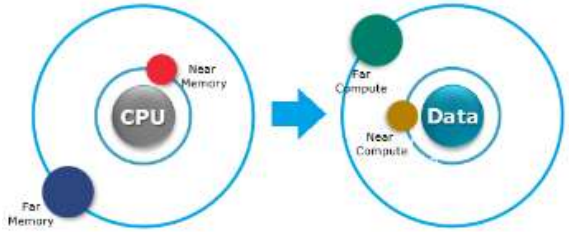
- **Low / no energy consumption**
  - Server cost due to power
  - Battery replacement cost (IoT / VR/AR)

➔ **Higher integration of NVM within logic**



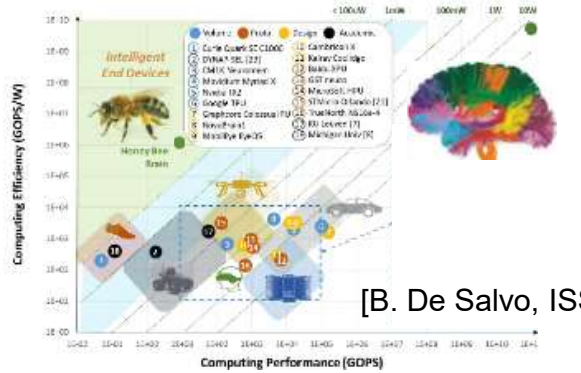
- **Data-centric computer architecture**
  - Data movement constrained
  - In-memory processing / Distributed processing
  - Machine learning / real time video analytics

➔ **Higher integration of logic within NVM**



- **"Brain targeting"**
  - Artificial spiking neural network / neuromorphic
  - Non-Von Neumann architecture

➔ **No logic / NVM frontier**



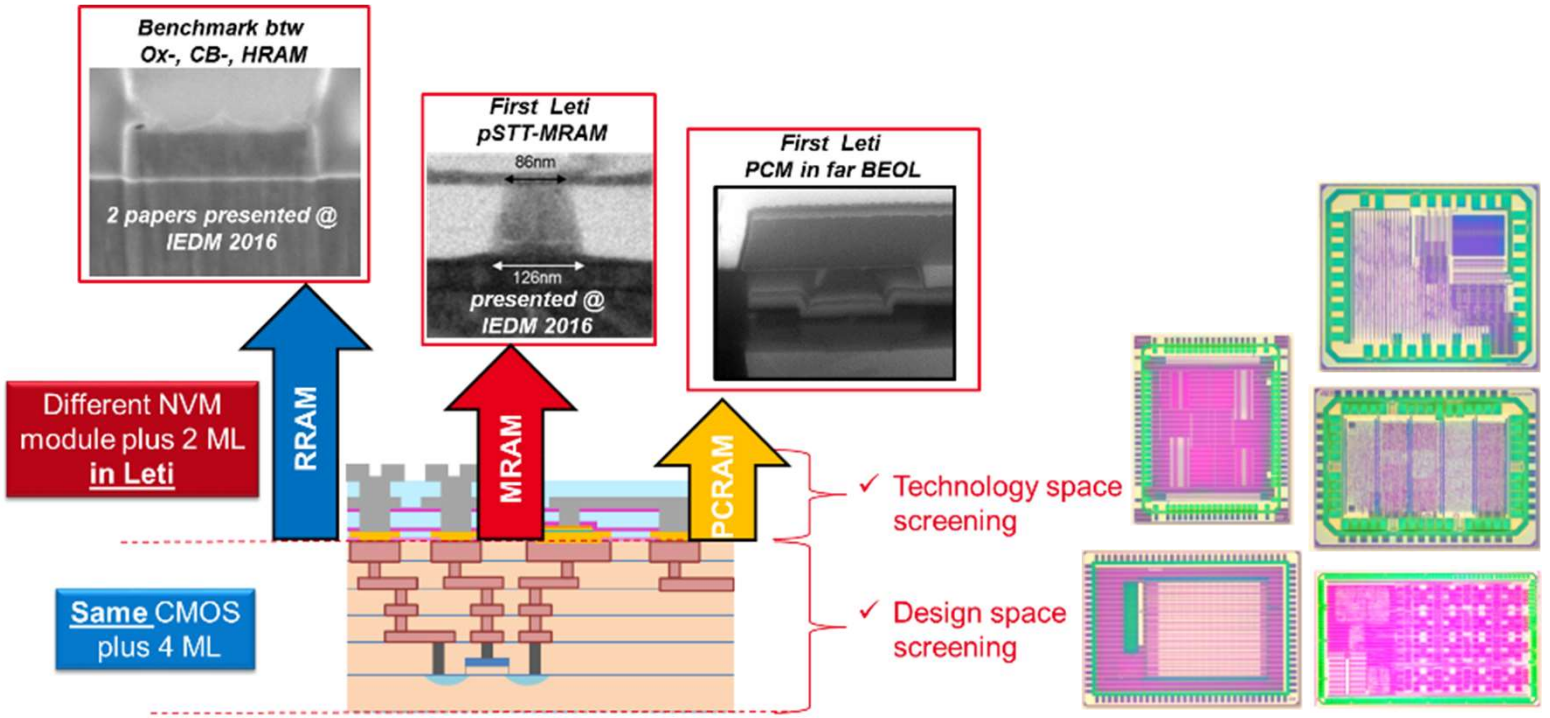
[B. De Salvo, ISSCC 2018]

MEMORY ADVANCED DEMONSTRATOR (MAD) FOR TECHNOLOGY EXPLORATION

- MPW Shuttle (today in 200mm; twice a year; next start may 2019)

→ From single cell to matrix and complex designs while continuing integration of new materials

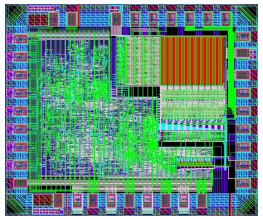
→ **In 2019: availability MAD300 – 300mm** to access more efficient CMOS (28nm FDSOI)



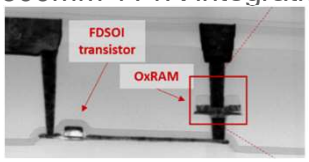
2017 - 2018 RESULTS OF LETI'S MAIN EXPERTISE FOR NVM

A wide toolbox for customized research & benchmark between different BEOL NVM technologies

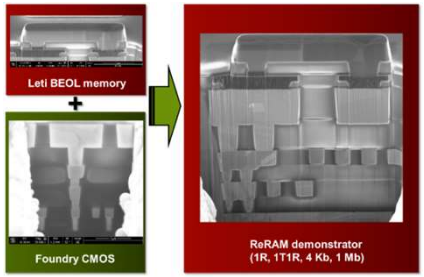
Dedicated NVM design

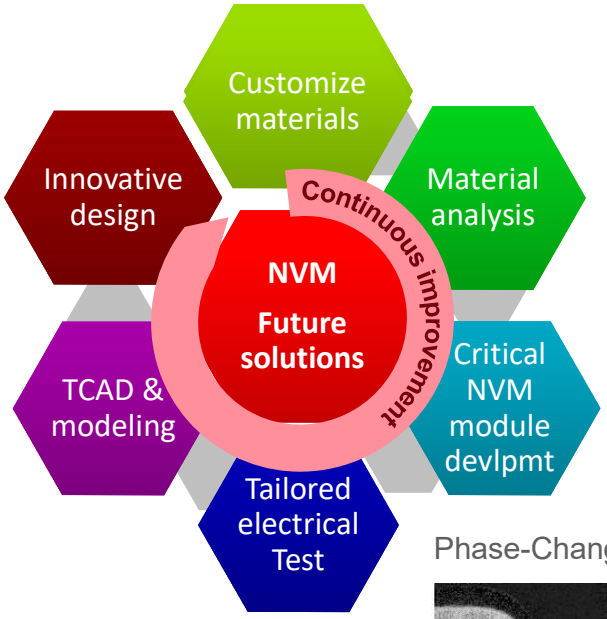


300mm 1T1R integration

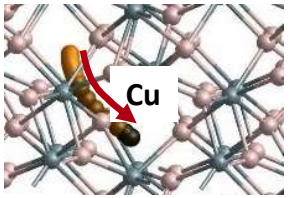


Memory Advanced Demonstrator (MAD shuttle -200mm)



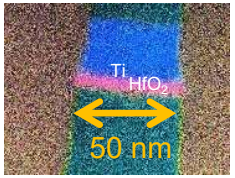


Ab-initio simulation



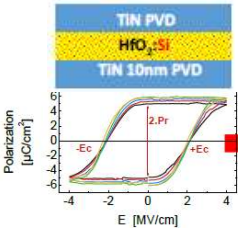
TED2018
TED, JAP2017

Resistive-RAM
OxRAM & CBRAM



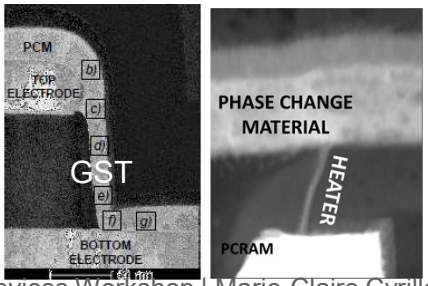
VLSI 2018
IMW2018
EDL2018

FeRAM



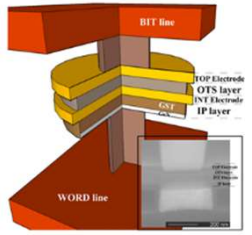
SSDM 2018

Phase-Change Memories



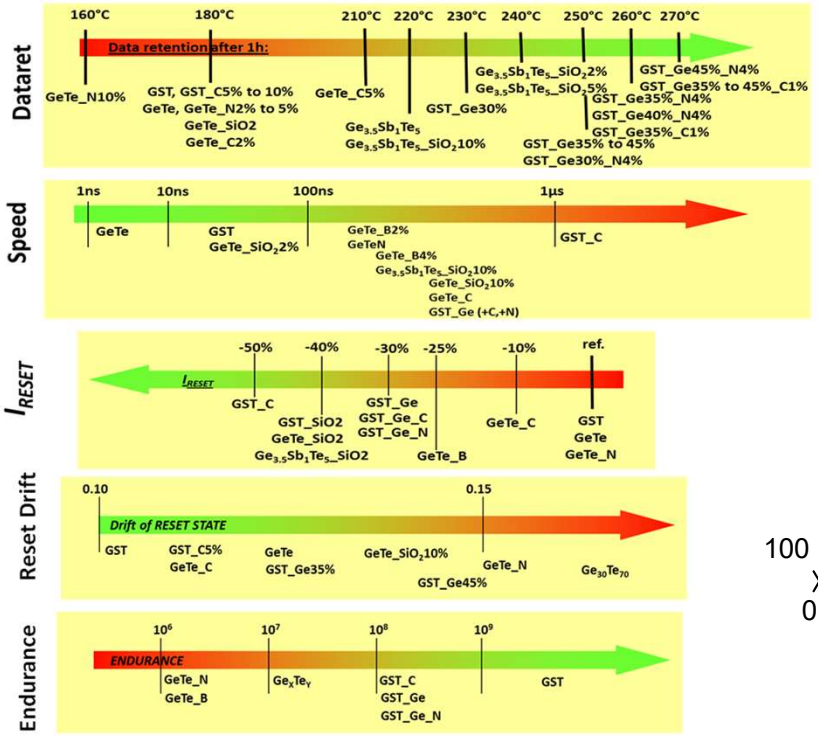
IMW 2018
NVMTS2018
NVMTS2017
SSDM2017

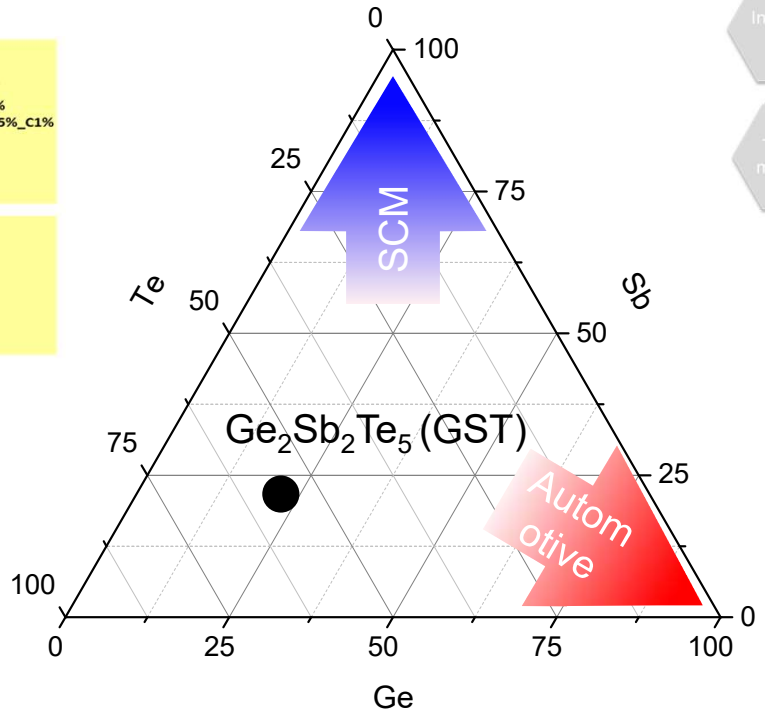
OTS based Selectors

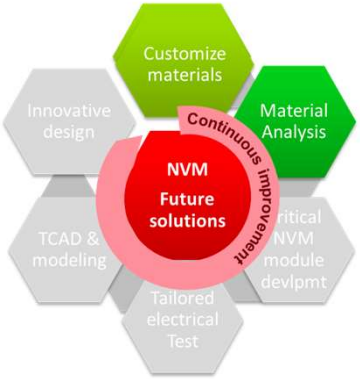


IEDM2018
IRPS 2018
IMW 2018
VLSI 2017

PHASE-CHANGE MATERIALS ENGINEERING AT LETI (1/3)



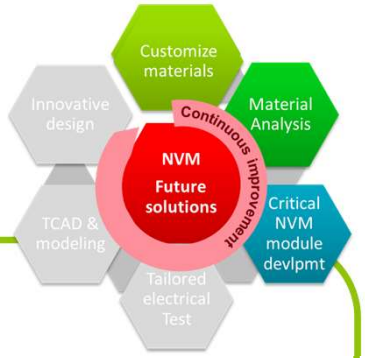


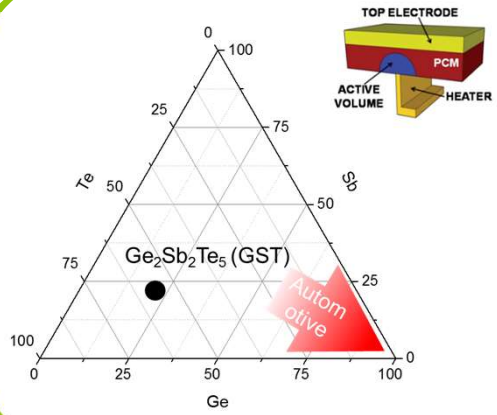


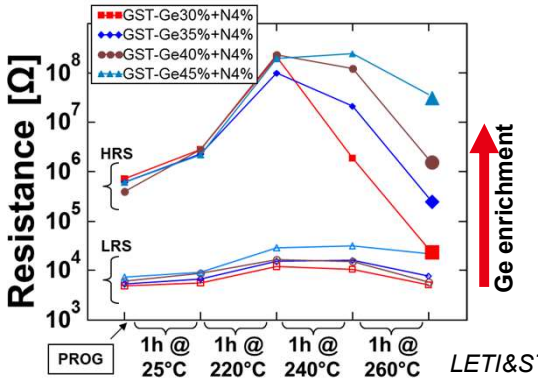
VLSI 2017, 2015
IMW 2018, 2016
NVMTS 2018, 2017, 2016
SSDM2017, 2015
CIMTEC 2016,2014
ECS 2017,2016, 2015
ePCOS 2017, 2015,2014
MRS 2017, 2015, 2014

- Ge-rich is compliant with JEDEC standards and it guarantees data preservation in automotive environment
- Sb-rich alloy for high-endurance, high-speed SCM applications

PHASE-CHANGE MATERIALS ENGINEERING AT LETI (2/3)







LETI&STM, IEDM 2013 & VLSI 2015

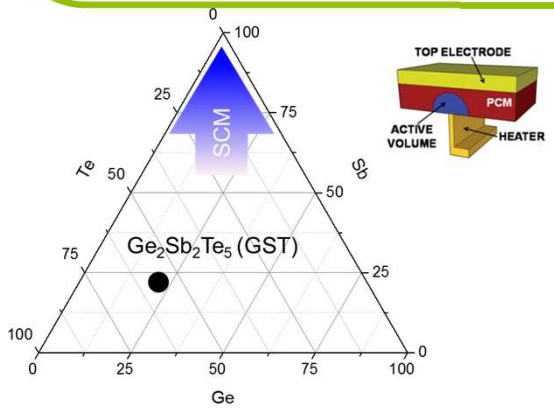
IEDM18 Session 18.4

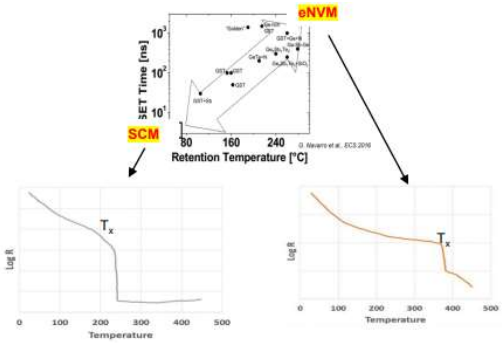
Truly Innovative 28nm FDSOI Technology for Automotive Micro-Controller Applications embedding 16MB Phase Change Memory

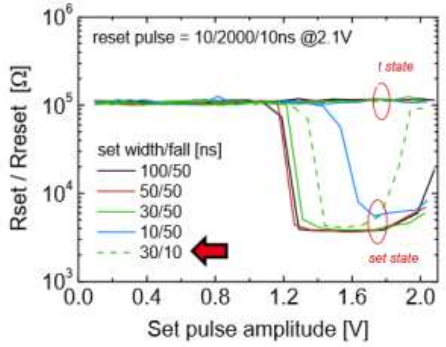
F.ARNAUD[1], P.ZULIANI[2], J.P.REYNARD[1], A. GANDOLFO[2], F.DISEGNI[2], P.MATTAVELLI[2], E.GOMIERO[2], G.SAMANNI[2], C.JAHAN[3], R.BERTHELON[1], O.WEBER[3], E.RICHARD[1], V.BARRAL[3], A.VILLARET[1], S.KOHLER[1], J.C.GRENIER[1], R.RANICA[1], C.GALLON[1], A.SOUHAITE[3], D.RISTOIU[1], L.FAVENNEC[1], V.CAUBET[1], S.DELMEDICO[1], N.CHERAULT[1], R.BENEYTON[1], S.CHOUTEAU[1], P.O.SASSOULAS[1], A.VERNHET[1], Y.LE FRIEC[1], F.DOMENGIE[1], L.SCOTTI[2], D.PACELLI[2], J.L.OGIER[1], F.BOUCARD[1], S.LAGRASTA[1], D.BENOIT[1], L.CLEMENT[1], P.BOIVIN[4], P.FERREIRA[1], R.ANNUNZIATA[2], P.CAPPELLETTI[2]

[1]STMICROELECTRONICS, [3]CEA-LETI, 850 rue Jean Monnet 38926 Crolles, France
[2]STMICROELECTRONICS via Camillo Olivetti 2, Agrate Brianza, Italy
[4]STMICROELECTRONICS, zone industrielle, 190 avenue Coq, 13106 Rousset, France

life.augmented



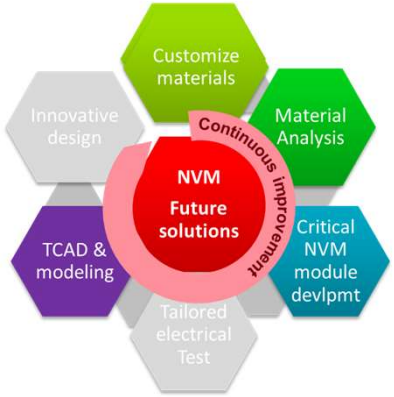




APPLIED MATERIALS® make possible

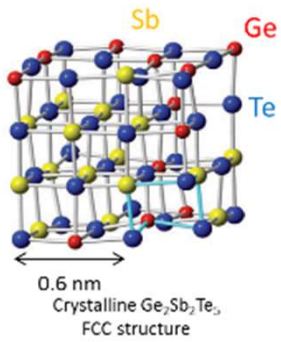
JDP LETI AMAT 2015, 2017
Flash Memory Summit 2018

PHASE-CHANGE MATERIALS ENGINEERING AT LETI (3/3)

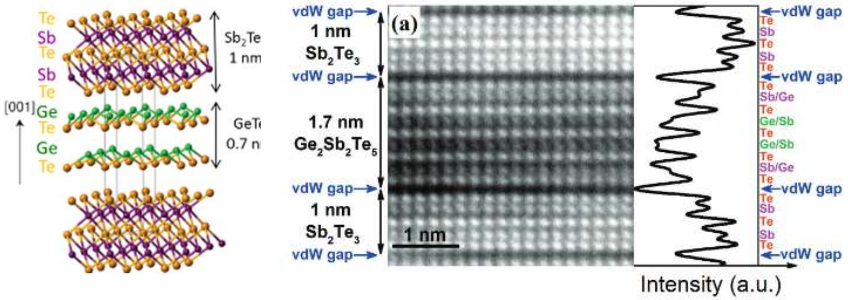


Next Material challenges

PCM alloy



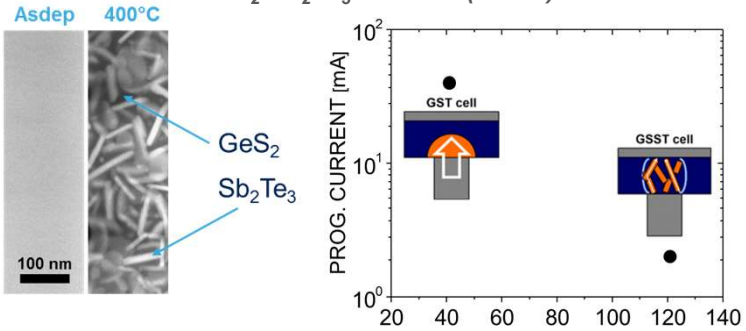
PCM Super Lattices@Leti



P Kowalczyk et al; Small 2018, 14, 1704514

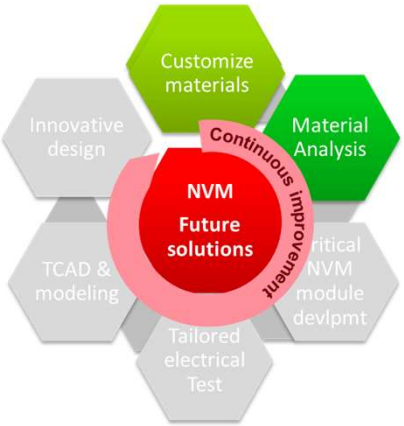
PCM Intergranular@Leti

GeS_2/Sb_2Te_3 material (GSST)

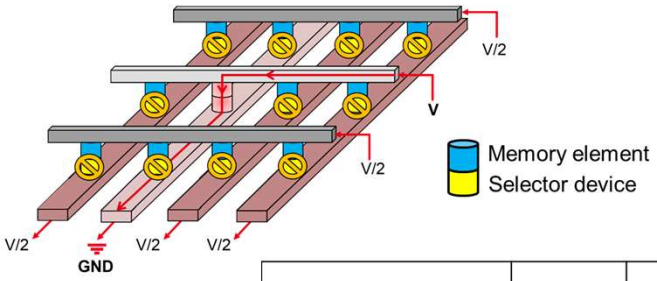


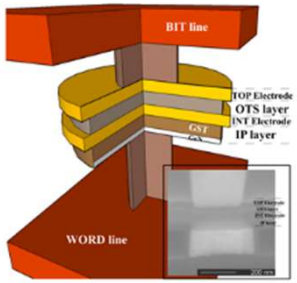
IMW 2018
NVMTS2018
NVMTS2017
SSDM2017

MATERIAL ENGINEERING FOR SELECTOR APPLICATIONS: AS FREE OVONIC THRESHOLD SWITCHING MATERIALS

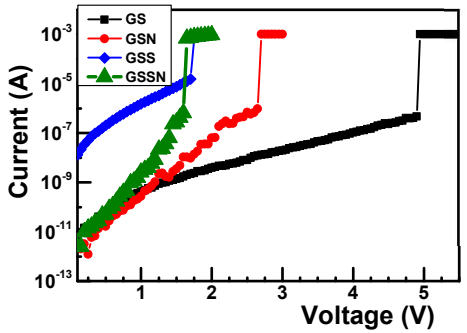


Need for a reliable selector to reduce sneak paths (reading fails and cell to cell disturbance)



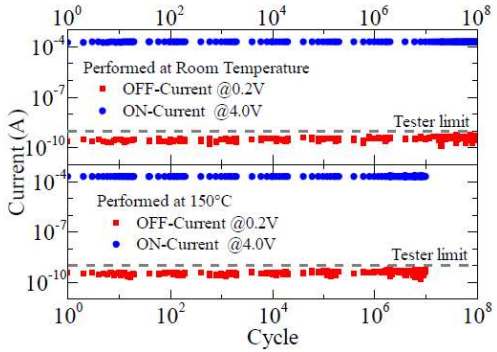


VLSI 2017



	Doped chalco. [1]	AsTeGeSiN [2]	SiTe [3]	GeSe [4]	AsTeGeSiSe [5]	LETI GSSN
Integration or device annealing Temperature	180°C 2h	500°C 30min	400°C 30 min	205°C	350°C 30min	400°C 30min
Leakage current @Vth/2 (A)	10^{-7}	10^{-7}	10^{-7}	10^{-7}	10^{-8}	10^{-10}
Endurance	10^{9}	10^{8}	$>10^{8}$	10^{8}	$>10^{10}$	$>10^{8}$

IEDM 2018
IRPS 2018
IMW 2018
IMW2017

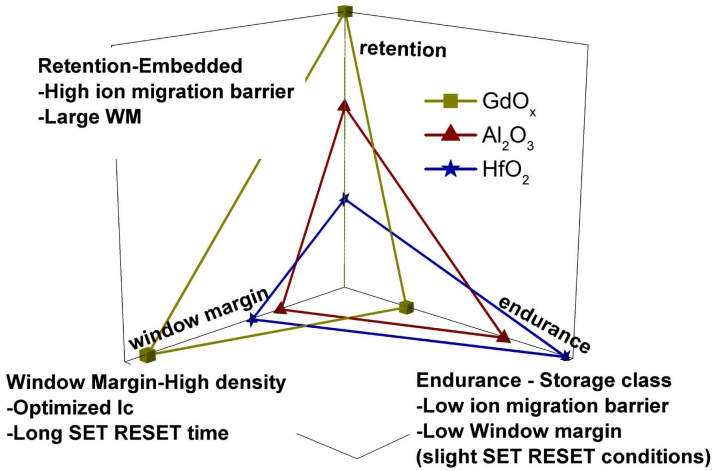


Optimized Reading Window for Crossbar Arrays Thanks to Ge-Se-Sb-N-based OTS Selectors

A. Verdy, M. Bernard, J. Garrione, G. Bourgeois, M. C. Cyrille, E. Nolot, N. Castellani, P. Noé, C. Socquet-Clerc, T. Magis, G. Sassine, G. Molas, G. Navarro and E. Nowak
CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France

IEDM18 Session 37.4

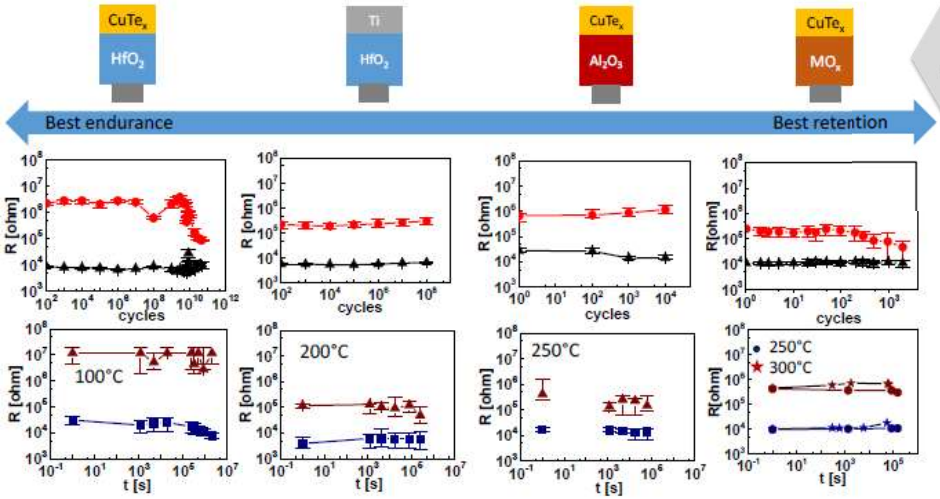
RRAM BENCHMARK FOR TRADE-OFF UNDERSTANDING

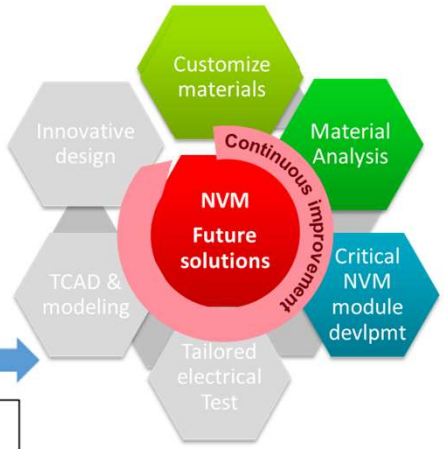


Retention-Embedded
-High ion migration barrier
-Large WM

Window Margin-High density
-Optimized Ic
-Long SET RESET time

Endurance - Storage class
-Low ion migration barrier
-Low Window margin
(slight SET RESET conditions)





VLSI 2018
IMW2018
EDL2018
IRPS2018

Towards circuit implementation

- **Via collaborations**
- **MAD shuttle**

LETI AND CMP ANNOUNCE WORLD'S FIRST MULTI-PROJECT WAFER SERVICE WITH INTEGRATED SILICON OXRAM

Weebitnano The Emerging Memory

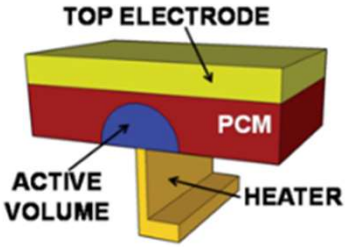
Weebit Nano and Leti extend their agreement to fast track commercialisation

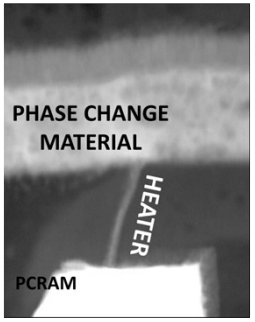
16 May 2018 – Weebit Nano (ASX: WBT), the Israel-based semiconductor company seeking to develop and commercialise the next generation of memory technology, today announced an extension of the agreement with its partner Leti, the French research institute recognised as a global leader in the field of micro-electronics, to further develop and optimise Weebit's ReRAM memory technology.

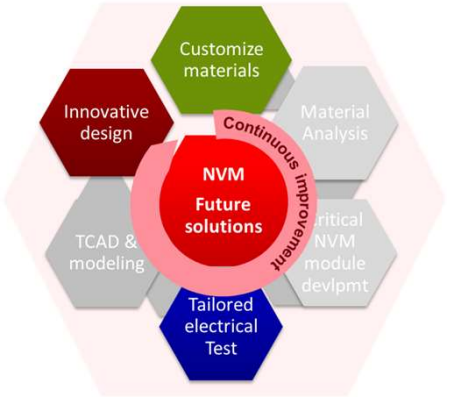
ETH zürich · Universität Zürich · C2N · Université Paris Sud · Stanford University · Université de Nantes · Université de Toulon

PCRAM: TOWARDS NEUROMORPHIC APPLICATIONS

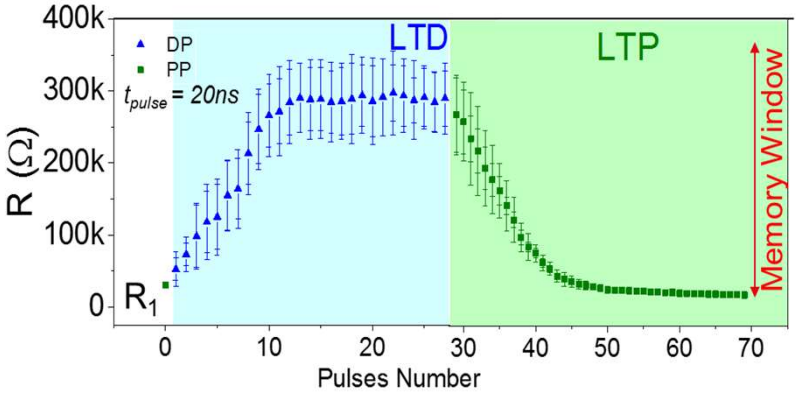
PCM as artificial synapse

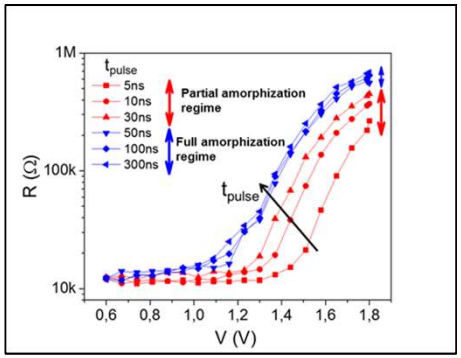






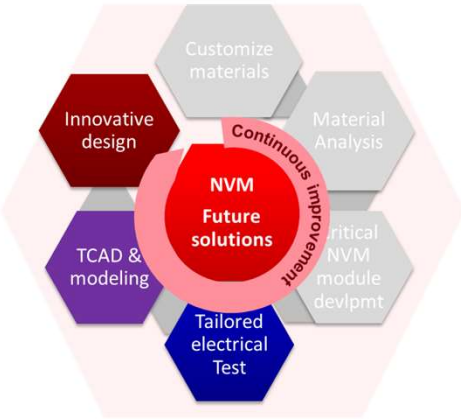
S La Barbera, Advanced Electronic Materials 2018





- **Programming strategy based on uniform short pulse sequence (t_{pulse}<50ns) to enable gradual depression (non-stationary regime)**
- **Amorphous region does not cover the entire area of the bottom electrode (i.e. the heater)**

RERAM: TOWARDS NEUROMORPHIC APPLICATIONS



In-depth Characterization of Resistive Memory-Based Ternary Content Addressable Memories

D. R. B. Ly[1], B. Giraud[1], J-P Noel[1], A. Grossi[1], N. Castellani[1], G. Sassine[1], J-F Nodin[1], G. Molas[1], C. Fenouillet-Beranger[1], G. Indiveri[2], E. Nowak[1] and E. Vianello[1]
[1]Univ. Grenoble Alpes, CEA, LETI, 38000 Grenoble, France, email: denys.ly@cea.fr ; elisa.vianello@cea.fr
[2] Institute of Neuroinformatics, University of Zurich and ETH Zurich

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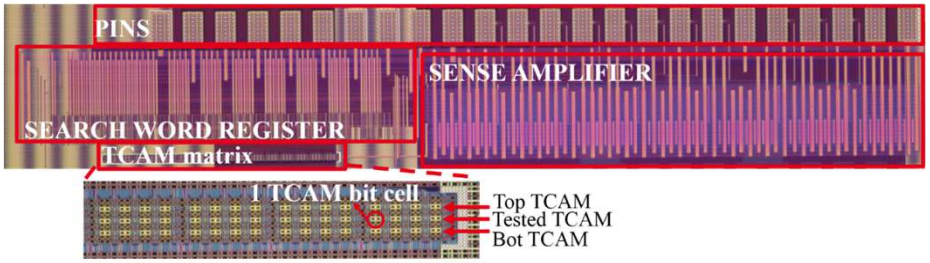
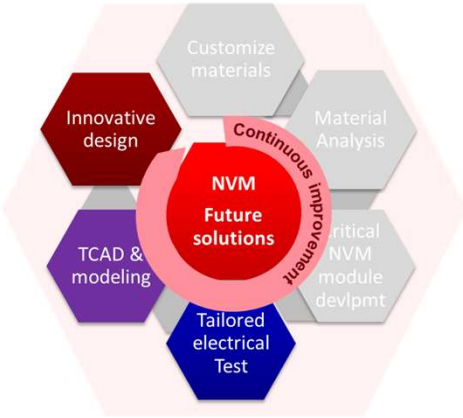


	[6] - 2T2R	[7] – 2.5T1R	[8] – 5T2R	[9] – 4T2R	[10] – 3T1R	This Work – 2T2R
TCAM circuit	8×2048×64 bit 90 nm CMOS	64×256 bit 90 nm CMOS	128×64 bit 90 nm CMOS	128×32 bit 180 nm CMOS	2×64×64 bit 90 nm CMOS	3×128 bit 130 nm CMOS
Search Latency	1.9 ns @ 0.75 V	1 ns @ 0.45 V	1.9 ns @ 0.75 V	1.2 ns @ 1.4 V	0.96 ns @ 0.48 V	90 ns @ 0.6 V
Measured results	Impact of *Search Voltage* on **Search Latency**					• **Search Latency** • **Match/mismatch search margin** • **Search/Read endurance (>10^6)** • **Programming endurance (> 10^6)**

- **MAD 200 Shuttle**
- **Fabrication of RRAM based TCAM circuits**
- **HfO_2 based OXRAMs**
- **Trade off between search latency and reliability (HRS programming conditions)**

RERAM: TOWARDS NEUROMORPHIC APPLICATIONS



In-Memory and Error-Immune Differential RRAM Implementation of Binarized Deep Neural Networks

IEDM18 Session 20.6

M. Bocquet[1*], T. Hirztlin[2*], J.-O. Klein[2], E. Nowak[3], E. Vianello[3], J.-M. Portal[1] and D. Querlioz[2]
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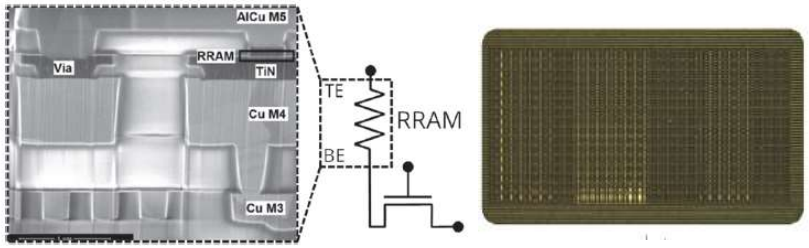
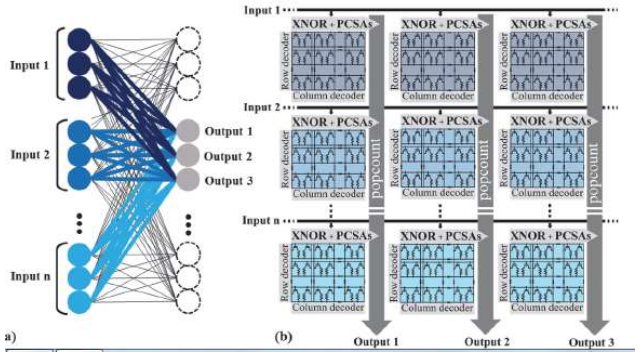
- MAD200 Shuttle
- HfO_2-based RRAM array with differential memory bitcells and sensing scheme for in-memory computing.
- Possible implementation of Binarized Neural networks : collection of Kbit arrays w CMOS digital circuitry
- Large power reduction





CONCLUSION: @LETI

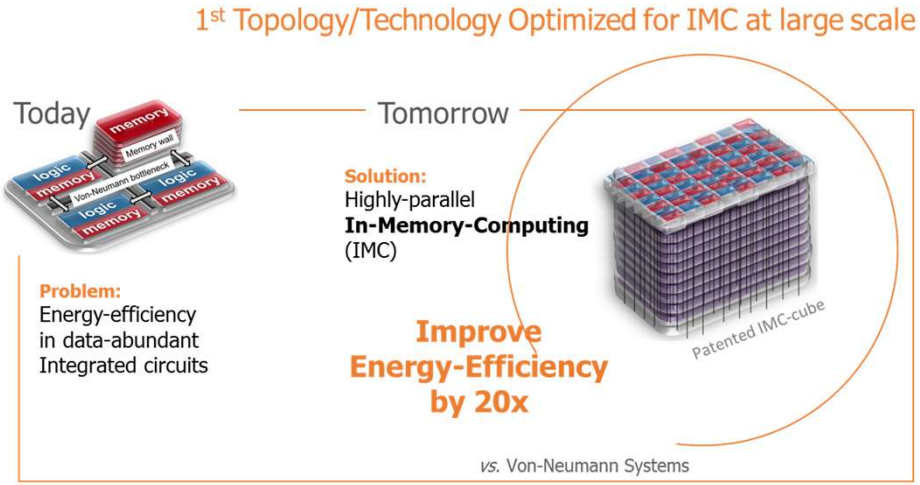
A wide toolbox for customized research and benchmark between different BEOL NVM technologies:

- Competitive experience in material development and exploration for eNVM
- Wafer shuttle platform in 200 & 300mm for material investigation & disruptive circuit development

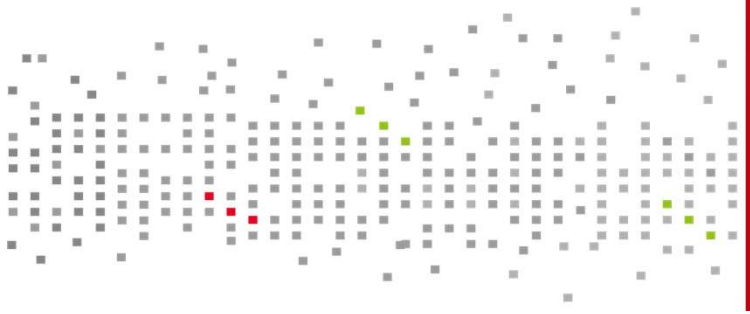
In the near future we will focus on

- New materials (2D materials for PCM, selectors, Mott insulators based RAMs)
- Silicon demonstration of disruptive computing paradigm (Neuromimetic, Machine learning…)

➢ 5-year research program funded by EU exploring In memory computing paradigm



Thank you for your attention



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