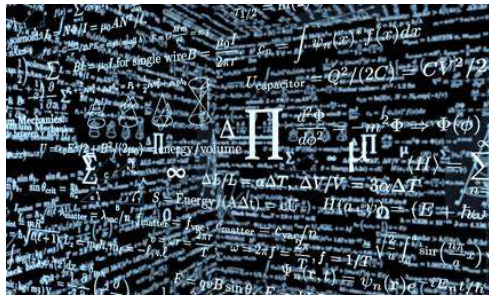


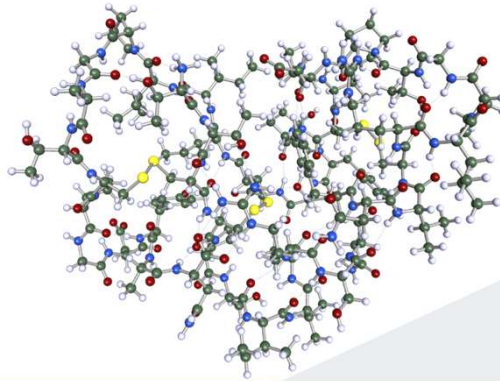
# QUANTUM COMPUTING ON SILICON

Leti Devices Workshop | Maud Vinet | Dec 2nd, 2018, Nikko Hotel, San Francisco

## QUANTUM COMPUTATION PROMISES



**Quantum supremacy**  
50 logical computational qubits/ 50 physical qubits for sampling



**Quantum chemistry for medicine and material developments**  
200 logical qubits



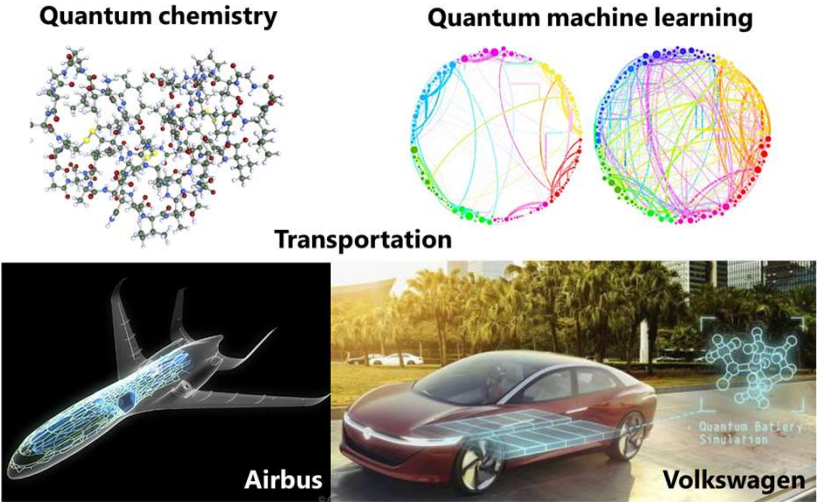
ETH Zurich, Bristol, Usherbrooke, Google...

**Factorizing prime numbers for security, AI, data mining**  
2000 logical qubits





# QUANTUM COMPUTATION NUMBERS



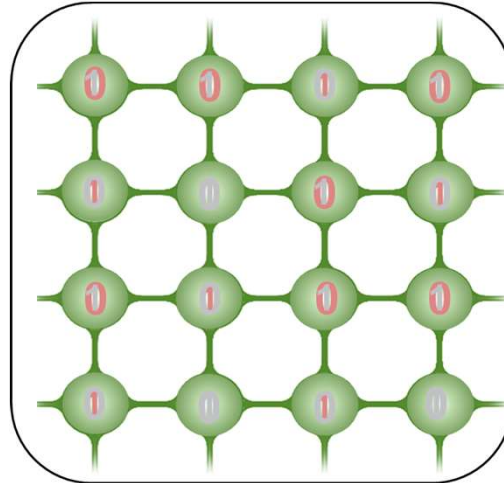
Still improving

**Hundreds of qubits**

**Millions of errorless quantum operations**

# Millions of errorless quantum operations

Quantum Error Correction  
protocols



**1 errorless logical qubit**  
> 1000 physical qubits



**Millions of physical qubits in a 2D array**

## SINGLE QUBIT SCALE FIGURES OF MERIT



### SPEED

Competitive run-time  
quantum calculation



### FIDELITY

Logical qubits better  
than physical qubits

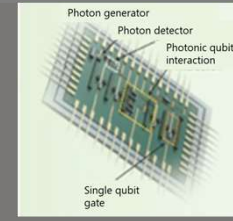
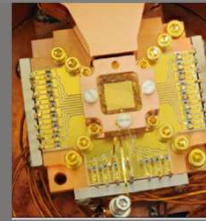
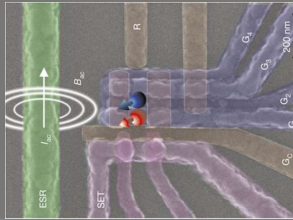
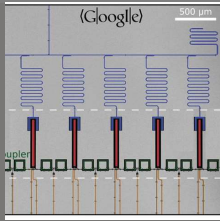


### SIZE

Manageable  
dimensions of the  
quantum circuit



## BENCHMARK AND PLAYERS



### Superconductors

### Silicon spins

### Trapped ions

### Photons

Size

$(100\mu\text{m})^2$

$(100\text{nm})^2$

$(1\text{mm})^2$

1 mm<sup>2</sup>

Fidelity

~99.9%

>98%

99.99%

50% (measurement and generation)  
98% (one and two-qubit gate)

Speed

200 ns

5  $\mu\text{s}$

100  $\mu\text{s}$

1 ms

Number of entangled qubits

17 (claimed 72)

2

20

18

Companies

IBM, Google, Intel, Dwave, Rigetti, QCI...

Intel, HRL, Silicon Quantum Computing

IonQ

Xanadu, Quandela, HP, Tundra systems, PsiQuantum

Leading academic teams

UCSB, Yale, IBM Zurich, CEA, Berkeley, TU Delft, MIT

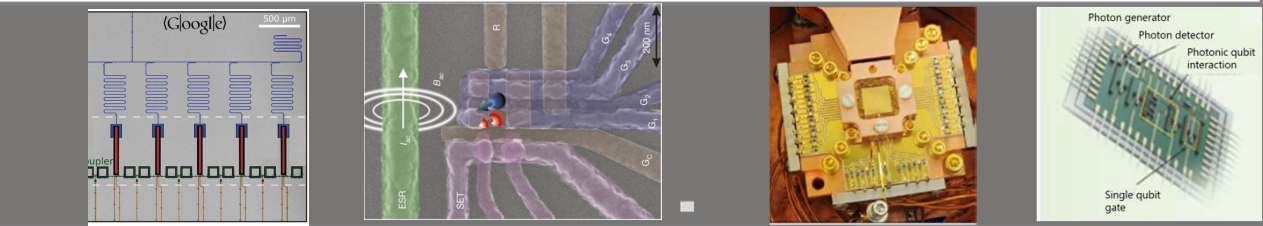
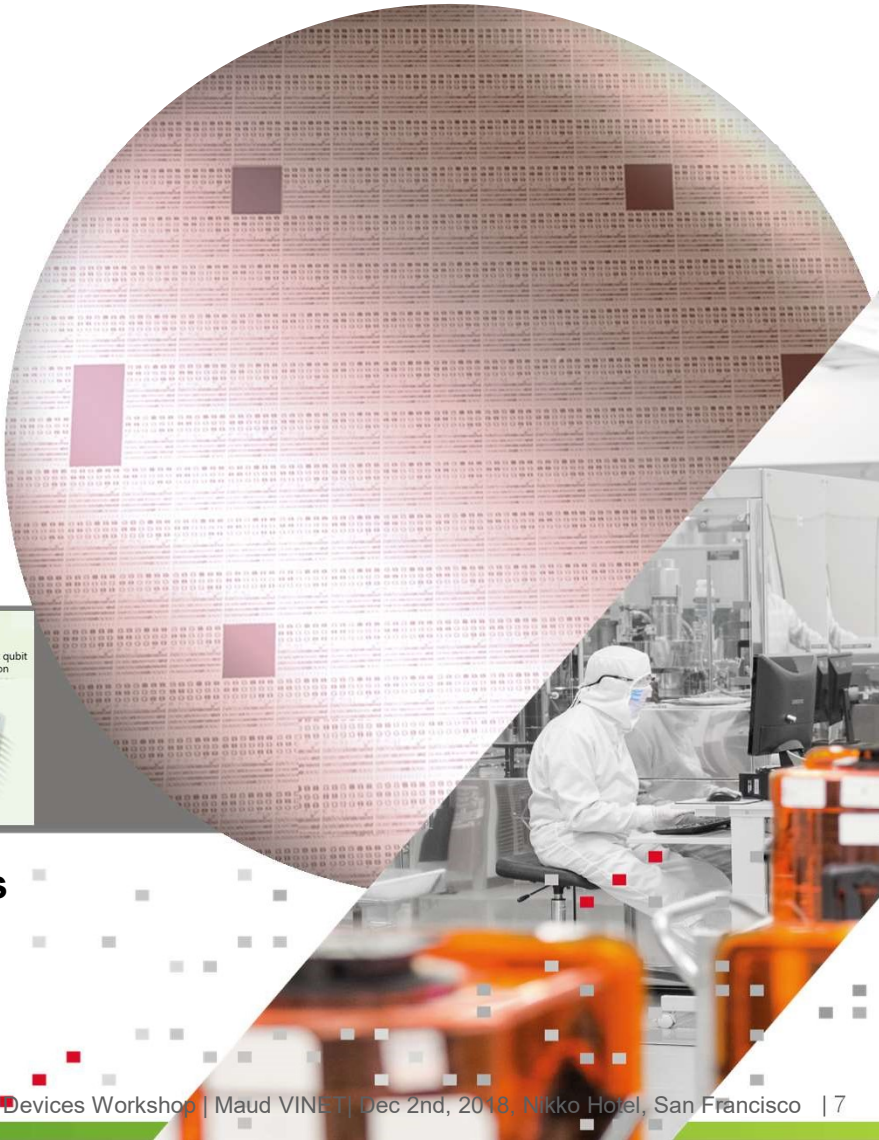
UNSW, CEA-CNRS Grenoble, Tokyo University, TU Delft, Princeton, Sandia, Uwiconsin, NTT

Innsbruck, Oxford, NIST, UMaryland, Sussex, MIT

Oxford University

# MATURITY OF VLSI TECHNOLOGY

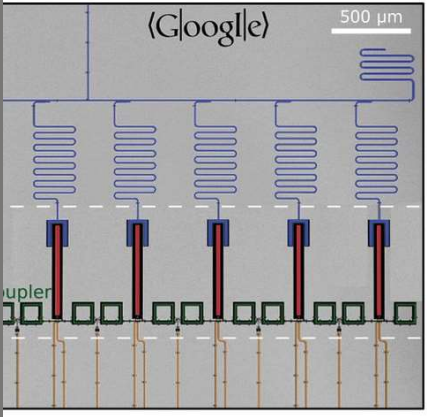
- Integration
- Better control of interfaces
- Better control of thicknesses
- Better control of chemical composition
- Better control of critical dimensions



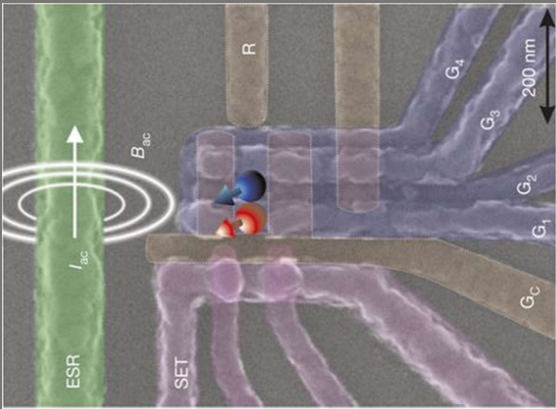
**Superconductors   Semiconductors   Trapped ions   Photons**

**REQUIRED FOR ALL TECHNOLOGICAL PLATFORMS**

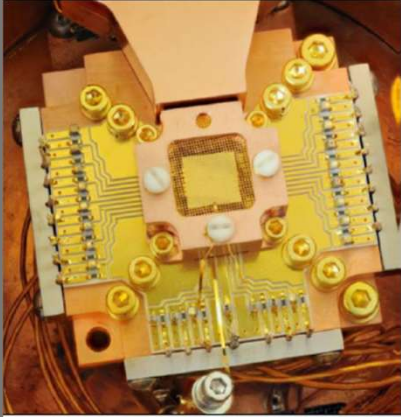
**Superconductors**



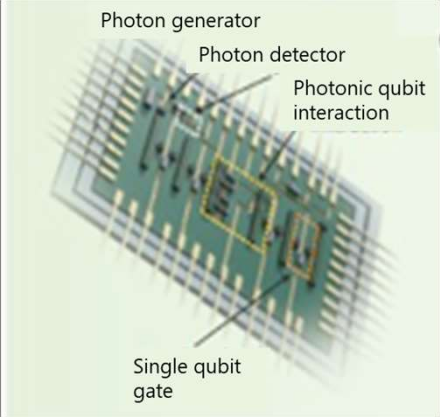
**Silicon spins**



**Trapped ions**



**Photons**



Yield and variability control

Yield and variability control

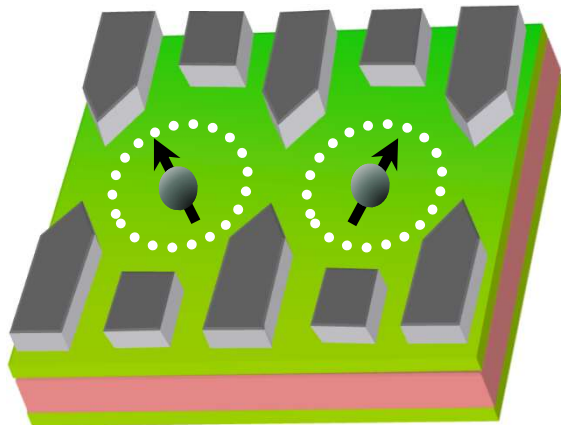
Better interfaces

Integration of all components





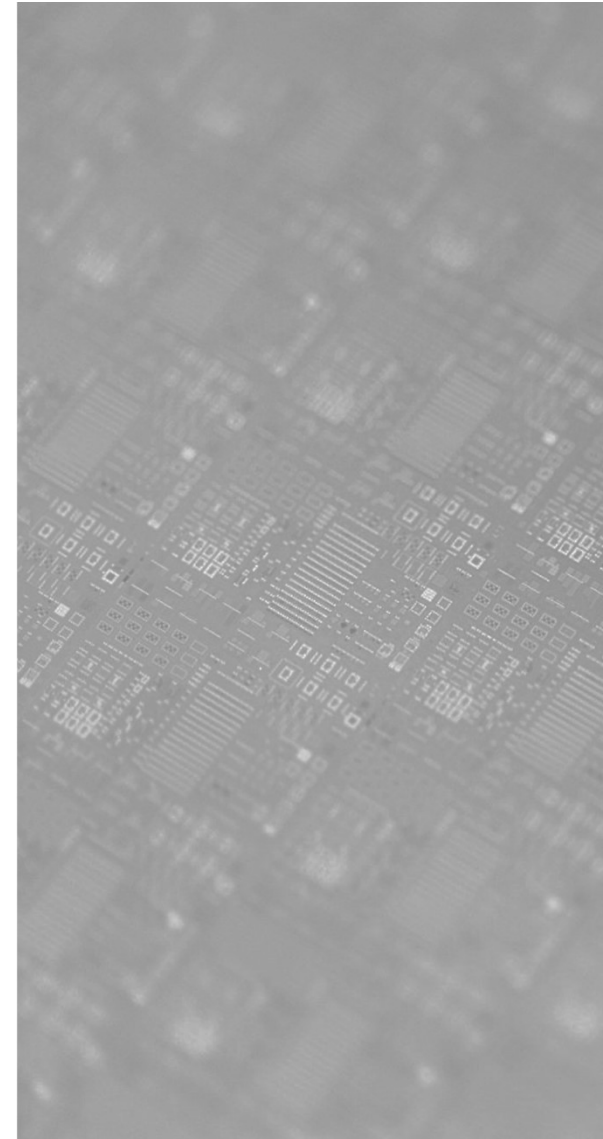
## Spin degree of freedom of an electron



$$0 \rightarrow |\uparrow\rangle$$

$$1 \rightarrow |\downarrow\rangle$$

Gate defined quantum dots



## QUBIT FIGURES OF MERIT



Speed ✓



Fidelity ✓



Size ✓

# Large ensemble of qubits



Variability

Large scale control

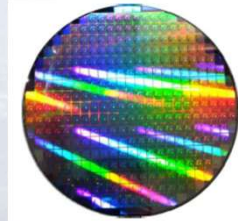


**INAC**  
INSTITUT NANOSCIENCES  
ET CRYOGÉNIE

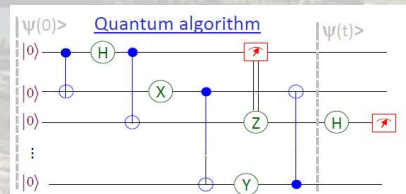


**CMOS Device physics**  
Spin and charge properties  
of Si CMOS devices

**VLSI technology**  
Advanced CMOS integration  
IC design and architecture



**Quantum engineering**  
Coherent control of electron spins in  
semiconductors



**NEEL**  
institut



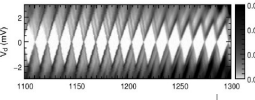
# GRENOBLE LONG STANDING EFFORTS TOWARDS SILICON QUANTUM COMPUTING

Key dates

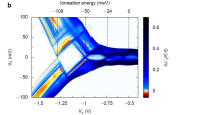
Key technological assets

Key fundings

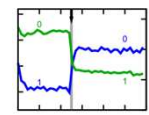
**2007** Control of Si CMOS quantum devices



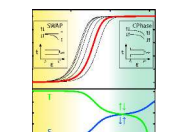
**2010** Spectroscopy of individual dopants in si CMOS nanodevices



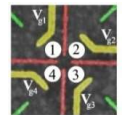
**2011** Control displacement of individual electrons



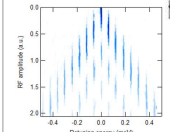
**2011** Fast Cphase protocol for individual electron spins



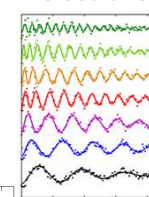
**2012** 2x2 array electron control



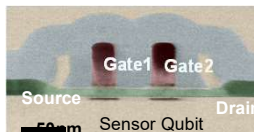
**2013** Coherent control on two dopants



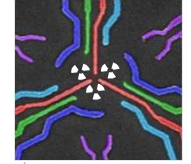
**2015** Symmetric exchange of a spin between 2 electrons



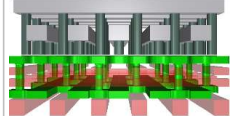
**2016** First CMOS Qubit



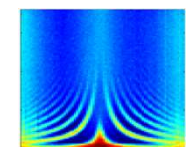
**2017** Coherent shuttling of individual electron spins



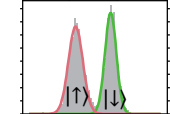
**2017** 3D integration for electron spin qubits patents



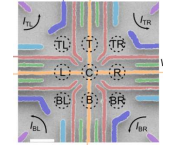
**2018** Spin entanglement at distance in semiconductor quantum devices




**2018** High fidelity spin read-out in Si CMOS devices




**2018** Electrons filling in a 9 dot array



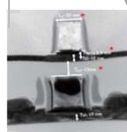

**2007** Poesi Electron pumps for metrology




**2009** AFSID Atomic functionalities in Si devices)




**2011** Demonstration Lg = 50nm Si/Si CMOS




**2013...2015** SIAM SISPIN TOLOP



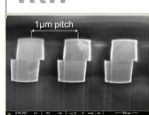
**2016** MOSQUITO



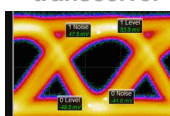
**2016** First 300mm monolithic 3D integration




**2017** Demonstration of 1µm pitch WtW



**2018** 10Gbit/s photonic transceiver

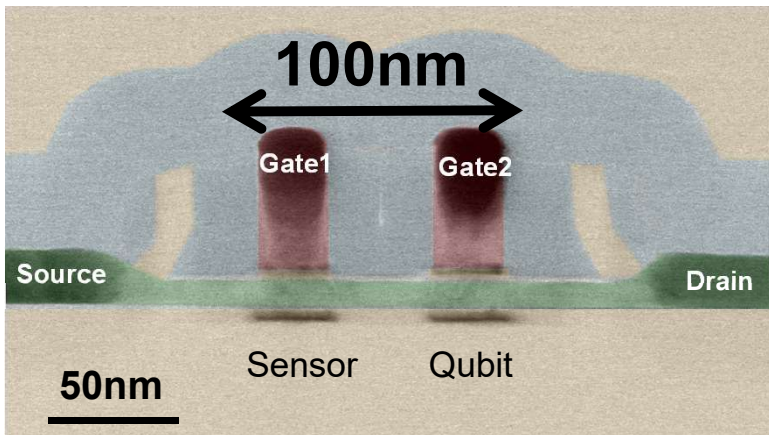


**2018** ERC QuCube





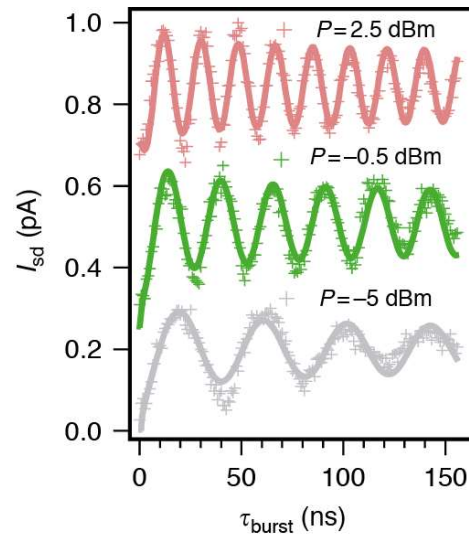
# 1<sup>ST</sup> CMOS SPIN QUBITS (OUR WORK)



## Single qubit gate

Maurand, *Nat. Comm.* (2016)

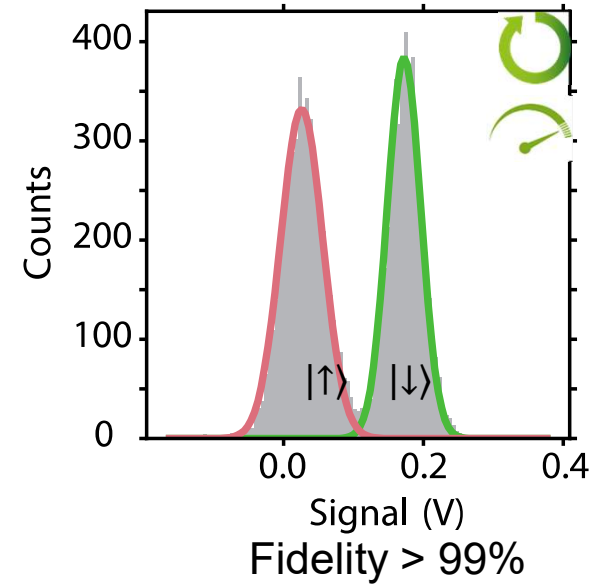
Hutin, *VLSI* (2016)



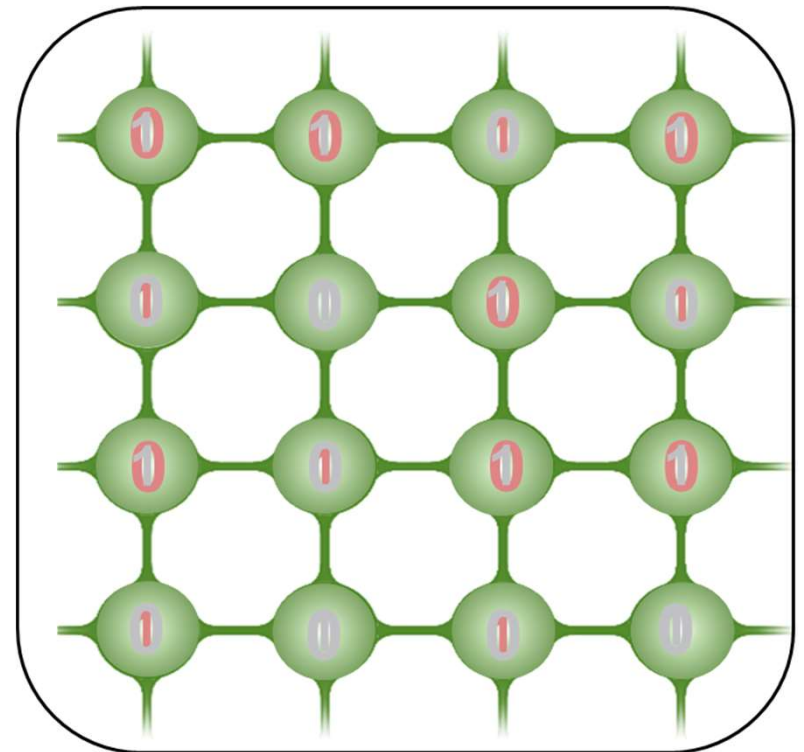
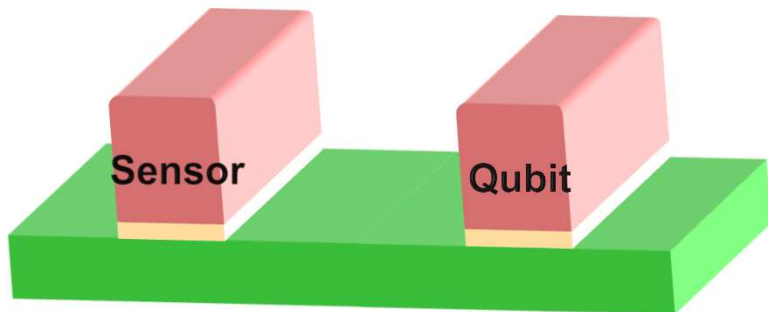
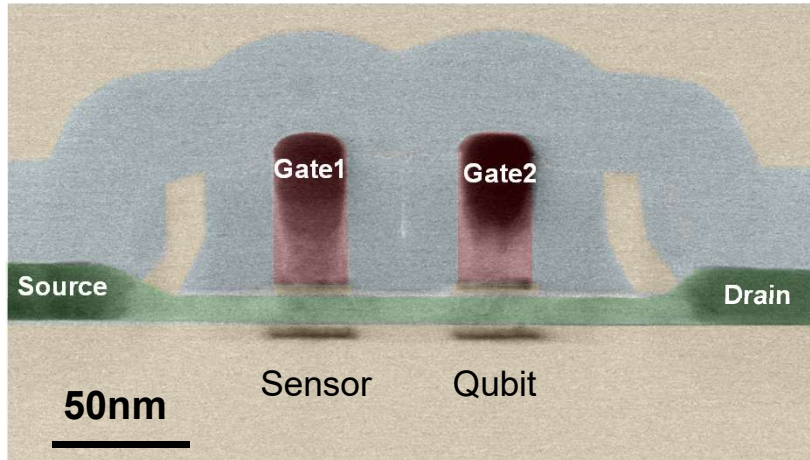
Manipulation time 20ns

## High fidelity RF scalable spin read-out

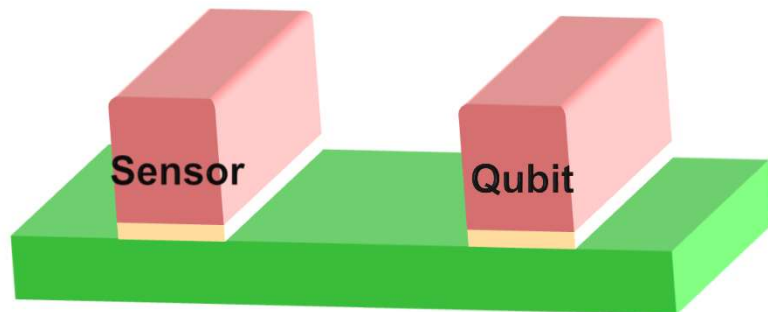
Urdampilleta (to be published)



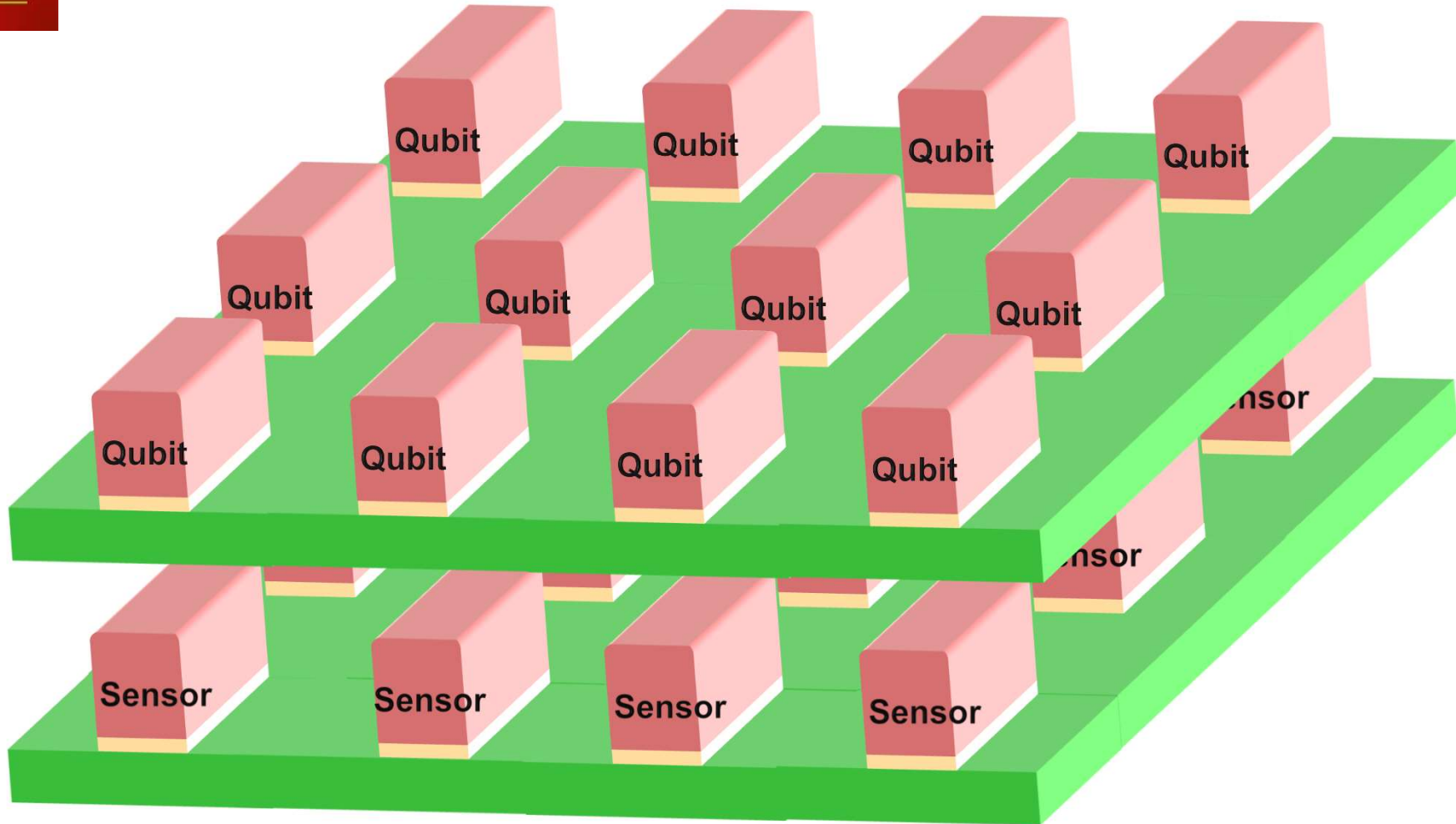
## NEXT STEP: SCALABILITY?



## NEXT STEP: SCALABILITY?



## NEXT STEP: SCALABILITY





## QUCUBE CONCEPT

Patent Hutin, Meunier, De Franceschi, Vinet (2017)

Control gates to manage qubit manipulation



European Research Council  
Established by the European Commission

Qubit layer

Control gates to tune detector/qubit coupling

Sensing layer

Gates to load carriers in sensing layer

## MORE TECHNICAL DETAILS DURING THE CONFERENCE

2:00 PM - 2:25 PM

**7.2 Breakthroughs in 3D Sequential Technology**, *L. Brunet, C. Fenouillet-Beranger, P. Batude, S. Beaurepaire, F. Ponthenier<sup>2</sup>, N. Rambal<sup>2</sup>, V. Mazzocchi, J-B. Pin<sup>\*\*</sup>, P. Acosta-Alba, S. Kerdiles, P. Besson<sup>\*</sup>, H. Fontaine, T. Lardin, F. Fournel, V. Larrey, F. Mazen, V. Balan, C. Morales, C. Guerin, V. Jousseau, X. Federspiel<sup>\*</sup>, D. Ney<sup>\*</sup>, X. Garros, A. Roman<sup>2</sup>, D. Scevola<sup>2</sup>, P. Perreau, F. Kouemini-Tchouake, L. Arnaud, C. Scibetta, S. Chevalliez, F. Aussenac, J. Aubin<sup>\*\*\*</sup>, S. Reboh, F. Andrieu, S. Maitrejean, M. Vinet, CEA-LETI, <sup>\*</sup>STMicroelectronics, <sup>\*\*</sup>Applied Materials Inc., <sup>\*\*\*</sup> SCREEN LASSE*

3:40 PM - 4:05 PM

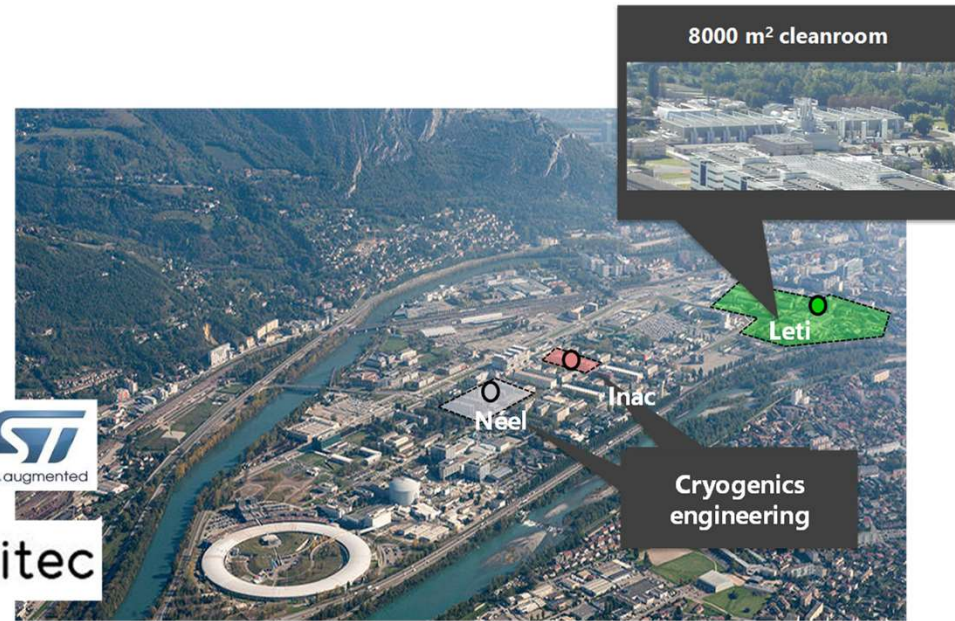
**6.5 Towards scalable silicon quantum computing (Invited)**, *M. Vinet, L. Hutin, B. Bertrand, S. Barraud, J.-M. Hartmann, Y.-J. Kim, V. Mazzocchi, A. Amisse, H. Bohuslavskyi, L. Bourdet<sup>\*</sup>, A. Crippa<sup>\*</sup>, X. Jehl<sup>\*</sup>, R. Maurand<sup>\*</sup>, Y.-M. Niquet<sup>\*</sup>, M. Sanquer<sup>\*</sup>, B. Venitucci<sup>\*</sup>, B. Jado<sup>\*\*</sup>, E. Chanrion<sup>\*\*</sup>, P.-A. Mortemousque<sup>\*\*</sup>, C. Spence<sup>\*\*</sup>, M. Urdampilleta<sup>\*\*</sup>, S. De Franceschi<sup>\*</sup> and T. Meunier<sup>\*\*</sup>, Université Grenoble Alpes, <sup>\*</sup>CEA, LETI, <sup>\*\*</sup>CNRS*



# CONCLUSION



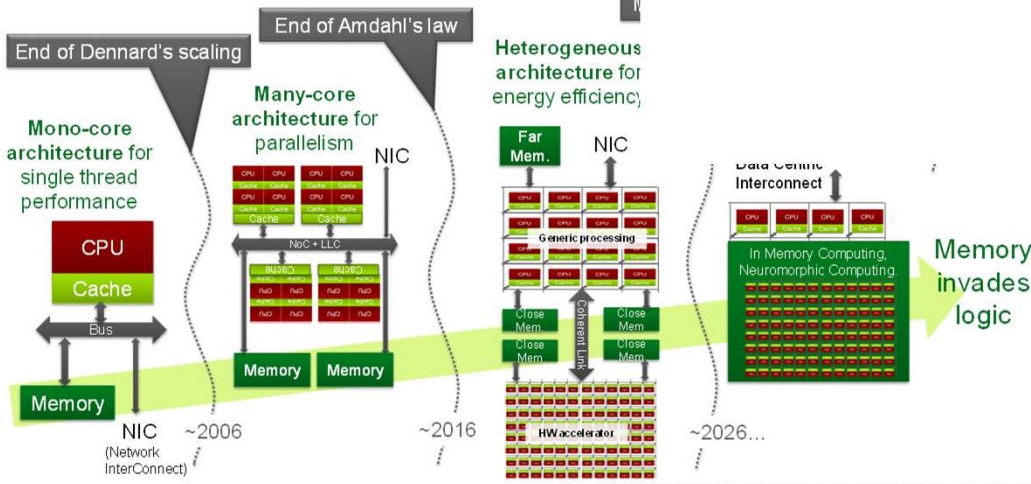
- Geographic proximity
- Exceptional co-location facilities
- Unique ecosystem
- Established collaborations



**Quantum Engineering**  
Univ. Grenoble Alpes



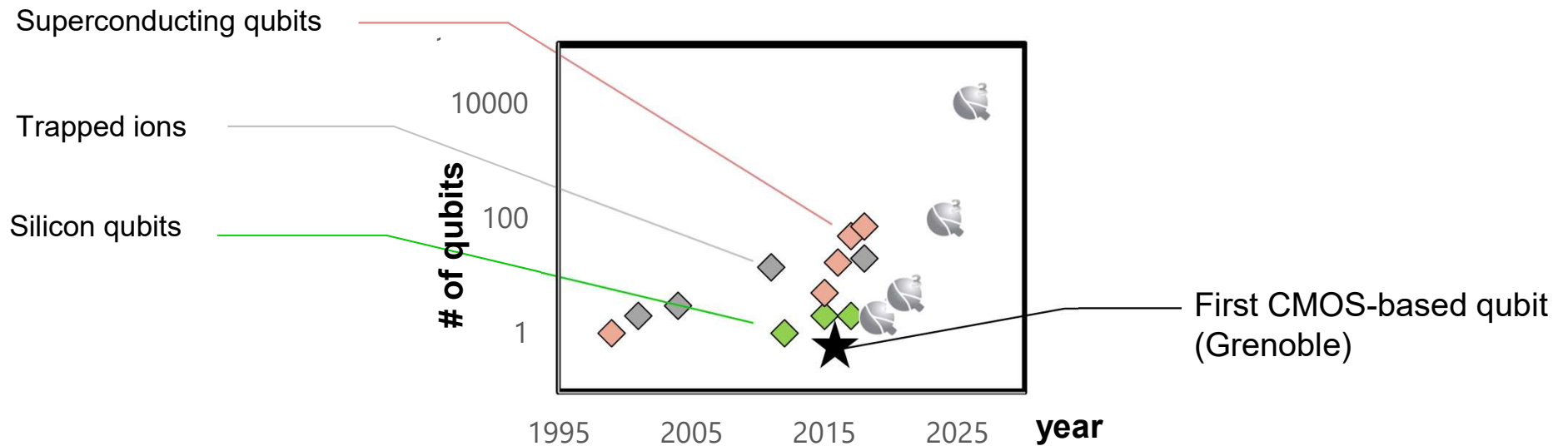
## PROCESSOR ARCHITECTURE EVOLUTION



Leti Devices Workshop | Duboit Denis | Dec 2nd, 2018, Nikko Hotel, San Francisco | 4

## CONCLUSION

We are willing to open a viable path to large-scale qubit integration



Create vast opportunities for the industrial ecosystem

- Semiconductor industry
- Software industry





# Thank you!

[www.quantumsilicon-grenoble.eu](http://www.quantumsilicon-grenoble.eu)



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