For the last 50 years, Leti has been leading innovation in the semi-conductor and healthcare industries using disruptive, miniaturized, and energy-efficient technologies.

Our mission is to design and prototype the next generation of components and systems, supporting incremental improvements to our society while generating value-added growth. Making things smaller, smarter, and more secure with lower energy consumption are the core skills of Leti. We offer breakage solutions for 5G, IoT, precise medicine, transportation and environment, contributing to the competitiveness of the European industry.

With more than 85 ongoing projects, Leti plays a key role in the European research programmes by leading projects based on state-of-the-art technologies and by developing strong alliances with partners.

I would like to thank our industrial partners, institutional fellows and academic collaborators, who have worked closely with us for many years to identify new European paths toward breakthrough technologies. Many thanks to our European team for maintaining Leti’s strong position and ever-extending the frontiers of innovation.

Naturally, we will continue to reinforce our collaborations with European partners and other major research and technology organizations to drive success in European innovation. I hope you will find in Leti’s 2016-2017 European Report a vision of a brighter future.

Leti’s active participation in European projects is a part of its innovation strategy of researching and developing new technologies that address the scientific, industrial and societal challenges of Europe.

Thanks to the efforts of Leti’s teams, and to fruitful discussions with French authorities and European officers, we are actively involved in numerous projects conducted under the umbrella of H2020. Leti is also a partner in the JU ECSEL and EUREKA clusters which are key public-private partnerships for technology development. Overall, these projects are addressing sensors, computing, photonics devices, power electronics, wireless communications and networks, cybersecurity, image & vision, medical devices, metrology and lithography.

Leti, along with its partners, are implementing and nurturing the European roadmaps and visions, defined by European associations, European Technological Platforms (ETP), EIT Knowledge Information Communities, and Public Private Partnerships (PPP). More precisely, we are contributing members to AENEAS, EPIC, Photonics21 PPP, ETP-4HPC, 5G PPP, NetWorld2020 ETP, Nanomedicine ETP, EARPA, etc.

I hope you will enjoy reading these pages and that our experience in the European Projects will encourage you to join us as a partner.
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Within the scope of European project NAREB, CEA-Leti is aiming to develop a more efficient therapy to combat infectious diseases such as tuberculosis and resistant Hospital-Acquired Infections (HAIs).

Lipidic particles (Lipidots) containing antibiotics have been developed and successfully tested, proving their performance in the following aspects:

- improved stability allowing long-term storage;
- adequate biocompatibility profile, when injected repeatedly at high doses;
- distribution within infected tissues;
- improved or maintained antimicrobial efficiency.

Upcoming scheduled tests will enable us to determine the beneficial efficiency/harmlessness of the anti-infectious lipidic particles retained.

The EUROCPS project is intended to furnish Europe with a network of competencies and platforms for enabling an SME from any sector, which builds innovative CPS products, to sustain demand for European manufacturing. The goal is to enable Europe to capture the emerging market of CPS products by offering innovative CPS to business in any sector. The project will also strengthen Europe manufacturing with a network of design centers by initiating synergies between SMEs and major CPS-platforms, by linking users and suppliers across value chains and by providing the continent’s competency providers with fast track industrial experiments.

More than 4000 SMEs have been contacted and 34 projects (Industrial Experiments) have been selected through three open calls. CEA-Leti is involved in 7 IEs, together with ST-F and ST-I industrial platforms. These IEs are win-win situations, in which SMEs, CEA-Leti and industrial platforms can together generate new business. SMEs represent the best indicators of current market and future development, so the EUROCPS project enables CEA-Leti to track promising ideas, technologies and market trends for developing tomorrow’s technologies. SMEs will be able to develop and validate innovative technology solutions thanks to CEA-Leti expertise and industrial partners; the will naturally stimulate leading edge technologies including silicon capabilities.

The MFM project aims to standardize microfluidic interconnects and to foster industrialization of microfluidic-based complex devices. Following the MFM research, an ISO New Work Item Proposal (NWIP) led by CEA-Leti and AFNOR was presented at the International Workshop Agreement held at the British Standards Institute in April 2016. The work is now disseminated worldwide through active participation at the workshop organized by the National Institute of Standards and Technology in June 2017. A solid basis for future microfluidics standardization has been laid through the following actions:

- overviewing the IWA on interoperability of microfluidic devices;
- combining microfluidics and electronics (integration);
- performing cell-based assays/in-vitro diagnostics;
- performing flow control and verification testing;
- designing and testing sensors and interconnectors;
- creating modular systems.

For many years, CEA-Leti has traced an innovative lithography path for sub-0nm nodes using very specific copolymers and implementing a DSA approach. The institute has introduced new materials such as PS and PMMA, and has modelled their interaction as block copolymers by graphoepitaxy, allowing nanometric structure fabrication techniques such as shrinking contact holes on 300mm silicon wafers.

CEA-Leti is in the forefront of research into a new generation of metrology and characterization tools and their associated methodologies to allow development of forthcoming semiconductor technology nodes. New 3D device architectures and materials (e.g. nanowires, III-V, 2D materials and high aspect ratio TSVs) raise major metrology and characterization challenges, which can no longer be overcome by pushing existing methods to their limits.

Among the main targets of 3DAM, CEA-Leti is addressing 3D structure morphology and dimensions, stress and strain, defects and crystal quality, composition, 3D dopant profiling and mobility.
The aim of the European EUROSERVER project is to develop an energy-efficient server design that meets the anticipated needs of exascale computing after 2020. The project develops a range of tools designed to support energy-efficient ARM-based servers for use in data centers. These tools include an innovative scalable memory scheme called UNIMEM, introduction of transparent main memory compression technology to maximize density and bandwidth of external memory, MicroVisor and additional advanced software features to optimize resource sharing and communication within a system, thereby paving the way towards the next generation of more power-efficient servers. There are multiple H2020 follow-up projects implementing the EUROSERVER approach. These could benefit from the project’s technology, including EcoScale, ExaRoDe, ExaLedSi and EuroEXA, to form the basis of a European server. Two spin-off companies have already emerged from the EUROSERVER project: KALEAO Ltd. in Cambridge, UK, which operates laboratories in Crete and Italy, and ZeroPoint Technologies in Gothenburg, Sweden. Dedicated collaboration has been initiated between KALEAO and CEA-Leti. The EuroPROC project conducted in April 2016 involved CEA-Leti, KALEAO and ZeroPoint Technologies.

**PIEZOMAT**

High resolution fingerprint sensing with vertical piezoelectric nanowire matrices

The aim of the European PIEZOMAT project is to develop and demonstrate new fingerprint sensing technology based on piezoelectric nanowires. The challenge of this project is to achieve a reduction in maximum pixel size to increase sensor resolution. Each nanowire or group of nanowires forms a pixel. The nanowires, connected at their base and top end, are subjected to compressive forces. When a finger is placed on the sensor, local deformation of the nanowire network generates a potential, whose amplitude is proportional to the nanowire displacement. One of the technical difficulties to be overcome by CEA-Leti has been to succeed in creating a matrix of doped ZnO nanowires. Moreover, all fabrication stages have been performed in-house.

**EUROSERVER**

Green computing node of European micro-servers

**LOMID**

Thinning and curving of OLED display

Curved microdisplays will reduce the complexity and dimensions of optical systems. In the LOMID project, display flexibility is achieved by thinning the water by chemical mechanical grinding. A dedicated hard coat is then applied to ensure subsequent safe handling of the thinned microdisplays. A first demonstrator has been fabricated with a 45mm radius of curvature without degrading OLED performance.

**SEQUOIA**

Dense wavelength division multiplexing on a silicon photonics platform

Within the scope of the SEQUOIA project, CEA-Leti has demonstrated an echelle grating demultiplexer for dense wavelength-division-multiplexing applications with 16 channels and 100 GHz channel spacing. The echelle grating has been designed and fabricated on a silicon-on-insulator platform with a 300 nm silicon guiding layer. Measured insertion losses of the echelle grating are lower than 2.6 dB for all channels and crosstalk is below 15 dB. Error-free transmission has been achieved for all channels with negligible penalty.

**PIEZOMAT**

Innovative reliable chip designs from low-powered unreliable components

The purpose of the i-RISC project is to increase knowledge and understanding of error-correcting codes within unreliable systems from two complementary perspectives (i) their ability to provide reliable error protection, if they operate on unreliable hardware and (ii) development of specific methods to embed error correcting techniques into circuit design such that fault-tolerant circuits are obtained. In i-RISC, CEA-Leti has contributed to developing theoretical foundations and practical designs of error correcting codes with fault-tolerant encoder and decoder architectures. The institute has also contributed to developing mathematical models and a theory of error coding-driven circuit synthesis. These developments pave the way for new, more powerful fault-tolerance techniques that will be inherently required for designing upcoming nanoelectronic devices.

**SISPIN**

Silicon platform for quantum spintronics

Silicon is already well known for making computer chips and will soon be the material of choice for the next generation of computing devices, known as quantum processors. Leveraging the industrial base of well-established complementary metal-oxide-semiconductor (CMOS) silicon technology would be a clear advantage to accelerating the development and integration of scalable quantum computing architectures. During the SISPIN project funded by the EU, a silicon quantum bit (qubit) device made with an industry-standard fabrication process has been demonstrated. The device consists of a two-gate, p-type transistor with an undoped channel. At low temperature, the first gate defines a quantum dot encoding a hole spin qubit, the second gate a quantum dot used for the qubit read-out. All electrical, two-axis microwave modulation to the first gate. The demonstrated qubit functionality in a basic transistor-like device constitutes the first promising step towards the elaboration of scalable spin qubit geometries in a readily exploitable CMOS platform.
The main objective of the 3CCAR project is to form a collaborative environment embracing almost 50 European research teams with common visions and aims in the well-defined, exponential growth area of electro-mobility. Such a large project is naturally divided into ten smaller parts, named Supply Chains (SC), which define a precise research field. Two CEA institutes (CEA-Leti and CEA-Liten) are taking part in 3CCAR and active in the fields of Smart Battery Cells (SC1), Functionally Integrated Powertrain (SC2) and Smart Semiconductors for Fuel Cells (SC3).

- The aim of the Smart Battery Cell activity is to build a 48V battery module demonstrator using smart Li-ion cells with embedded electronics for measuring cell properties, ensuring safe control and communicating with the external Battery Management system (BMS). CEA-Leti and CEA-Liten teams are designing the best architecture and algorithms for embedded Electrochemical Impedance Spectroscopy (EIS) and estimating the electromechanical performance of the cell. This output will be used by other partners to determine the cell temperature.

- The entire vehicle powertrain falls within the scope of the Functionally Integrated Powertrain activity. CEA-Leti and CEA-Liten engineers are designing and simulating an electric motor with its integrated power controller to be ideally constructed using GaN transistor technology.

- All the elements and devices composing a Smart Fuel cell system are addressed by the Smart Semiconductors for Fuel Cells activity. CEA-Liten’s team is developing a prototype of a DC/DC power converter, whose characteristics make it suitable for range extender applications with a 10 - 15 kW power output.

Results achieved by the middle of the project’s 2nd year:

- Smart Battery Cells: hardware development is now finished, embedded software is under development. Preliminary laboratory tests on one GenIQ cell equipped with our embedded electronics (only the analog part) allowed us publishing first results (conference paper and poster).

- Functionally Integrated Powertrain: motor and inverter specifications have been defined and simulations started.

- Smart Semiconductors for Fuel Cells (CEA-Liten only): power converter specifications have been defined and simulation started in January 2017.

Publications

The presented poster was awarded with the ‘Best Poster Award’. Full text link: https://www.researchgate.net/publication/308470908_Electronic_Module_for_the_Thermal_Monitoring_of_a_Li-Ion_Battery_Cell_through_the_Electrochemical_Impedance_Estimation

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TRL

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ACTIVAGE is a European Multi Centric Large Scale Pilot on Smart Living Environments. The main objective is to build the first European IoT ecosystem across 9 Deployment Sites (DS) in nine European countries, reusing and scaling up underlying open and proprietary IoT platforms, technologies and standards, and integrating new interfaces needed to provide interoperability across these heterogeneous platforms, that will enable the deployment and operation at large scale of Active & Healthy Ageing based solutions and services, supporting and extending the independent living of older adults in their living environments, and responding to real needs of caregivers, service providers and public authorities.

The project will deliver the ACTIVAGE IoT Ecosystem Suite (AIOTES), a set of Techniques, Tools and Methodologies for interoperability at different layers between heterogeneous IoT Platforms and an Open Framework for providing Semantic Interoperability of IoT Platforms for AHA, addressing trustworthiness, privacy, data protection and security. User-demand driven interoperable IoT-enabled Active & Healthy Ageing solutions will be deployed on top of the AIOTES in every DS, enhancing and scaling up existing services, for the promotion of independent living, the mitigation of frailty, and preservation of quality of life and autonomy. ACTIVAGE will assess the socio-economic impact, the benefits of IoT-based smart living environments in the quality of life and autonomy, and in the sustainability of the health and social care systems, demonstrating the seamless capacity of integration and interoperability of the IoT ecosystem, and validating new business, financial and organizational models for care delivery, ensuring the sustainability after the project end, and disseminating these results to a worldwide audience. The consortium comprises industries, research centres, SMEs, service providers, public authorities encompassing the whole value chain in every Deployment Site.

42 months

ACTIVAGE at a glance

Project Coordinator
MEDTRONICS global project, IRT Nanoelec / Leti for the french deployment site

Partners
49 partners from 9 countries: Finland, France, Germany, Greece, Ireland, Italy, Spain, Switzerland, UK
FR: CEA-Leti, Département de l'Isère, FDT (Fédération Française de Domotique), IRT Nanoelec (leader of the French consortium), KORIAN IMA (InterMédiation Assistance), Madopra, STM, TAGDA, Technosens

Total budget
€ 25 m.
EC Contribution
€ 20 m.

Contract Number
732679

ACTIVAGE
Breaking barriers for a sustainable Active and Healthy Ageing through IoT

Large Scale Pilots: smart environment for EC Programme H2020 IoT-01-2016

Keywords
Aging well
Cybersecurity
Internet of Things (IoT)
Interoperability
Large scale deployment
Smart home
User centered design

ACTIVAGE is responsible for the Interoperability and Security workpackage which aims to deliver the ACTIVAGE IoT Ecosystem Suite (AIOTES). CEA-Leti is developing the open source IoT platform SensiNact’s available through the Eclipse community. SensiNact will be integrated into the AIOTES and required bridge are being developed, in particular, to make the solution compatible with the Z-Wave radio protocol, which is becoming increasingly popular in the field of home automation.

Security and privacy risk analysis of the architectures using STRIDE and DREAD complementary methodologies have been defined and will be used by all deployment site of the large scale pilot.

CEA-Leti through the IRT Nanoelec, is leading the French Deployment Site (DS) based in Isère department. The focus of ISERE-DS is to propose and test modular personalized IoT packs to enhance safety, comfort and social link to enable elderly to stay autonomous at home as long as they wish. The concept is to follow persons evolving needs along the ageing stage and support caregivers’ intervention to detect early sign of fragility, prevent loss of autonomy, and avoid unnecessary hospitalization. In coordination with TASDA partner and the local authority framework IsèreADOM, an User-Centered Design co-conception process has been conducted involving all the stakeholders, leading to 38 requirements for the IoT Packs.

CEA-Leti has specified the IoT equipment’s to fulfil the requirements and integrated a first IoT solution using SenSinact middleware and integrated to Technosens partner commercial solution for elderly social inclusion.

To ensure deployment in the best conditions, the IRT Nanoelec has set a dedicated space on its existing living lab facility the Link Technology Platform (PTL). Set up at the end of summer 2017, this space of about twenty square meters represents a room of nursing home composed of a bedroom and a bathroom. The solution is under test at the PTL and has been also deployed in a testbed room at the rehabilitation clinic Korian Les Granges. The solution will be fully operational first quarter 2018 and shall be deployed in 10 institution rooms and 70 individual houses along the project duration.

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ACTIVE HANDS

The Active Hands Project is dedicated to support independent living of individuals with difficulties to organize daily activities due to deficits of the central neural system. The Active Hands project will develop an innovative home-based guidance system that will support individuals who have suffered functional loss in daily tasks such as tea-making. The platform monitors the user's ability to follow a pre-defined succession of actions using wireless sensors and a Kinect camera. When users make a mistake or requests help, audio-visual cues help to guide them to a successful outcome while fostering their independence at home. The platform directly supports individuals with cognitive disorders such as dementia and stroke patients. The existing healthcare system will also benefit by reducing the demands placed on existing home support services and by linking health care professionals to the platform for remote monitoring.

12 months

ACTIVE HANDS
at a glance

**Project Coordinator**
Technical University Of Munchen TUM (Ge)

**Partners**
ES: University Polytechnica de Madrid UMP 5
FR: IRT Nanoelec, CEA-Leti, MADOPA, TECHNOSENS

**Total budget**
e 0.426 m.
**EC Contribution**
e 0.426 m.

**Contract Number**
X25143

Leti in ACTIVE HANDS

CEA-Leti/IRT Nanoelec has designed and developed the compact, robust, reliable wireless device «ACTISENS» for attachment to an object to monitor complex activity, such as tea-making, and provide action recognition. Device re-design was performed in the first month of this project based on CEA-Leti’s know-how acquired on the «PATCH Sante» Carnot project.

In conjunction with a partner, functional specifications have been drawn up for the ACTISENS device based on a usage-centered approach. ACTISENS integrates a 3-axis Accelerometer/3-axis Gyroscope (3A3G) sensor to estimate the object’s motion and trajectory, a proximity sensor to detect object grasping and a temperature sensor to measure the temperature of the object surface. It also features a rechargeable battery, BLE communication and RGB LED usage indicators. Four devices are needed to run the rehabilitation application. BLE communication software has been developed to provide reliable, low data losses at a high transmission rate (50 Hz).

ACTISENS communication has been thoroughly characterized, performances are higher than 98% at 50Hz with four devices connected (8 data / devices). CEA-Leti has defined the optimum system architecture together with UPM and TECHNOSENS. The TECHNOSENS eLio box gateway is at the center of the future service. This gateway has been adapted to BLE communication to gather all the gesture data from the Kinect and the ACTISENS. The solution has been installed in the CEA-Leti/IRT Nanoelec Living Lab dedicated to the smart environment for ageing well to functional testing prior to pilot trials with a patient.

CEA-Leti, IRT-Nanoelec and TECHNOSENS have delivered a full set of 3 ACTISENS + Gateway systems to UPM for algorithm development and TUM for pilot trials.
Leti in ADVANTEX

Progress is clearly visible in the ADVANTEX project with significant advances made in technical textile technologies. The project has been structured to include several iterations of sensor and sub-system development and integration in firefighting personal protection equipment (clothing, gloves and boots). Each sequential improvement builds on an existing protective clothing product line, which allows rapid deployment of innovation in successive products. CEA-LETI is strongly involved in developing better sensors and wireless communication between sensors and the central processing unit carried by the firefighter. A unique wireless RFID tag reader is used to transmit power remotely, interrogate and read out signals from sensors. A first SOI technology-based ASIC has been designed, fabricated and tested in various environments. Performance has been validated in -40 to 180°C temperature range with remote powering of sensors possible up to a distance of 35 cm. This can be extended to several meters, when the sensor is fitted with an accumulator.

Bulk acoustic wave gas sensors have been developed to incorporate process optimization and to achieve a resonant frequency of \(2.4\) GHz. Sensor functionalization can be programmed for detection of different gases. To date, detection of carbon dioxide and hydrogen have been validated, while chemistries for detection of other gases are under development. In parallel, nano-electromechanical microsystems (NEMS)-based sensors for gas detection have also been investigated for the firefighting environment. NEMS rely on piezoresistive resonant excitation of a free-standing cantilever, which is functionalized to detect a specific gas or family of gases. This type of sensor can eventually be integrated using the product offer of the APIX Analytics company, a start-up launched by CEA-LETI.
EC Programme H2020-EUJ-2016
Keywords Big data, Edge processing, Europe, Internet of Things (IoT), Japan, Smart city, Smart tourism

**BigClouT**

**Big data meeting Cloud and IoT for empowering the citizen clout in smart cities**

As we enter 2017, the world is facing a number of critical challenges such as global warming, economic crisis, security threats, inequality, natural disasters and ageing society. Urban areas are particularly affected, given that the world population is increasingly concentrated in those areas. ICT solutions have the potential to change the world and improve the quality of life and security of its citizens. In particular, IoT, cloud and big data are today’s key enablers for increasing the efficiency in using shared urban infrastructure, economic and natural resources.

The overall concept of the BigClouT project is to give an analytic mind to the city by creating distributed intelligence that can be implanted in the whole city network. The unprecedented number of connected things and the associated big data naturally raise new technical challenges in terms of interoperability, scalable and online data processing, actionable knowledge extraction, self-management, security and privacy. The BigClouT project is bringing together resources and knowledge necessary from prestigious European and Japanese institutions for tackling those challenges.

BigClouT will leverage the results of the ClouT project and bring them further steps and add, in particular, distributed intelligence with edge computing principles, big data analytics capability and self-awareness property.

The BigClouT platform will be deployed and validated in 4 pilot cities in the project, Grenoble, Bristol, Tsukuba and Fujisawa. BigClouT gives a particular importance to the involvement of citizens during the whole lifetime of the project, from use case definitions to validation. BigClouT has also the ambitious objective of creating a community of external end-users to build their own applications/business on top of BigClouT tools and platform, and to maintain alive this community during the project and beyond, which will ensure the sustainability of the results of the ClouT and BigClouT projects.

**BigClouT at a glance**

- **Project Coordinator**
  - CEA-Leti (FR), NTT East (JP)
- **Partners**
  - FR: Absiskey CP, Grenoble-Alpes Métropole
  - GR: NTU Athens
  - IT: Engineering Ingegneria Informatica Spa
  - JP: Keio University, National Institute of Informatics, NTT East, NTT R&D, University of Tsukuba
  - UK: BristolIs Open Limited, Lancaster University
- **Total budget**
  - € 3 m.
  - EC Contribution
  - € 1.5 m.
  - (+ 1.5 m. contribution from Japanese NICT)
- **Contract Number**
  - 723139

**Leti in BigClouT**

CEA-Leti is coordinator of the European side of the project. At the technical level, CEA-Leti is providing its IoT data collection and processing platform, sensiNact. This comprises a software platform for collecting, processing and redistributing IoT data relevant to improving people’s quality of life through various applications from domains such as smart city, smart home, smart transport, etc. It provides programming interfaces for different data access modes (on-demand, periodic, historic, etc.) as well as application development and deployment to build easily and rapidly applications on the platform.

The platform will be enhanced with self-management properties and intelligence at gateway level by integrating the machine learning techniques provided by the project. The objective is to distribute data processing at the edge level, thereby reducing data forwarding to the Cloud in response to the concerns of network traffic, energy consumption and user data privacy. CEA-Leti is also providing its IoT service creation tool, sensiNact Studio, having added a dependability property to it to allow reliable, secure IoT application building.

Working closely with the Grenoble-Alpes Metropole, the platform will be used for urban deployment the purpose of monitoring an industrial area in Grenoble and the impact of business tourism to the local economy. Along with the other pilot deployments in partner European and Japanese cities, the project will demonstrate the platform concept in relevant environments, thereby increase its TRL.
BONVOYAGE

From Bilbao to Oslo, intermodal mobility solutions and interfaces for people and goods, supported by an innovative communication network

BONVOYAGE will design, develop and test a platform optimizing multi-modal door-to-door transport of passengers and goods. The platform integrates travel information, planning and ticketing services, by automatically analysing non-real-time data from heterogeneous databases (on road, railway and urban transport systems); real-time measured data (traffic, weather forecasts); user profiles; user feedback. The platform is supported by an innovative information-centric communication network that collects and distributes all the data required. The highly heterogeneous, distributed and mobile nature of data, coming from data-centers, sensors, vehicles, goods and people on the move, calls for an innovative networking paradigm. Current networks (e.g. Internet) limit themselves to “just” providing communication channels between hosts. Our paradigm, called Internames, allows communications among entities identified by names, without the constraint of a static binding to a particular location. The request of a “user” (be it a person or a parcel) to travel from source to destination is managed by the platform with several tools: Metadata Handler collects and elaborates data related to the request and generates a corresponding Context; User Profiler creates a personalized profile; Context Handler collects and elaborates data related to the request and generates a personalized context; Multi-Objective Optimizer develops personalized travel instructions, optimal for the Context and User Profile. The user may give feedback, before accepting the travel itinerary. If a trip is not available at request time, the user is notified if it becomes available later on. An Actuator triggers the necessary services. A Tariff Scheme Designer is responsible for the multi-part tariff schemes.

BONVOYAGE at a glance

Project Coordinator
CNIT (IT)

Partners
AU: Fluidtime
ES: Azkar, Bilbao
FR: CEA-Leti
IT: CNIT, CRAT, Trentalix
NO: Oslo, SINTEF

Total budget
€ 4 m.
EC Contribution
€ 4 m.

Contract Number
635867

Leti in BONVOYAGE

- CEA-Leti’s objective is twofold:
  1) to develop an algorithm to assess automatically the user transportation mode and to define the user modal share (e.g. User A never rides a bike, User B never takes a plane…)
  2) to develop an algorithm to assess automatically user stress level; transport mode and user stress level are both used for inferring a traveler profile in the BONVOYAGE project.

- CEA-Leti is working with 2 types of sensors:
  - wearable sensors (Empatica® wristband) for assessing user stress level.
  - a first CNIL-certified database containing 217 recordings has been drawn up for development of initial machine-learning algorithms;
  - a first algorithm has been implemented to recognize 7 different transport modes (walking, running, rail transport, air transport, bicycle, stationary mode);
  - offline average performances (i.e. on computer, from database) obtained are:
    - 64% (with GPS signal)
    - 74% (when GPS signal is not received by the smartphone)

- New mathematical features will be designed to improve the mathematical model and achieve better transport mode recognition. A first Android application embedding Version 1 of the transport algorithm has been developed. This Android App includes 3 functionalities:
  - Raw data recording from smartphone sensors
  - Wifi data transfer to secured (SFTP) server, enabling data acquisition in worldwide
  - Transport mode recognition in real time and graphical display.

- Real-time assessment of user stress level delivered by wearables:
  - initial comparative analysis of data recorded by medical devices and a wearable Empatica® wristband has confirmed the reliability of wearable data;
  - a first algorithm has been developed from recorded real-life data using Blood Volume Pressure (BVP) and ElectroDermal Activity (EDA) as input signals;
  - this algorithm has been embedded in a first Android App version featuring a Bluetooth connection to the Empatica® wristband sensors.

- A first demonstration of the transport mode and user stress level Android Apps was performed and witnessed by the EC expert and Project Officer during a project review meeting.

- Both these Android Apps will be integrated into the BONVOYAGE Android App at the final project stage.

Publications

© CEA-Leti
2016.

CEA-Leti has developed an IoT platform, sensiNact, in the context of several EU projects and already validated it in different application domains. The platform follows rather a centralised (or hierarchical) approach for management of a connected IoT devices and sub-platforms. In the BRAIN-IoT project, the platform sensiNact will be extended with a distribution support. The idea is to allow one sensiNact platform to be able to interact with others in a peer-to-peer fashion. Besides, the BRAIN-IoT project will allow adding edge computing features to sensiNact distributed platforms and validating the approach within the project’s test sites in water management and robotic based logistics domain.

The distribution of CEA-Leti’s sensiNact platform is based on the open source software model. Its exploitation strategy is based on creating developer ecosystems for different application domains at national and international levels and accompanying the relevant stakeholders (small and large industries, cities, etc.) for their digital transformation. SensiNact is an open source project in the Eclipse foundation, which has a large and active community of developers all around the world, in particular in the IoT domain. CEA-Leti has a large portfolio of public and private, national and international partners towards which this platform is being promoted. The core of the platform is open, however added value services and features are to be valorised by CEA-Leti’s industrial partners. BRAIN-IoT project will increase the added value of the sensiNact by bringing additional features such as distribution, edge computing capabilities and dependable service composition.
ClouT
Cloud of Things for empowering the citizen clout in smart cities

ClouT’s overall concept is leveraging the Cloud Computing as an enabler to bridge the Internet of Things with Internet of People via Internet of Services, to establish an efficient communication and collaboration platform exploiting all possible information sources to make the cities smarter and to help them facing the emerging challenges such as efficient energy management, economic growth and development.

ClouT will provide infrastructures, services, tools and applications that will be reused by different city stakeholders such as municipalities, citizens, service developers and application integrators, in order to create, deploy and manage user-centric applications taking benefit of the latest advances in internet of things and cloud domains. ClouT with its user-centric approach, will also offer to end-users the possibility of creating their own Cloud services and share them with other citizens.

ClouT will have the following major outputs: i) a smart city infrastructure with a near to infinity processing and storage capacity of data from trillions of things and people that are integrated via virtual services in the Cloud while keeping their universal interoperability; ii) a set of platform level tools and services aiming at facilitating IoT application development, deployment and supervision iii) secure data access and processing mechanisms that can handle big data acquired from the heterogeneous sources in quasi real-time; iv) innovative city applications and field trials in four pilot cities: Santander and Genova in Europe, Mitaka and Fujisawa in Japan.

ClouT will reduce costs and time to develop and deploy new applications by using new flavours of public-private partnerships inspired by the Cloud models, supporting win-win strategies for all stakeholders. ClouT’s ultimate goal is to join the forces and create a long-lasting synergy for smart city initiatives between Europe and Japan.

Leti in ClouT

Within the scope of the ClouT project, CEA-Leti has developed its IoT data collection and processing platform (sensiNact) and a tool for quickly building IoT applications (sensiNact Studio). SensiNact is a software platform for collecting, processing and redistributing IoT data relevant to enhancing urban citizens’ quality of life through various applications from domains such as the smart city, smart home, smart transport, etc. It provides programming interfaces for different data access modes (on-demand, periodic, historic, etc.) as well as application development and deployment to build easily and quickly innovative applications on the platform.

The sensiNact platform has been used in the project to aggregate data from IoT devices deployed in the 4 project pilot cities of Santander, Genoa, Mitaka and Fujisawa. Over 10,000 physical devices and 500,000 virtual devices have been connected to the platform via more than 10 communication protocols. Over 5000 end-users used the 5 ClouT applications deployed in the 4 pilot cities via applications such as environmental monitoring, context aware coupons, city dashboards, citizen safety and elderly care social networks. These have been validated by field trials involving real end-users.

In addition to real-life testbeds, multiple scientific publications have been edited during the project, in particular a book entitled “Enablers for Smart Cities”, which includes a specific chapter on the sensiNact platform. In 2016 the ClouT project received the “Star of Europe” award from the French Ministry of Research and Education for the project’s successful achievements and generated impact.

The ClouT project has built the foundations of its follow-up project, BigClouT, which complements the ClouT architecture with big data aspects. BigClouT was launched in July 2016 and will run for 3 years.

Publications
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Batteries are not yet the ideal energy container they were promised to be. They are expensive, fragile and potentially dangerous. Moreover, the current Electric Vehicle (EV) cannot compete yet with traditional vehicles when it comes to driving range and flexibility. EVERLASTING intends to bring Li-ion batteries closer to this ideal by focusing on the following technology areas.

- **Predicting the behavior of battery systems in all circumstances and over their full lifetime.** This enables accurate dimensioning and choice of the correct battery type, leading to lower cost. It also facilitates the development of a powerful battery management system during all stages of its evolution from idea to fully tested product.
- **Sensing signals beyond the standard parameters of current, voltage and temperature.** This multi-sensing approach provides more varied and in-depth data on the status of the battery, facilitating proactive and effective management of the batteries, preventing issues rather than mitigating them.
- **Monitoring the status of the battery by interpreting the rich sensor data.** By intelligently combining this information with road, vehicle and driver data, we intend to offer accurate higher-level driver feedback. This induces a bigger trust and hence a lower range anxiety.
- **Managing the battery in a proactive way, based on a correct assessment of its status.** Efficient thermal management and load management results in increased reliability and safety and leads to lower overall cost through an increased lifetime.
- **Defining a standard BMS architecture and interfaces and gathering the necessary support in the market.** This allows an industry of standard Battery Management System (BMS) components to flourish which will result in lower cost.

**EVERLASTING at a glance**

- **Project Coordinator**
  - Carlos Mol, VITO (BE)
- **Partners**
  - **BE:** Vlaamse instelling voor technologisch onderzoek V.L.I.N.V.
  - **DE:** Lion SMART GmbH, Rheinisch-Westfälische technische Hochschule Aachen, Technische Universität München, TÜV Süd Battery testing gmbh
  - **FR:** CEA, Siemens industry software
  - **IS:** Algoldion LTD
  - **NL:** Technische universiteit Eindhoven, VDL Bus & Coach BV
  - **SK:** GreenWay Operator a.s.
- **Total budget**
  - **€ 8.2 m.**
  - **EC Contribution**
    - **€ 8.2 m.**
- **48 months**
  - **Sep. 2016 > Sep. 2020**

**EVERLASTING Electric Vehicle Enhanced Range, Lifetime And Safety Through INGenious battery management**

**EVERLASTING adresses a series of challenges related to the understanding of batteries.** CEA-Liten and CEA-Leti institutes are both contributing to this project as follows.

- **a)** Safety hazards. **EVERLASTING** provides new, unique model-based tooling and methods for robust detection of safety hazards, prevention of false detection and early prediction of thermal runaways.

- **b)** Battery aging phenomena. **EVERLASTING** generates knowledge through online estimation of battery deterioration by advanced sensing and analysis using cutting-edge mathematical techniques. CEA-Leti contributes to this by defining sensing strategy.

- **c)** Reducing complexity of holistic battery models. CEA-Liten is investigating techniques for battery cell model order reduction that allow trade-offs between accuracy and computational complexity.

- **d)** Modeling and simulation tools. CEA-Liten is developing and validating a better tool chain that supports model-based validation of a BMS throughout the development stages.

- **e)** Range prediction and optimization to decrease range-related anxiety. CEA-Liten is developing BMS technology that will extend driving range without increasing battery physical size. Charging time will also be reduced by 30%.

- **f)** Sensors and algorithms to predict safety hazards. CEA-Leti is contributing to new model-based tooling and methods for smart safety hazard detection and prediction. For the first time, proactive and reactive safety management will prompt corrective actions to prevent fires, which have already caused Ms of damage, personal injuries and even death. Such tools and methods will increase the reliability, safety and consumer demand for EVs but also assist the industry in meeting the stricter safety standards and regulations being developed in response to transportation battery failures.

CEA-Leti is developing new predictive intelligence algorithms to eliminate the drawbacks involving the passiveness of existing battery safety management systems. It is establishing conditions for efficient warning, correction and intervention for benign, chronic and acute safety hazards by introducing the new concept of safety domains and safety time constants. This concept is a powerful tool in developing advanced Lithium-Ion Battery (LIB) designs for EV applications that optimize performance, safety and ergonomy.
FED4SAE
Federated CPS Digital Innovation Hubs for the Smart Anything Everywhere Initiative

The overall ambition of the FED4SAE innovation action (IA) is to boost and sustain the digitization of the European industry by strengthening competitiveness in Cyber Physical Systems (CPS) and embedded system markets. In alignment with the «Smart Anything Everywhere» initiative goals, FED4SAE will:

- create a pan-European network of Digital Innovation Hubs (DIH) by leveraging existing regional ecosystems across full value chains and a range of competencies. DIHs will enable both tech and non-tech innovative Third parties (Startups, SMEs, Midcaps) from any sector to build new products and services with “digital inside”;
- act as a European added-value one-stop-shop to facilitate innovators-suppliers cross-border partnerships which will accelerate innovation in products and processes of European Third parties by providing technical, industrial and innovation management expertise. This will lead to quantifiable increases in market shares, productivity, industrial capacities of the Third parties, and a broader adoption of CPS and embedded systems solutions;
- link innovators to investors associated to DIHs to reach out to further funding opportunities and enable the next steps of the Third parties’ developments after completing their application experiments (AEs);
- ensure the self-sustainability of the DIHs pan-European network by developing cooperation with regional organizations and key stakeholders engaging public and or private investment to fund FED4SAE network activities.

FED4SAE is built upon the key learnings obtained in the EuroCPS, GateOne-project, OPSE Labe IA. FED4SAE will leverage the best practices related to Third party engagement, submission, evaluation and selection of AEs. FED4SAE will give birth to a competitive ecosystem where European Startups, SMEs and Midcaps will thrive as they access to leading technology sources, competencies and industrial platforms and also to well-connected business infrastructures and existing regional innovation hubs.

Leti in FED4SAE

First year for the FED4SAE so no real outcome at this stage, but thanks to the EUROCPS experience, CEA-Leti foresees results, impacts and benefits:

- expected results: support Third parties to integrate innovative technologies in their products and services. Transfer advanced low-power technology bricks into Third parties CPS solutions;
- exploitation strategy: strengthen or create new collaborations with Third parties, extend its ecosystem to reach more Third parties;
- benefits: learning about innovative products and services technology needs by Third parties. Learning about start-ups, SMEs, midcaps business case constraints. Identification of the next technologies to develop. Learning about innovation management needs to adopt innovation.

36 months

FED4SAE at a glance

Project Coordinator
CEA-Leti (FR)

Partners
AT: AVL
CH: CSEM
DE: Fraunhofer, Fortiss
ES: UNICAN
FR: BLIMORPHO, CEA-Leti, STMicroelectronics, Thales
HU: DME
IE: Intel
IT: STMicroelectronics
UK: Digital Catapult

Total budget
€ 7.6 m.
EC Contribution
€ 6.9 m.

Contract Number
761708
The development of the Internet of Things is set to have a strong impact on many aspects of society. Test-beds and experimental facilities, both of small scale and up to city scale, will be an essential enabler to facilitate the development of this vision. Facilitating the access to these test-beds to a large community of experimenters is a key asset to the development of a large and active community of application developers, necessary to address the many challenges faced by European and Japanese societies. FESTIVAL project's vision is to provide IoT experimentation platforms providing interaction facility with physical environments and end-users, where experimenters can validate their Smart ICT service developments in various domains such as smart city, smart building, smart public services, smart shopping, participatory sensing, etc. FESTIVAL testbeds will connect cyber world to the physical world, from large scale deployments at a city scale, to small platforms in lab environments and dedicated physical spaces simulating real-life settings. Those platforms will be connected and federated via homogeneous access APIs with an “Experimentation as a Service” (EaaS) model for experimenters to test their added value services. There have been long years of research work in Europe and Japan on federated testbeds and more recently on IoT testbeds. FESTIVAL will carry on this work and will seek to improve it as much as possible make reuse of existing software and hardware available in Europe and in Japan for building such testbeds. Mutually applying European enablers for Japanese testbeds and vice versa in a multi-device, multi-protocol and multi-cultural environment.

FESTIVAL has also involved its Art & Science division through a video-maker artist, who interprets big data generated by the platform and reflects it in his art work. led by CEA-Leti, the FESTIVAL project consortium constitutes the core of the Urban Technology Alliance, a working group created in Eclipse Foundation, which will bring together various worldwide stakeholders in the smart city domain.

CEA-Leti is coordinator on the project’s European side. On a technical level, the institute is providing its IoT data collection and processing platform, sensiNact. This comprises a software platform allowing collection, processing and redistribution of IoT data relevant to improving people’s quality of life through various applications from domains such as smart city, smart home, smart transport, etc. The sensiNact platform provides programming interfaces for different data access modes (on-demand, periodic, historic, etc.) as well as application development and deployment for easily and rapidly building innovative applications on top of it. The sensiNact platform has been used in the project as a federator of IoT testbeds by generating data from IoT devices deployed at different testbeds at Santander city, two train stations in Osaka, experimental smart homes on CEA-Leti premises and in Japan, etc. As a result, experimenters (including those external to the project) are offered uniform, federated access to this rich set of European and Japanese IoT resources via a unique tool. Experimenters are therefore able to use, compose and extend these resources for developing and testing applications in close-to-real conditions in a multi-device, multi-protocol and multi-cultural environment.

CEA-Leti has also involved its Art & Science division through a video-maker artist, who interprets big data generated by the platform and reflects it in his art work. Led by CEA-Leti, the FESTIVAL project consortium constitutes the core of the Urban Technology Alliance, a working group created in Eclipse Foundation, which will bring together various worldwide stakeholders in the smart city domain.

**FESTIVAL at a glance**

**Project Coordinator**

CEA-Leti (FR), Osaka University (JP)

**Partners**

- **ES:** Santander Municipality, University of Cantabria
- **FR:** Easy Global Market, InnoTSD, Sopra Steria
- **IT:** Engineering Ingegneria Informatica Spa
- **JP:** ADUTUS, JCOMM, JRISS, Knowledge Capital, Kyoto Sangyo University, Osaka University, Ritsumeikan University

**Total budget**

€ 3 m.

€ 1.5 m. (+ 1.5 m. contribution from Japanese NICs)

**Contract Number**

643275

**Publications**


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**TRL**

1 2 3 4 5 6 7 8 9
GATEONE-project
Innovation Service for European Smaritization by SMEs

FREE EVALUATION PROGRAM OF DEMONSTRATORS for SME’s
The objective of gateone-project is to accelerate smart systems adoption by European SMEs in facilitating their access to advanced technologies for the development of innovative and smart solutions. GATEONE-project offers Innovation as a Service to the benefit of SMEs in structuring a complete and adapted innovation chain to:
- demonstrate to European SMEs the strength of smart system Key Enabling Technology to create sustainable differentiation on their market.
- Motivate SME’s engagement in radical and disruptive innovation in a techni-push approach to consolidate a business case.
- generate innovation opportunities for SMEs while reducing and managing their investment risk:
  - GATEONE-project enables state-of-the-art technology assessment by SMEs with free of charge demonstrators;
  - GATEONE-project ensures introduction to potential production partners when required.

GATEONE-project has the vision to make smart systems technologies accessible as solutions to non-expert SMEs: newcomers to invest in smart systems technologies, traditional European industries that are not familiar with smart systems or innovation.

GATEONE-project aims to position SMEs as key players of the European industry smartization to strengthen Europe competitiveness.

This innovation action aims to generate a structured dialogue through concrete collaborations between the research community (research centers and academics) and SMEs.

GATEONE-project contributes to define best practices at a Pan European level and a sustainable framework for RTOs and SMEs collaborations.

EC Programme
H2020 ICT-02-2014
Smart System Integration
https://cmetlab.ingenierie-sante.eu

Keywords
Demonstrator Innovation Internet of Things (IoT) Product innovation process RTO Smart system SME

GATEONE-project
Innovation Service for European Smaritization by SMEs

36 months
Jan. 2015 > Dec. 2017

GATEONE-project at a glance
Project Coordinator CEA-Leti (FR)
Partners

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<td>UK:</td>
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<td>FR:</td>
<td>Institut National de la Recherche Scientifique, CEA-Leti</td>
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<td>Blumorpho, LAAS- Centre National de la Recherche Scientifique, CEA-Leti</td>
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Total budget € 6.7 m.
EC Contribution € 5.4 m.
Contract Number 644856

OUTCOMES
Eight demonstrators have already been launched in conjunction with European SMEs and the following five have been developed and are being tested by SMEs:
- Secureloc: for Swiss SME ALRIDE is an autonomous localization system for the mountain rescue market - Product: backpack-integrated airbags - Usage case: airbag inflates in an avalanche and simultaneously activates the SECURELOC system, which transmits an audio message on the PMR446 radio wave standard;
- Autonomous Flowmeter: for French SME ITK. An autonomous agricultural flowmeter - Product: energy harvesting flowmeter for generating enough long-range communication power - Usage case: agricultural irrigation management and chemical, pharmaceutical and food industry process monitoring;
- Multi Sensor Wearable Device: a bracelet integrating sensors to monitor continuously chronic diseases based on reliable accelerometer, magnetometer, SpO2 level (HR delivery) and skin temperature measurements;
- Smart Soles: energy harvesting for Start-up R’Cup. A 3D printed insole; which uses only kinetic movement to create enough power for the device to measure and transmit step counting data; based on a holistic approach CEA-Leti has designed the energy transfer module and low-power architecture to provide various measurement features in a future product;
- Cassius: connecting boxing gloves for SMEs Sportcom, Internet Force 5 and Movolab. CEA-Leti’s broad IP in gesture recognition has enabled design a demonstrator of a brand new training approach. The institute very rapidly developed this glove-integrated functional demonstrator and the concept can now be demonstrated to users, while acquiring their feedback. This is the starting point for minimum viable product development. Three demonstrators are still under development and will be delivered to the SMEs for testing in 2017 and for potential development studies.

Publications
- “Wireless energy harvesters for autonomous wearables.”
- The smart boxing gloves demo will be showcased during the 5th CES event in Las Vegas.

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EC Programme

Keywords
Gas analyser
ICL-array
Mid infrared
QCL-array
Spectroscopy

Leti in iCspec

CEA-Leti has designed and realized integrated beam combiners for three different wavelength domains based on specifications agreed by the project partners:
- A specification dedicated to a continuous spectral domain around 6.8 μm.
- A specification dedicated to a monitoring system operating at 9 specific wavelengths around 3.4 μm.
- A more prospective specification dedicated to a broad spectral domain around 9 μm.

CEA-Leti is currently performing characterization and will soon deliver selected samples for prototyping. It has also developed, tested and delivered an ASIC capable of driving the QCL array and is currently developing a modified version of this ASIC for the ICL array.

iCspec

In-line Cascade laser spectrometer for process control

Real-time measurements of multi-components in process streams respond to long demanded industry requirements of fast, accurate, reliable and economical process analyzers. The rise of such -yet unavailable- systems will lead to a paradigm change throughout the process control and production chain. iCspec focus on the development of compact, robust and maintenance-free sensors for fast in-line multi-species chemical composition measurements for process analytics of many technically relevant gases such as hydrocarbons. The projected sensors will replace state-of-the-art systems of elevated cost and pollution. We will extend established laser-based in-line gas sensing to the mid-infrared “chemical fingerprint” spectral range for multi-species detection.

The developments base upon two key technologies: (1) The integration of mid-IR laser arrays and (2) the advancement of spectroscopic and chemometric data evaluation. Demonstrators will be integrated in the control loop of a petro-chemical plant allowing significant improvements as optimized product quality, minimized waste and thus less environmental pollution and increased safety in cases where hazardous conditions have to be detected without delay.

36 months
Apr. 2015 > Mar. 2018

iCspec at a glance

Project Coordinator
Siemens (GE)

Partners
FR: III-V Lab, CEA-Leti, Mirsense

Total budget
€ 5.5 m.
EC Contribution
€ 5.5 m.

Contract Number
636930

Publications
- “Integrated TDLs-Gassensor - from NIR to MIR”, A. Popescu, 6th Gassensor-Workshop, 9 Sept. 2015, Freiburg, Germany.
- “Mid-Infrared (~2.8 μm to ~7.1 μm) Interband Cascade Lasers”, S. Höfling, R. Weih, M. Dallner, J. Scheuermann, L. Naehle, M. Fischer, J. Koeth, M. Kamp, SPIE Optics + Photonics, 9 – 13 August 2015, San Diego, USA.

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TRL
1 2 3 4 5 6 7 8 9
InDeal
Innovative Technology for District Heating and Cooling

Challenged by climate change, and coupled with the need to secure sustainable economic growth and social cohesion, Europe must achieve a genuine energy revolution to reverse present-day unsustainable trends and live up to the ambitious policy expectations. A rational, consistent and far-sighted approach to heating and cooling is key for ensuring such transformation. Toward this direction, district heating and cooling systems need to be more efficient, intelligent and cheaper. InDeal project will offer an innovative platform that will impose a fairly distribution of heating and cooling among the network’s buildings by: (i) real-time energy consumption data gathering via artificial intelligent meters, (ii) identifying and evaluating the network’s buildings’ need and demand for heating and cooling depending to their energy efficiency, energy consumption and type of building (EDP tool), (iii) predicting the short-term and long-term weather conditions and forthcoming need for heating and cooling (EDP tool), (iv) monitoring and control the level of energy stored in network’s storage stations and substations (SMT), (v) 24/7 monitoring of the DHC system by a central control platform and (vi) minimizing heat losses via novel pipe design solutions and innovative insulation materials. The target of InDeal is to turn the current DHCS into a new next-level automated DHCS that will guarantee the increase of the overall energy efficiency of the system accomplishing a fairly distribution of heating and cooling energy demands. In light of this, InDeal will make a significant step forward contributing to wider use of intelligent district heating and cooling systems and integration of renewables, waste and storage.

Leti in InDeal

CEA-Leti’s main contribution to InDeal is development of energy harvesting solutions to supply in-line intelligent water meters. Water flow and thermal energy harvesting will be evaluated. Energy harvesters enable flow meters to operate for years without human intervention to replace their batteries. This supports eco-design principles since it limits the quantity of batteries thrown away.

Water flow energy harvesters are based on micro-turbines (cm²) capable of operating at mL/s or L/min to comply with the compatibility requirements of building environments. The micro-turbines will be designed and optimized for this application. Industrialization opportunities will be qualified. Water flow energy harvesters will be tested in District Heating and Cooling System (DHCS) water pipes. The power management circuit, which converts the raw AC (Alternating Current) output power of microturbines into a viable DC (Direct Current) supply source for Wireless Sensor Nodes, will be designed and optimized for maximum micro-turbine conversion efficiency with respect to water flows. The thermal energy harvesters will be based around Seebeck units controlled by efficient power management circuits capable of operating down to 50-100mV. The energy harvesters with their power management circuits will be supply sources that are compatible with sensor, microcontroller and Radio Frequency (RF) chip requirements.

InDeal at a glance

- Project Coordinator
  City University (GB)

- Partners
  CY: CETRI
  ES: CEMITEC
  FR: Leti
  FR: CEA, SNCU
  GB: City University
  GR: CERTH
  PL: Inzab, Promar
  SI: Energetika

- Total budget
  € 2 m.
  EC Contribution
  € 2 m.

- Contract Number
  696174
IoF 2020
Internet of Food & Farm

The IoF2020 project is dedicated to accelerate adoption of IoT for securing sufficient, safe and healthy food and to strengthen competitive-ness of farming and food chains in Europe. It will consolidate Europe’s leading position in the global IoT industry by fostering a symbiotic eco-system of farmers, food industry, technology providers and research institutes. The heart of the project is formed by 19 use cases grouped in 5 trials with end users from the Arable, Dairy, Fruits, Vegetables and Meat verticals and IoT integrators that will demonstrate the business case of innovative IoT solutions for a large number of application areas. A lean multiactor approach focusing on user acceptability, stakeholder engagement and sustainable business models will boost technology and market readiness levels and bring end user adoption to the next stage. This development will be enhanced by an open IoT architecture and infrastructure of reusable components based on existing standards and a security and privacy framework. Anticipating vast technologi-cal developments and emerging challenges for farming and food, the 4-year project stays agile through dynamic budgeting and adaptive decision-making by an implementation board of representatives from key user organizations. A 6 M€ mid-term open call will allow for tes-ting intermediate results and extending the project with technical so-lutions and test sites. A coherent dissemination strategy for use case products and project learnings supported by leading user organizations will ensure a high market visibility and an increased learning curve. Thus IoF2020 will pave the way for data-driven farming, autonomous operations, virtual food chains and personalized nutrition for European citizens. In brief, the main objective of the IoF2020 Large-Scale-Pilot is to foster take-up of IoT in the European farming and food domain by demonstrating the business case of IoT for a large number of application areas in farming and food; integrating and reuse available IoT technologies by exploiting open architectures and standards; ensuring user acceptability of IoT solutions in farming and food by addressing user needs, including security, privacy and trust; ensuring the sustainability of IoT solutions beyond the project by validating the related business models and setting up an IoT Ecosystem for large scale take-up.

IoF 2020 at a glance

- **Project Coordinator:** Wageningen University and Research
- **Partners:** [IoF partners](http://www.iоф2020.eu/about/partners)
- **CEA-Leti** is mainly involved in Wine optimization use case in Bordeaux with the partners:
  - Bordeaux INP - IMS Laboratory
  - Denis Dubourdieu Domaines
  - ISVEA
  - STMicroelectronics
  - Vinidea

- **Total budget:** € 30 m.
- **EC Contribution:** € 30 m.
- **Contract Number:** 731884

CEA-Leti is providing its IoT data collection and processing platform, sensiNact, which allows building interoperable services and applications in the smart farming domain. sensiNact is an open platform which is result of several European projects such as BUTLER, ClouT, OrganiCity and FESTIVAL and already validated in various application scenarios within those projects. The IoF2020 project gives the opportunity to validate this European platform in the smart farming domain with a large scale deployment. CEA will be one of the main promoters of the project achievements to its industrial partners and to its other ongoing and future IoT and smart farming related projects.

CEA-Leti is in particular involved in the wine optimization process use case, which utilises IoT technology to monitor accurate weather conditions in real time, vine conditions (such as grape detection, phenological stages determination, and disease status characterisation) and key cellar conditions, thereby demonstrating the potential benefits of these new cultivation methods.

sensiNact platform will be used in the use case to aggregate data coming from IoT devices deployed in 5 vineyards and 4 wineries in the area of Bordeaux, France. A wide variety of physical devices, equipped with LORA connectivity, will be connected to sensiNact. The list of devices includes weather stations, temperature and humidity devices, water flow and energy consumption devices. sensiNact will provide an easy monitoring of the measurements, detection of emergency situation, etc. and will allow the exploitation of the collected data by the vineyard owner for better managing their resources.
Leti in LAB4MEMS II

The Lab4MEMS II project is an opportunity for the CEA-Leti to develop knowledge and skills in the field of Micro-Optical Electro Mechanical Systems (MOEMS) such as the micro mirror.

The outcomes of the Lab4MEMS II project contributed by CEA-Leti are:

- the opportunity to develop a MEMS micro mirror component based on CEA-Leti design and technology;
- developments allowing CEA-Leti to communicate on this subject (publications presented at international conferences), to be positioned and recognized as a major player in this area;
- the possibility of using an Electro Active Polymer as piezoelectric actuation material in a MOEMS component. The project has prompted development of a new technology capable of integrating this type of inexpensive, low temperature process material. For the CEA-Leti, this represents an opportunity for a new actuator material complementing its other actuator materials;
- device characterization is enabling assessment of Electro Active Polymer material potential;
- integration of Electro Active Polymer material into technologies allows links to be created and prompts future collaboration opportunities with Arkéma, the polymer material supplier;
- extended development of CEA-Leti’s piezoelectric actuator design skills by building of a Finite Element Method model;
- continued collaboration with STMicroelectronics (Italy), one of the major industrial stakeholders in the MEMS field;
- knowledge development opening the door to discussion with potential future partners in relation to possible future contracts.

Lab4MEMS II at a glance

Project Coordinator
Okmetic OY (FI)

Partners
AT: Besi Austria
BE: KLA-Tencor
FI: Aalto University, Murata Electronics OY, Okmetic OY, VTT, VTT Memfab
FR: Arkema, CEA-Leti
IT: CNR-IMM, IUNET, Politecnico di Milano, Politecnico di Torino, STMicroelectronics
MT: STMicroelectronics Malta, University of Malta
NO: Polewall AS, SINTEF
PL: ITE
RO: University Politehnica of Bucharest

Total budget
€ 23.7 m.
EC Contribution
€ 3.6 m.

Contract Number
ENIAC-621176-2

Lab4MEMS II
Micro-Optical MEMS, micro-mirrors and pico-projectors

Lab4MEMS II focuses on launching a pilot line for Micro-Opto-Electro-Mechanical Systems (MOEMS) that merge MEMS and Micro-optics to sense or manipulate optical signals. MOEMS technologies generally integrate mechanical, optical, and electrical systems. This particular project goes beyond traditional MEMS to develop a pilot line for next-generation MEMS devices augmented with such advanced technologies as piezoelectric or magnetic materials and 3D packaging. Lab4MEMS II also features the realization of demonstrators on the Pilot Line as a means of validating technology for miniaturization of critical optical systems using micro-optics, micromechanics, and microelectronics.

36 months
Nov. 2014 > Oct. 2017
MIRIFISENS
Mid InfraRed Innovative lasers For Improved SENsor of hazardous substances

The mid-infrared (MIR) region is emerging as the favourite wavelength band for a number of applications, including high sensitivity trace detection, chemical emission monitoring, process control, and biological sensing applications. An efficient way to get precise and reliable information is to rely on spectroscopic analysis and, among the existing technologies, Tunable Diode Laser Spectroscopy (TDLS) has been identified as the most attractive solution due to the unique adsorption spectrum of chemicals, allowing their unambiguous detection. In the MIR region, the availability of Quantum Cascade Lasers (QCL) covering a broad portion of the spectral range (MIR, 3-12μm), has recently pushed forward the commercialisation of TDLS-based detection units.

Further technology advancements are still needed in the TDLS and QCL domains, the crucial bottlenecks being the range of tuneability, the footprint, power consumption & wallplug efficiency. Besides high cost and poor versatility, these limitations set a barrier for the realisation of powerful versatile detection units. To address these issues, MIRIFISENS brings major technological advancements in the field of miniaturisation, process development, heterogeneous integration and co-integration of MEMS functionalities.

The project exploits state-of-the-art micro and nano-fabrication techniques. The major technologic achievements proposed address the issues of sensitivity & selectivity, multi-gas capabilities, compactness, efficiency and cost effectiveness as specified by a number of selected Safety & Security applications. These achievements have been tested and validated for these applications. MIRIFISENS will deliver a new class of sensors with superior tuneability, better portability and extended detection capabilities, changing radically the current landscape of MIR chemical sensing spectroscopy.

Leti in MIRIFISENS

Photometric platform
CEA-Leti has chosen to investigate an alternative approach to implementing the entire detection chain within a millimetric footprint through the use of commercial microphones. This photometric (PA) cell, called the miniPA, is a hybrid platform for validating, at laboratory bench level, the photometric model and design using commercial MEMS. Within the scope of miniPA platform development, Leti’s work has involved completing the entire detection chain by coupling the miniPA to a QCL and a dedicated readout circuit, called Mirific, developed in-house. The institute has implemented a 12-bit Lock-In Amplifier (LIA)-based readout circuit dedicated to Photo Acoustic gas sensors. This LIA is fully integrated since it embeds the low pass filter, the clock generation circuit and the 12-bit ADC. It has been implemented in 0.35μm CMOS technology, its power consumption is 1.3mW under 3.3V supply voltage and it achieves a 10μV/√Hz input referred noise. Measured readout circuit linearity is 1.7%.

Finally, CEA-Leti has built a complete functional chain for bench-based sub-ppm detection including the QCL source, the miniPA cell, the specific readout circuit and dedicated software. System integration has been performed thanks to the work of MirSense, a start-up that has decided to commercialize a detector based on these developments.

Development of QCL laser sources on Silicon
CEA-Leti has validated key steps such as molecular bonding of III-V quantum wells on Si and fabrication of the DFB grating and the ridge. This will enable QCL fabrication on 200mm Si to reach the production line, to curtail costs and to increase yield.

Publications

Jean-Guillaume Coutard, jean-guillaume.coutard@cea.fr

Laurent Fulbert, laurent.fulbert@cea.fr
**MIRPHAB**

**1. MIRPHAB at a glance**

- **Project Coordinator**: CEA-Leti (Fr)

**48 months**


**MIRPHAB** is a pilot line for prototyping and production of Mid-IR devices for the detection of chemicals in gas and liquids. MIRPHAB offers open access to design, prototyping and fabrication of miniaturized photonics devices.

The goal of MIRPHAB is to foster the emergence of new market segments for optical sensing by reducing the investment cost to access innovative MIR solutions. The main objectives of MIRPHAB are:

- to provide a reliable supply chain of mid-infrared (MIR) photonic components for companies including smaller SMEs already active in analytical MIR sensing;
- to facilitate access to innovative MIR solutions for companies (including SMEs) working in the field of analytical sensors by reducing investment costs by providing open access to already developed technologies for design and test;
- to attract new companies to the field of analytical sensors, aiming to integrate MIR sensors into their products.

**Key technology breakthrough & challenge:**

- **miniaturization at chip/package level** as a key leverage tool to add functionalities, improve performances & enforce standardization while reducing costs;
- **mix and match different technologies** on the same platform.

**Market potential:**

- deploy new products swiftly in the market - fast track of key technological achievements into high added value products;
- pave the way to large scale industrialization of Mid-IR spectroscopic sensing.

**Total budget**

€ 17.2 m.

**EC Contribution**

€ 13 m.

**Contract Number**

688265

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**Leti in MIRPHAB**

Different MIR multiplexer technologies are under development or in maturation at CEA-Leti for the 4.5μm to 12μm spectral range.

Based on SiGe gradient technology, new packages have been fabricated in view of developing MUX with various ranges:

- 2877-3037 cm⁻¹;
- 1440-1480 cm⁻¹;
- 1050-1250 cm⁻¹;
- 1050-1160 cm⁻¹.

Ge technology suitable for longer wavelengths was stabilized early in the year and two packages featuring AWG were developed in the ranges:

- 1050-1250 cm⁻¹;
- 1050-1160 cm⁻¹.

To facilitate device testing, CEA-Leti introduced a new technology for fabricating SiGe40-based grating couplers. This 4.5μm technology produces very low losses (0.3dB/cm); grating couplers were fabricated at the end of the process.

Development of integrated microphones for mini-phot acoustic gas sensors has been launched using an innovative design based on MNEMS technology and this has already been transferred to a company. A new process combining SiGe gradient waveguides and MNEMS is under development.

Brokerage activity has started with an open call.

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**EC Programme**

H2020 ICT-28-2015 - Cross-cutting ICT KETs

**Keywords**

- Chemical sensing
- Micro PhotoAcoustic cell (μPA cell)
- Mid infrared Photonics devices
- Quantum Cascade Lasers (QCLs)
- Spectroscopic

**Publications**

The first year of the NEREID project has been packed with dynamic, stimulating workshops and events that have brought together experts in a forum environment to exchange opinions on future directions in micro- and nanoelectronics-related fields. Careful monitoring and questioning of various user groups during these events revealed emerging trends in nanoelectronics. As a core partner of NEREID, CEA-Leti is heavily involved in several important sections of the NEREID roadmap, including nanoscale FET, outside system connectivity, smart sensing, smart energy and energy harvesting. CEA-Leti also has a secondary role in the remaining topics, which are equally important to shaping the future of nanoelectronics R&D in Europe.

A number of roadmapping exercise outcomes were announced with publication of the first public version of the roadmap in September 2017. We already note some important trends with respect to power semiconductors and III-V materials, for example. SiC and GaN materials and their growing significance for electrical mobility (electric vehicles) and solar energy (photovoltaic converters) are clearly making headway in the marketplace. At the same time, emerging technologies, such as GaN on Silicon, may take a market share if they arrive at the right time in the window of opportunity. Detailed forecasts of such issues are provided in the roadmap as a guidance for stakeholders in the field. Similarly, the implications of technology adoption for deploying the IOT are highlighted in the Smart Sensors section, in which special attention is given to European technologies and providers. The roadmap promises to be a valuable tool for any European nanoelectronics stakeholder active in the area of nanoelectronics.
PIEZOMAT

High Resolution fingerprint sensing with vertical Piezoelectric nanowire Matrices

Biometrics is part of our everyday lives and is bound to become increasingly widespread in our society, inherently of novel intensive smart-device-connected behaviors and networking activities which require enhanced security measures for identification (ID) protection. Forensic and civil identification as well as rigorous access control remain large segments of the biometrics market, whereas consumer identification applications, notably in terms of access to banking and health care, are emerging. Given the zero fault tolerance for these applications, manufacturers turn towards innovative solutions for fingerprint sensors which enable large area scanning on small volume terminals, with very high spatial resolution, using scalable and portable technologies and complying with governmental requirements.

The PiezoMAT concept is to design a new technology of fingerprint sensor based on a matrix of inter-connected piezoelectric nanowires (NWs). The direct consequence of integrating nano-objects rather than conventional microsystems is to diminish the size of individual pixels, which enables larger integration densities and thus higher spatial resolutions.

OUTCOMES:
> proposal of new, scalable, fingerprint sensor technology offering sufficient resolution to detect level 3 minutiae such as pores and ridge edges. This level of resolution reinforces considerably the reliability of fingerprint reading and enables security reinforcement regarding biometric identification, which is in ever greater use in society’s everyday activities;
> exploitation of multidisciplinary competences in nanoscale fabrication, characterization and integration in a constructive and efficient manner. This approach responds to the aim of ensuring the fastest possible industrial transfer of large scale production-compatible solutions;
> investigation of innovative bottom-up integration, which is unlimited to piezoelectric NWs and fingerprint sensors. Through successive technological development, PIEZOMAT addresses wider nanotechnology integration issues and aims to validate methodologies that open up immediate and longer term ICT innovation routes through further performance enhancement and functional diversity.

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TRL 1–2–3–4–5–6–7–8–9

Leti in PIEZOMAT

CEA-LETI’s contributions to the PIEZOMAT project embrace definition of different layouts to be adopted based on preliminary simulations and experimental results and taking into account the stringent requirements of industry-compatible nanowire matrix integration.

CEA-LETI has also developed a related chip process that is compatible with all the ensuing steps, performed at project partners’ facilities, to achieve a final device. The institute has also coordinated and ensured smooth project management and communication among partners.

Publications
Leti in SmartEES

SmartEES is the European acceleration program on flexible electronics. This acceleration program help innovative companies to access new markets and grow their business by integrating flexible electronics into products and services. It currently has more than 35 electronics flexible solutions to design your product (Design freedom #Function integration #Production agility).

Within the project, 20 experiments will take place by helping companies with this integration. SmartEES allows accessing up to 140 000 worth support. Experiments submission will take place at any time and will be evaluated after the following 5 cut-off dates (March ’18; July ’18; Nov. ’18; Apr. ’19; Sept. ’19).

The main Services & Benefits of SmartEES are:

- dedicated team of technical experts and business managers;
- access to financial resources and investors;
- unique European Digital Innovation Hub on Large Area Electronics.

In this framework, CEA-Leti’s contribution will focus on providing electronics flexible solutions based on sensing matrices, low-power sensing platform, compatible energy harvesting devices... CEA-Leti, together with all the involved RTOs will support SMEs and mid-caps from all over Europe to submit experiments making use of these solutions. CEA-Leti will also be involved in the networking activities and sustainability development of the SmartEES Digital Innovation Hub.

SmartEES is part of the Smart Anything Everywhere initiative together with 3 other projects: FED4SAE (CEA-Leti’s coordination), Tetramax, Diatomics.

![SmartEES logo](https://example.com/smartees-logo)

**EC Programme**
Horizon 2020 - ICT-04-2017 - Smart Anything Everywhere Initiative

**Keywords**
Competence centre
Digital innovation hubs
Flexible electronics
Large area electronics
SME

**36 months**

**SmartEES at a glance**

- **Project Coordinator**
  - CEA-Liten (FR)

- **Partners**
  - BE: EBR, IMEC
  - CZ: AMIES
  - DE: Fraunhofer
  - ES: EURECAT
  - FR: BLUEMORPHO, CEA-Leti
  - FI: VTT
  - NL: TNO
  - UK: CPI

- **Total budget**
  - € 4.8 m.
- **EC Contribution**
  - € 4.5 m.

**Contract Number**
761496

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![EC programme logo](https://example.com/programme-logo)
TSV HANDY

Through Silicon Via Hvm AND Yield optimisation

TSV (Through Silicon Via) is a “More-than-Moore” technology that enables new chip architectures. Some challenges reside along the several steps of process to make TSV products cost efficient. The project aims at supporting the HVM ramp-up and improving the yield for manufacturing TSV products.

The challenges addressed in the project are:
- the handling of heterogeneous 300mm wafers with edge trim inspection;
- the development of metrology and new logistical concepts for wafers on 380mm frames;
- the improvement of temporary bonding and debonding processes.

Synergies will be created with other CATRENE projects like NGC450, SOI450, MASTER_3D.

The industrial partners intend to release new products to the market by early 2018.

CEA-Leti is a leader in process-related research.

Leti in TSV HANDY

CEA-Leti’s main TSV HANDY project task undertaken in 2016 was to modify the existing 300mm EVG560 bonder. Performed at EVG HQ, this operation involved adding a coating capability to the existing tool. EVG delivered the coater tool to CEA-Leti in August 2016. Bonding and coating capabilities of the new tool have been validated with a polymer adhesive. The quality of the bonding process has proven to be excellent and the resulting bonded stack has exhibited no fault (void or delamination). This has led to a robust process suitable for production. Moreover, the coating process is operational and provides an adhesive film without any air bubble or de-wetting areas. The bonding process obtained from this structure is also fault-free.

Another sub-task has involved selecting a high-performance temporary adhesive for use in the new EVG560 tool. To achieve this, CEA-Leti has designed a vehicle test and has identified a polymer adhesive compatible with high temperature processes. It has demonstrated that a structure bonded with the new adhesive exhibits no delamination up to 350°C, whereas a standard adhesive delaminates at 250°C. This compound is therefore highly promising especially for high temperature oxide deposition.

CEA-Leti launched the de-bonding process study in 2016. It first demonstrated that frame de-bonding of the new adhesive was possible and would ensure a crack- or chip-free dismounted wafer.

The institute is ready to supply various 300mm 3D wafers for RECIF and FOGALE in connection with designing and testing the new inspection tool.
Leti in ASCENT

CEA-Leti has played a pivotal role in establishing the starting community for nanoelectronic access to infrastructure. The protocols and procedures developed by CEA-Leti and its partners for implementation in ASCENT are now in place to help stimulate the nanoelectronics research community. These procedures allow for exchange of test vehicles, expertise and other research results with external teams of nanoelectronics experts in the quest for research excellence.

CEA-Leti is now providing access to test chips produced with the most advanced technology nodes based on FDSOI and nanowire technology. Stringent processing requirements governing nanoelectronics fabrication facilities at CEA-Leti make it possible to produce advanced test structures that enable studies of device variability and quantum effects for incredibly small geometries. Integration of novel ‘Beyond CMOS’ and ‘More than Moore’ technologies requires non-standard processing, for example to produce small-size nanowires. CEA-Leti also provides access to compact models, process design kits (PDKs) as well as characterization and electrical testing tools and data.

Many research groups from Europe and abroad have already made use of the ASCENT offer. The groups that access ASCENT are required to publish the results of their work, thereby further expanding the scientific impact of their discoveries. The expectation is that a successful network built around the infrastructures and activities of three major institutes will lead to long-term benefits for the entire European nanoelectronics research community and for industry.
COMPOSE3

Compound Semiconductors for 3D integration

COMPOSE3 develops 3D stacked circuits in the front end of line of Complementary Metal Oxide Semiconductor (CMOS) technology, based on high mobility channel materials. The final objective is a 3D stacked SRAM cell, designed with gates length taken from the 14nm technology node. This technology provides a new paradigm shift in density scaling combined with a dramatic increase in the power efficiency of CMOS circuits. Our synergetic approach is based on the use of high mobility channel materials such as SiGe and InGaAs, utilized in fully depleted metal-oxide-semiconductor field effect transistors (MOSFETs), for p and n channel MOSFETs respectively. The low processing temperatures (<600°C) that can be used for high mobility channels are indeed advantageous for an intimate 3D stacking. COMPOSE3 also exploits the knowledge accumulated in Europe for the processing temperatures (<600°C) that can be used for high mobility channels are indeed advantageous for an intimate 3D stacking. COMPOSE3 also exploits the knowledge accumulated in Europe for the fabrication of high mobility channels. The overall objectives of COMPOSE3 address the substrate, device and circuit issues. One objective is to validate InGaAs layer transfer for implementation on 300mm wafers. Another objective is to benchmark InGaAs nFETs with relevant contact layers on a pMOSFET with a 28nm gate length on a SiGe channel.

Leti in COMPOSE3

CEA-LETI’s main objective is to transfer a thin InGaAs layer onto fully processed 14nm MOSFET devices fabricated on 300mm wafers. In 2016, a milestone was achieved with full transfer of a thin film of In0.53Ga0.47As on 14nm MOSFET devices with an SiGe channel on 300mm wafers.

The SiGe MOSFET wafers have now been fabricated by STMicroelectronics on a 14nm process line. After fabrication, the wafers have undergone surface preparation using the CoolCube™ integration process flow developed at CEA-Leti. A series of deposition and polishing steps have been implemented to achieve a planar SiO2 surface, providing suitable topology for subsequent direct bonding.

The III-V layers have been epitaxially grown on a second 300mm Si wafer using an MOCVD tool at CEA-Leti. The process involves growing sacrificial buffer layers of GaAs (400nm) and InP (300nm) to compensate the crystal lattice mismatch between the Si and the InGaAs thin film (300nm). Al2O3 and a SiN/SiO2 bilayer are deposited to optimize electrical properties and bonding quality.

Direct bonding of the two wafers has been achieved by surface activation by polishing of the oxide layers and bringing the surfaces into contact. To reinforce this direct bonding, annealing annealing at 300 °C is applied for 1 hour. The Si substrate is then removed along with the III-V buffer, allowing access to the thin (30nm) InGaAs active layer. The Smart Cut™ process is then implemented to remove the Si wafer to transfer high quality InGaAs layers onto 300mm wafers for the first time.

The fabricated substrates have been forwarded to our partner IBM Zurich for continued integration of nFETs transistors on the active InGaAs layer to produce a 3D SRAM. CEA-LETI has therefore demonstrated state-of-the-art hybrid 3D “n-over-CMOS” with top InGaAs n-FinFets and bottom layer FDSOI Si CMOS with inter-layer contacts. Utilizing Functional 3D ST-GRAM with a denser packing than a 2D layout has been demonstrated using 3D device and interlayer stacking. This provides a robust 3D monolithic integration platform for high-mobility III-V materials and opens the door for dense digital circuits and functional integration of RF-over-Si CMOS.
Leti in EuroCPS

CEA-Leti is the project coordinator of EuroCPS project, in conjunction with project partners, it has successfully organized 3 open calls and an industrial experiment selection process. In total, 34 industrial experiments have been retained from more than 118 high quality applications. These 34 experiments are located in 11 different European countries, two of which are not directly represented by a EuroCPS partner. 80% of experiments are cross-border, which demonstrates the efficiency of the new EuroCPS cooperation model in initiating and boosting synergies between SMEs, major CPS platforms and CPS skills providers from different European countries.

In addition to its project coordination work, CEA achieved its objective of 7 selected industrial experiments split between CEA-Leti and CEA-List institutes. These experiments concern different technical fields ranging from new technological brick development (by facilitating access to FD-SOI technology) to system integration of different CPS domains including communication protocol, indoor localization, low-power sensing node, etc. The most advanced industrial experiments and the expertise and technological development for SMEs provided by the two CEA institutes bear witness to gains in SME competitiveness through early adoption of emerging technologies. Further collaborations (e.g. common laboratories) extending beyond EuroCPS are therefore expected. The high quality of industrial experimentation has prompted presentation of scientific publications at top ranking international conferences (e.g. ISSCC).

Within the scope of the EuroCPS project, CEA-leti and CEA-List are demonstrating their capacity to curtail SME innovation risk and reduce CPS development time.
Leti in EUROSERVER

The founding principle of EUROSERVER is to design of scale-out architecture, i.e. use of multiple simpler computing nodes. Integration of multiple cores in one package is therefore a critical issue. The project partners have considered three options to deal with integration: 1/ an active silicon interposer, 2/ a passive silicon interposer and 3/ an organic interposer. The organic interposer was selected in early 2015 and this decision is discussed and detailed in a memo entitled «Impact of Technology Change per partner» issued in June 2015.

During 2016, interest in chiplet commercialization increased dramatically and this led CEA-Leti and ST to analyze possibilities of EUROSERVER chiplet industrialization. This development roadmap called for additional design efforts to ensure that the compute node/chiplet was industrially viable (improved DFT, upgrade of high serial links, ROOM boot, lower power modes, security, etc.).

This meant that the commercialization objectives were not compatible with the EUROSERVER schedule/roadmap as defined in the Amendment 2 (July 2015). Amendment 3 was therefore drafted, submitted and accepted in April 2016. Its main features were non-availability of the HW prototype by ST and cancellation of all associated tasks (board integration specification, CEA-Leti development of RDMA, integration into organic interposer, scaling and structure of new package). These tasks were mainly managed by CEA-Leti and ST. During the early months of 2016, CEA-Leti and ST worked jointly to finalize tasks involving the integrated system design (mainly functional verification and routing) and this led to finalization of the SIP physical instance. Full co-design activities between the CEA-Leti design team and the ST package team started in 2015 and continued through 2016, focusing on full SIP feasibility analysis. The results of these tasks were detailed in two deliverables. As described in Amendment 3, the CEA-Leti task involves principally project coordination. 2016 saw the signing of a cooperation contract with start-up Kaleao in the domain of 3D advanced packaging for micro-servers.

With regard to the overall project, the “compute-node” board was manufactured in 2016 based on the design specification drafted in 2015. Board prototypes have been designed, manufactured and made available to EUROSERVER partners for running performance evaluation tests. The board prototype includes an SIP instance, a field-programmable gate array (FPGA) and usual components such as memory, network adapter, etc. Dedicated SW developments (memory compression, optimized memory management, Microvisor, OpenStack VM manager and VMs management, workloads, etc.) were undertaken in parallel. All developments were successfully ported on dedicated evaluation platforms enabling us to run successful performance evaluation tests and prepare an integrated demonstration for the final review in early 2017.
ExaNoDe
European Exascale Processor Memory Node Design

ExaNoDe will investigate, develop integrate and validate the building blocks (technology readiness level 5) for a highly efficient, highly integrated, multi-way, high-performance, heterogeneous compute element aimed towards exascale computing. It will build on multiple European initiatives for scalable computing, utilizing low-power processors and advanced nanotechnologies. ExaNoDe will draw heavily on the Unimem memory and system design paradigm defined within the EUROSERVER FP7 project, providing low-latency, high-bandwidth and resilient memory access, scalable to Exabyte levels. The ExaNoDe compute element aims towards exascale compute goals through:

- integration of the most advanced low-power processors and accelerators (across scalar, SIMD, GPGPU and FPGA processing elements) supported by research and innovation in the deployment of associated nanotechnologies and in the mechanical requirements to enable the development of a high-density, high-performance integrated compute element with advanced thermal characteristics and connectivity to the next generation of system interconnect and storage;
- undertaking essential research to ensure the ExaNoDe compute element provides necessary support of HPC applications including I/O and storage virtualization techniques, operating system and semantically aware runtime capabilities and PGAS, OpenMP and MPI paradigms;
- the development of a hardware emulation of interconnect to enable the evaluation of Unimem for the deployment of multiple compute elements and to leverage the potential of the ExaNoDe approach for HPC applications. Each aspect of ExaNoDe is aligned with the goals of the ETP4HPC. The work will be steered by first-hand experience and analysis of high-performance applications and their requirements; investigations being carried out with “miniapplication” abstractions and the tuning of their kernels.
Leti in MONT-BLANC2

Within the scope of the Mont-Blanc 2 project, CEA-Leti is involved in defining and analyzing the computing node architecture based on its experience in multicoresystem design and advanced technology integration. The main task consists in exploring different 3D integration solutions by taking into account technological, design and performance constraints. The contributions are focused on various aspects of:

- technology characterization (including 3D memories);
- 3D architecture exploration (including tools and methodology);
- hardware complexity evaluation for memory coherency support.

During the project, CEA-Leti has performed the following feasibility studies and architectural analyses to optimize selection of available technologies based on performance and cost constraints:

- integration specification of Hybrid Memory Cube (HMC) in an AMBA-based SoC;
- selection of chip-to-chip interconnection solutions within a integration context;
- performance estimation based on 3D physical exploration of different architectural options;
- physical floorplan of different partitioning options for computing node within a silicon interposer integration context;
- cost analysis for different computing node partitioning levels.

MONT-BLANC2 at a glance

- Project Coordinator
  Barcelona Supercomputing Center (ES)

- Partners
  DE: Bayerische Akademie der Wissenschaften, Forschungszentrum Jülich GmbH, Universität Stuttgart
  ES: Barcelona Supercomputing Center, Universidad de Cantabria
  FR: Bull SAS, CEA-Leti, CNRS, INRIA
  GB: Allinea Software Limited, ARM Limited, University of Bristol
  IT: Consorzio Interuniversitario Cineca

- Total budget
  € 11.4 m.
- EC Contribution
  € 8 m.
- Contract Number
  610402

MONT-BLANC2

European Scalable and Power Efficient
HPC Platform based on Low-Power
Embedded Technology

The Mont-Blanc2 project aims at developing a European Exascale approach leveraging on commodity power-efficient embedded technologies. The project has developed a HPC system software stack on ARM, and deployed the first integrated ARM-based HPC prototype in 2014, and is also working on a set of 11 scientific applications to be ported and tuned to the prototype system.

The Mont-Blanc 2 proposal has 4 objectives:

- to complement the effort on the Mont-Blanc system software stack, with emphasis on programmer tools (debugger, performance analysis), system resiliency (from applications to architecture support), and ARM 64-bit support;
- to produce a first definition of the Mont-Blanc Exascale architecture, exploring different alternatives for the compute node (from low-power mobile sockets to special-purpose high-end ARM chips), and its implications on the rest of the system;
- to track the evolution of ARM-based systems, deploying small cluster systems to test new processors that were not available for the original Mont-Blanc prototype (both mobile processors and ARM server chips);
- to provide continued support for the Mont-Blanc consortium, namely operations of the Mont-Blanc prototype, and hands-on support for our application developers.

MONT-BLANC2

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- to complement the effort on the Mont-Blanc system software stack, with emphasis on programmer tools (debugger, performance analysis), system resiliency (from applications to architecture support), and ARM 64-bit support;
- to produce a first definition of the Mont-Blanc Exascale architecture, exploring different alternatives for the compute node (from low-power mobile sockets to special-purpose high-end ARM chips), and its implications on the rest of the system;
- to track the evolution of ARM-based systems, deploying small cluster systems to test new processors that were not available for the original Mont-Blanc prototype (both mobile processors and ARM server chips);
- to provide continued support for the Mont-Blanc consortium, namely operations of the Mont-Blanc prototype, and hands-on support for our application developers.
Leti in MONT-BLANC2020

CEA (CEA-Leti and CEA-List institutes) will refine its expertise for memory and chip-to-chip interconnects, and gain new experience in data intensive compute subsystems with associated design methodologies related to verification with an emulation platform. CEA will gain expertise in interposer-based design, low-power IPs and power management strategy for such sub-systems. CEA, by exploring in M2020 methodologies enabling a better time-predictability for mixed-critical applications will also get a strategic position on the processor for other future markets like the autonomous vehicle. MB2020 results will therefore help CEA in its willingness to actively build an industrial ecosystem around these two key markets and pave the way for future technology transfers. CEA-Leti will mainly participate to the subject «Low Power HPC SoC design and implementation» working on these different tasks: T55: «Low power source synchronous digital PHY with integrated calibration for 3D short range links», our team has developed a digital Physical Layer (PHY) in 28nm Fully-Depleted Silicon-On-Insulator (FDSOI) technology for short range links on passive/active interposers and for 3D connections. This PHY is based on a source synchronous propagation with credit based link layer. This PHY has tunable timings however it lacks calibration of these timings and relies on trial and error. CEA will strengthen the PHY IP with a 22nm technology node. It will make it possible back-end netlist simulation required for improving the IP with the integration of an innovative solution for the auto-calibration of timing knobs. In addition, this back-end implementation will allow precise PPA in 22nm node and estimated PPA for 7nm. T56: «Global Power Management», CEA’s contribution in MB2020 is to study the integration of power tree in a 3D context. Rely on dedicated layers that integrate the bulky power supply components, the overall power density of on-chip power management may be greatly increased. The multi-core context of MB2020 is unique opportunity to apply system- to circuit-level analysis based on partners’ exchanges. This study paves the way to fully integrate the power management in a SoC context and allows a finely-grained power strategy for high-density and low-power computation. A report on the system-level and topology choice of the power tree including quantified achievable power density, best interposer technology choice and power supplies topology based on MB2020 multi-core digital processor. T57: «Clock generator with IR-drop detection and prevention», CEA will develop a clock generator based on a Frequency Locked Loop (PLL) with IR-drop detection and prevention capabilities. The clock generator will be able to monitor the compliance of the clock frequency with the actual circuit voltage to detect any circuit failures resulting from IR-drops. When an IR-drop is detected, the clock frequency will be automatically reduced to avoid the failure. To achieve this, CEA will develop a clock generator based on a low-power design with IR-drop detection and prevention capabilities. The clock generator will be able to monitor the compliance of the clock frequency with the actual circuit voltage to detect any circuit failures resulting from IR-drops. When an IR-drop is detected, the clock frequency will be automatically reduced to avoid the failure. The Mont-Blanc 2020 (MB2020) project ambitions to initiate the development of a future low-power European processor for Exascale. MB2020 lays the foundation for a European consortium aiming at delivering a processor with great energy efficiency for HPC and server workloads. A first generation product is scheduled in the 2020 time frame. Our target is to reach exascale-level power efficiency (50 Gflops/Watt at processor level) with a second generation planned for 2022. Therefore, we will, within MB2020:

- define a low-power System-on-Chip (SoC) implementation targeting Exascale, with built-in security and reliability features;
- introduce strong innovations to improve efficiency with real-life applications and to outperform competition (vector instruction implementation, memory latency and bandwidth, power management, 2.5D integration);
- develop key modules (IPs) needed for this implementation;
- provide a working prototype demonstrating MB2020 key components and system-level simulations, with a co-design approach based on real-life applications;
- explore the reuse of these building blocks to serve other markets than HPC.

Our key choices are:

- to use the ARM ISA (Instruction Set Architecture) because its has strong technological relevance and it offers a dynamic ecosystem, which is needed to deliver the system software and applications mandatory for successful market acceptance;
- to design, implement or leverage new technologies (Scalable Vector Extension, NoC, High Bandwidth Memory, Power Management,…) as well as innovative packaging technologies to improve the versatility, performance, power efficiency, reliability, and security of the processor;
- to improve on the economic sustainability of processor development through a modular design that allows to retarget our SoC for different markets.
Let in MOS-QUITO

Significant progress has been made in the design, fabrication and testing of the first batch of devices fabricated at CEA-Leti in NanoWire CMOS technology on 300nm diameter SOI wafers. This is a step towards implementing CMOS-based spin qubits in silicon. The first 300nm SOI samples were fully processed during the overlap period with the F77 project SIAM. The batches contained a variety of devices with dense gates, which were suitable for electrical characterization at low temperature within the MOS-QUITO project scope.

Morphology, critical thicknesses and lateral dimensions were monitored and documented during fabrication. The technical splits most likely to work for MOS-QUITO were confirmed on that basis. A few potential design and integration issues were identified and corrected in the following design iteration, which provided the mask set dedicated to MOS-QUITO. This would be used on the second 300mm SOI batch.

A systematic testing protocol at 300K was implemented to identify potentially interesting “Split Gate” and “pump” devices prior to forwarding them to project consortium members. A database was generated to document the electrical behaviour of each device from each EBeam die on each wafer. Once the project partners had identified their technical splits of interest, a few (typically 2-3) EBeam dies from each wafer were forwarded, along with a description file containing the floorplan, pad assignment, device geometry, device dimensions, list of functional devices, test protocol and an archive containing screenshots of 300K I-V measurements. This procedure has assisted the partners in minimizing time spent looking for adequately functioning devices.

MOS-QUITO

MOS-based Quantum Information Technology

Quantum computing is now widely regarded by many in academia, governments and industry to represent a major new frontier in information technology with the potential for a disruptive impact. Many different materials and approaches have been explored, with a narrowing of focus in recent years on scalable implementations based on solid state platforms. In particular, there is now strong evidence that silicon, the primary platform technology for today’s processor technology, inherently possesses many key properties that make it advantageous for quantum computing. Two types of qubit based on spins in silicon nano-devices made in academic research labs have already been reported with demonstrated high-fidelity operation. Our project builds on this success to take this technology to the next readiness level by showing that silicon-based qubits can be realised within a full CMOS platform, using the 300nm-scale fabrication facilities in our consortium. In doing so we demonstrate the true potential of silicon based qubits in terms of scalability and manufacturability.

Our focus is on distilling the silicon device design down to the simplest core element necessary to demonstrate qubit behaviour, in order to lay the foundation for a scalable technology. We design, model and fabricate these qubit devices, and then benchmark them using key operating parameters. Our attention is not limited at the lowest level technology layer where the qubits reside, and includes higher control layers necessary to operate such devices, including demonstrating strategies for achieving local control and readout in large-scale arrays without cross-talk and developing cryo-CMOS electronics to support the qubit operation. Both of these may be spin-out and yield their own technological impacts. Thus, our holistic approach offers a wider opportunity to harness the tremendous proven capabilities of integrated CMOS technology to become a key driver of quantum technology development.
NEURAM3
NEUral computing architectures in Advanced Monolithic 3D-VLSI nano-technologies

Neuram3 is fabricating a chip implementing a neuromorphic architecture that supports state-of-the-art machine learning algorithms and spike-based learning mechanisms. With respect to its physical architecture, the chip features an ultra low power, scalable and highly configurable neural architecture that will deliver a gain of a factor 50x in power consumption on selected applications compared to conventional digital solutions; and a monolithically integrated 3D technology in Fully-Depleted Silicon on Insulator (FDSOI) at 28nm design rules with integrated Resistive Random Access Memory (RRAM) synaptic elements.

In complement to this vision, complementary technologies are developed that address the full spectrum of applications from mobile/autonomous objects to high performance computing coprocessing, by developing processing, delivering: an ultra-low power massively parallel non von Neumann computing platform with non-volatile nano-scale devices that support on-line learning mechanisms; a programming toolbox of algorithms and data structures tailored to the specific constraints and opportunities of the physical architecture; an array of fundamental application demonstrations instantiating the basic classes of signal processing tasks. The neural chip validates the concept and be a first step to develop a European technology platform addressing from ultra-low power data processing in autonomous systems (Internet of Things) to energy efficient large data processing in servers and networks.

NEURAM3 at a glance

- Project Coordinator: CEA-Leti (FR)
- Total Budget: € 4.2 m.
- EC Contribution: € 3.2 m.
- Contract Number: 687299

36 months
Jan. 2016 > Dec. 2018

NEURAM3 NEUral computing architectures in Advanced Monolithic 3D-VLSI nano-technologies

Leti in NEURAM3

At present, most dedicated hardware designs for neuro-computing rely exclusively on conventional digital CMOS technology and consequently require complex circuits and a large silicon area. Furthermore, energy efficiency remains a major challenge in these systems. It is difficult to push scaling further to increase high-density integration. While silicon neuron functionality can be implemented by CMOS circuits, it is not straightforward to emulate the synaptic function on silicon-based devices without using a complex circuit. Since neural networks typically need many more synapses that neurons (approximately 1000 to 10000 synapses per neuron), synapse circuit design primarily limits practical implementation of hardware neural systems. Introduction of a compact nanoelectronic device emulating the function and plasticity of biological synapses in neuromorphic hardware architecture can significantly improve the density and, possibly, the power consumption of conventional CMOS implementations of neural computing. Among proposed candidates for the fabrication of hardware mimicking synaptic functionality, resistance change memory devices (RRAM) that exploit resistance switching (RS) phenomena are very attractive because of their compatibility with CMOS technology and potential scalability down to 10nm or below.

In this context, CEA-Leti has worked on two approaches. On one hand, it has developed the Memory Advanced Demonstrator (MAD) test vehicle based on 130nm CMOS technology and HP32 based RRAM memories. This test vehicle has allowed the NeuRAM3 partners (ETH and CSG) to implement innovative neuromorphic circuits using CEA-Leti RRAM technology to implement the synaptic connections. The ETH contribution to MAD involves implementing CMOS circuits that interface an array of 1024 RRAM based synapses to two neurons. The CSC contribution to MAD is a spike-based algorithm with 1T1R resistive memory.

CEA-Leti has also investigated implementation of new functionalities in the baseline processes and, in particular, different forms of plasticity in the synaptic element. The institute has proposed an architecture, which implements both Spike-Timing-Dependent Plasticity (STDP) and Synaptic Adaptation (a type of Short Term Plasticity). Furthermore, CEA-Leti has shown that Long Term STDP allows the neural network to learn patterns without a training data set. Furthermore, CEA-Leti has also investigated implementation of new functionalities in the baseline processes and, in particular, different forms of plasticity in the synaptic element. The institute has proposed an architecture, which implements both Spike-Timing-Dependent Plasticity (STDP) and Synaptic Adaptation (a type of Short Term Plasticity). Furthermore, CEA-Leti has shown that Long Term STDP allows the neural network to learn patterns without a training data set and Short Term Synaptic Adaptation makes the learning process very robust to background noise in the input data.

Publications:

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Embroided memory resistance RRAM cell scanning electron microscope showing positionings between metal 4 and metal 5 circuit schematic and measurements of Set and Reset states.
Leti in PANACHE

Within the scope of the PANACHE project, CEA-Leti has been developing and transferring competitive innovative memory solutions, handling critical developments and solving problems and completion times related to direct introduction of new materials in 200nm and 300nm industrial pilot lines.

To develop an optimized memory stack and accelerate adoption of these new technologies, CEA-Leti has developed the so-called Memory Advanced Demonstrator (MAD), today based on 130nm ground rules with 4 copper metal lines. The memory module, which can feature PCM, OxRAM, CBAM or MRAM technology, is fabricated in the BEOL before pad level. This versatile test vehicle offers the possibility of integrating into the same silicon test structures, simple resistors (1R), resistors with selector transistors (1T1R), memory arrays (1Mb cuts) and complex designs implementing routing placement on 4 metal levels. Complex designs of this type may be developed by client designers using a 2K plus memory add-on provided by CEA-Leti.

All these structures are essential for in-depth analysis of memory functionality from bulk material (with its interfaces) screening obtained by the 1R and 1T1R, through statistical analysis of extrinsic bits obtained by memory arrays to first validation of complex functions obtained by specific designs.

The PANACHE MAD offers a benchmark opportunity to utilize the same test vehicle to extract individual advantages and drawbacks from different technologies. After investigating the best memory solution in 200mm using the MAD, CEA-Leti offers the move to 300mm by exporting the memory module on the project partner base wafers with aggressive nodes. The last step is typically achieved through wafer exchange: the partner’s (or the foundry stakeholder’s) incoming wafers implementing the appropriate CMOS process and number of metal lines are sent to CEA-Leti for plugging the optimized memory module. After processing, the wafers are returned to the partner (or foundry stakeholder) clean room for BEOL completion. Prior to this stage, CEA-Leti expertise is used to modify the client design kit and add the appropriate add-on kit required for successful integration.

Within this value chain, MAD offers CEA-Leti partners the chance to ramp up both technology and design maturity; both condition closely the success of each disruptive technology industrialization.

PANACHE
Pilot line for Advanced Nonvolatile memory technologies for Automotive Micro-Controllers, High security applications and general Electronics

PANACHE is the ENIAC KET Pilot Line project addressing design technologies and semiconductor process and integration.

The primary objective is to set-up a pilot line for embedded Flash technology design and manufacturing for the prototyping of innovative microcontrollers in Europe. The already defined 28nm technology platform will be developed and consolidated in order to provide a solid base for extension to 40nm technology.

The contributions from a strong consortium will build a solid manufacturing platform on these technology nodes. The project will also provide pathfinding activities to extend the basic building blocks of the technology to achieve a prototyping maturity for a new BEOL based non-volatile memory architecture suitable with the 28 nm node.

To achieve this goal of generating high value added semiconductor circuits in Europe in a breakthrough leading edge technology the project will deploy all the necessary activities to bring a new technology to an early industrial maturity stage. These activities encompass technology enhancements for specific application requirements such as wide temperature range and reliability, high security, high flexibility, design enablement allowing first time silicon success, and prototyping of demonstrator products in the targeted application areas: Automotive, Consumer/Industrial and Secure Devices.

48 months

PANACHE at a glance

Project Coordinator
STMicroelectronics (FR)

Partners
FR: STMicroelectronics Grenoble, STMicroelectronics Le Mans,
CEA-Leti, Gemalto SA, Thales Communication & Security SAS
CNRS-LTM, Adixen
DE: Robert Bosch GmbH, IPH
Leibniz, TU Darmstadt
BE: ASM Belgium
IT: STMicroelectronics
FR: ASM Microchemistry Dy
IE: Institute of Microelectronic Applications, Ltd., Institute of Information Theory and Automation of the AS CR
ES: Universitat Autonoma de Barcelona
DK: TUB/IK, Sabanci University, Inovent Coop
IL: Livel Ltd.

Total budget
€ 224.7 m.
EC Contribution
€ 33.7 m.

Contract Number
ENIAC-621217

Publications
- “Fundamental Variability Limits of Planar-based RRAM”, A. Grossi,
F. Nowak, C. Zambelli, C. Pellissier, S. Bernasconi, G. Obrad, A. Grossi,
C. Zambelli, C. Pellissier,
- “Understanding RRAM endurance, retention and window margin trade-off using experimental results and simulations”, C. Nal, G. Obrad,
- “Data Retention Extractions Methodology for perpendicular STT-MRAM”, L. Teli, E. Novak, R. C. Souza, M. C. Cyriko, B. Delat,
T. Majza, A. Perinola, J. Langer,
- “Experimental demonstration of short and long term synaptic plasticity using OxRAM multi k-bit arrays for reliable detection in highly noisy input data”, T. Werner,
E. Vianello, O. Berton, A. Grossi,
F. Novak, J. F. Rodin, B. Yvert,
- “Understanding RRAM endurance, retention and window margin trade-off using experimental results and simulations”, C. Nal, G. Obrad,

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Leti in REMINDER

During the Year 1 of the REMINDER project, CEA-Leti achieved results in four research topics: technology, electrical characterization, simulation and modeling.

In technology, based on inputs from UGR, IMPE and LAHC laboratories, process flows of three candidate technologies (MSDRAM, A2RAM and Z²-RAM) were analyzed and compared. The only 1T-DRAM structure fully compatible with the standard 28FDSS0 route is the Z²-RAM, this motivated selection of Z²-RAM for the project. No technology specific developments are required at CEA-Leti for the 3 planned runs. In electrical characterization, CEA-Leti delivered A2RAM wafers to Granada University for performing electrical investigations of gate stack properties on SiGe channels for different Ge content. SiGe channels will propel 28FDSS0 towards new performance levels with an eye to longer term studies (3D non-planar architectures).

In simulation, STMicroelectronics/CEA-Leti research collaboration provided the REMINDER project consortium with calibrated 28FDSS0 TCAD deck usable for 1T-DRAM applications, this is calibrated on the electrical performance of 28FDSS0 technology. CEA-Leti also developed and provided a TCAD simulation deck of a A2RAM cell, enabling main technological parameter variation such as body thickness, bridge thickness, gate length, gate oxide thickness and doping. This deck centers the electrical behavior of A2RAM cell and evaluates the range of polarization to use in transient TCAD simulations. In selecting the best 1T-DRAM structure, TCAD simulations were required to assess the optimum performance achievable for each structure (MSDRAM, A2RAM and Z²-RAM). CEA-Leti focused on A2RAM and performed extensive A2RAM TCAD simulations, while varying not only the main technological parameters, but also the operating polarizations. The institute also contributed an evaluation of the best performance trade-off achievable by A2RAM structures.

In modeling, CEA-Leti was to provide an analytical model of DC operation of the selected 1T-DRAM structure. For Z²-RAM, the behavior of this device was insufficiently understood for building this analytical model. The first step was to perform an extensive simulation study to understand device behavior. In a close collaboration with IMPE, CEA-Leti contributed to the project an in-depth understanding of Z²-FET DC operation including the four operating regimes of Z²-RAM, a physical explanation of DC hysteresis and guidelines for TCAD simulations applied to compact model development. CEA-Leti’s analytical model of Z²-FET DC operation will form the basis for Z²-FET compact model development required in the remainder of the project.
Leti in SIAM

CEA-Leti is contributing to the SIAM project the advanced silicon design and water processing expertise required for producing various types of atomic scale devices. In the first device configuration, the institute has focused on developing a wafer level integration flow to investigate a mixed SOI-CMOS/STM device fabricated on Si:H surfaces. The team has developed an integration flow and a dedicated system for connecting electrically atomic scale devices to microscale pads for further integration of such devices within other circuit electrical functions or for automated electrical testing. Base devices with sources and drains were prepared at CEA-Leti before integration of atomic nanowires by Scanning Transmission Microscopy (STM) at IBM. The wafers were then cleaned and re-integrated into the CEA-Leti CMOS line to produce gate structures by e-beam lithography, while interconnects were created by a complex chip-to-wafer bonding process. Following final electrical characterization, this integration flow has been successfully proven on test chips fabricated by IBM and CEA-Leti.

Another set of investigated devices comprises multi-gate silicon-on-insulator (SOI) nanowire devices for electron pumps and single/coupled-atom transistors with a 65nm gate pitch. During the project, a wide range of devices has been fabricated including two, three and even four gates in series in N- and P-FET devices. The SIAM multi-gate samples have yielded results for electron pumping and its associated theory. These results have enabled the CEA-Leti team to demonstrate the first hole spin qubit as well as the first (real) CMOS spin qubit. These results are only briefly mentioned here since qubit measurement and its physics are reported in the Si-SPIN FET-OPEN project also coordinated by CEA. It should be emphasized that SIAM project remains, to date, the one and only “supplier” of such samples and this has given rise to a new mask-set to be developed within the H2020 MOS-QUITO project, which started in 2016.

SIAM at a glance

- Project Coordinator
  CEA INAC (FR)

- Partners
  CH: IBM Research
  DE: Physikalisch-Technische Bundesanstalt
  FR: CEA-Leti
  LV: Latvijas Universitate
  NL: Universiteit Twente

- Total budget
  € 2.9 m.
  EC Contribution
  € 2 m.

- Contract Number
  INFSO ICT-610637

- Publications
  - “Development of a CMOS Route for Electron Pumps to Be Used in Quantum Metrology”, S. Barraud et al., Technologies 2016, 4, 10, available (open access) at http://dx.doi.org/10.3390/technolo-
    gies4010010.
    dx.doi.org/10.1103/PhysRevAp-
    plied.4.044009.

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EC Programme
ICT-2013.9.7 - FET Proactive:
Atomic and Molecular Scale Devices and Systems

Keywords
Nanowire Quantum

SIAM
Silicon at the Atomic and Molecular scale

The SIAM project investigates the fundamental properties of devices with single dopant atoms. Single atomic devices could have a profound impact on future device architectures which take advantage of their distinct quantum behavior. The key idea is to use the very sharp, deep and reproducible potential created by a dopant in a semiconductor host crystal. Despite its small size (on the scale of the Bohr radius), the dopant state of a single dopant can be addressed with conventional lithography techniques, and is therefore perfectly suitable for realistic devices exploiting the quantum nature of single atoms.
SISPIN
Silicon Platform for Quantum Spintronics

Quantum spintronics uses the quantum nature of individual spins to bring new functionalities into logic circuits, either for more efficient information processing or through spin-based quantum algorithms. This project investigates new directions based on p-type SiGe nanostuctures. This system has the unique combination of low hyperfine and strong spin-orbit couplings. Aside from developing demonstrator devices such as spin-filters or single spin qubits, we aim at exploiting recently proposed schemes for long range spin-spin coupling, an essential requirement for scalable qubit circuits.

Keywords
Quantum

SISPIN at a glance

Project Coordinator
CEA-INAC (FR)

Partners
AT: University of Linz
CH: IBM Zurich, University of Basel
DK: University of Copenhagen
FR: CEA-Leti
NL: TU Delft

Total budget
€ 4.3 m.
EC Contribution
€ 3.7 m.

Contract Number
ICT-323841

36 months

Leti in SISPIN

Recent breakthroughs in silicon spin quantum bits provide a truly CMOS-compatible route towards scalable, integrated qubits. A first step towards this goal has been made using silicon-on-insulator (SOI) nanowire transistors featuring two closely spaced gates parallel to each other. This configuration results in two coupled quantum dots (QDs) in series, in which each QD can be operated down to the few electron regime by adjusting the voltages applied to the corresponding top gate and to the global back gate provided by the silicon substrate. We have observed signatures of Pauli spin blockade (PSB) in different electronic configurations and for different values of the singlet-triplet splitting. The PSB regime has been studied as a function of the external magnetic field applied perpendicular to the chip plane. Since PSB is a commonly used mechanism for spin-qubit readout, our work is relevant to producing CMOS-based qubits.

CEA-Leti has implemented SiGe (Silicon Germanium On Insulator) for nanowire transistors and quantum dots using a 300-mm state-of-the-art CMOS foundry. The Ge content in these structures was initially limited to 30% as imposed by the available technology. For this Ge content, the current Si technology at CEA-Leti is compatible with SiGe materials. We could therefore fabricate not only innovative SiGe based nanomaterials, but also MOSFET devices built on these SiGe patterns. We have demonstrated single quantum well and superlattice core/shell nanowire SiGe30% transistors with high-K dielectrics and a metal gate sized down to 15nm gate length. CEA-Leti has investigated different options for increasing the Ge content in SiGe-based nanostructures to well above 30%. New methods for fabricating SiGe-based nanostructures with a larger Ge content (Ge>30%) have been developed. We have tested and validated an innovative process sequence for fabricating SiGe nanomaterials using a top-down approach on 300nm SOI substrates. The morphological characterization (STEM, EDX) confirms that the Ge content in the 9nmx 28nm SiGe nanowire is as high as 60% with a uniform Ge concentration within the patterns and excellent crystal quality.

Several SISPIN project partners are also using CEA-Leti’s SiGe dot devices for spin-based quantum computing experiments. Increasing research efforts in the one-dimensional character of Ge-Si core-shell nanowires is starting to reveal the unique electronic properties of these materials. Experiments in Ge-Si core-shell nanowires include experiments on double quantum dots and spin relaxation times.

Publications


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The microelectronics industry will face major challenges related to power dissipation and energy consumption in the next years. Both static and dynamic consumption will soon start to limit microprocessor performance growth. The goal of the spOT project is to modify the memory hierarchy by the integration of non-volatility (NV) as a new feature of memory cache, which would immediately minimize static power as well as paving the way towards normally-off computing. To accomplish this aggressive goal, limitations of present NV memories in terms of speed and endurance must be overcome and new architectures taking full benefit of these new functionalities must be developed. The consortium will base its research on a recent discovery achieved jointly by SPINTEC and ION, called «Spin Orbit Torque» (SOT). This disruptive technology, which can be viewed as the ultimate evolution of Spin Transfer Torque, offers the same non-volatility and compliance with technological nodes below 22nm, with the addition of lower power consumption, cache-compatible high speed, and truly infinite endurance. To demonstrate its viability for cache, a fabrication of single cell memory devices has been accomplished. Functional devices as small as 80nm have also been demonstrated. Ultra-fast magnetic switching has been demonstrated (400ps) and this validates the ultimate evolution of Spin Transfer Torque, for the memory test chip demonstrators. GDS files have been generated and provided to the foundry to include the necessary alignment marks and measurement structures for the back end of line. A mask set has been generated from the GDS design provided by partners Spintec and KIT. The wafers used for the demonstrators are MPWs, so the mask set has been modified to include part of the reticle that does not contain SOT circuits but also requires processing. This has led to:
- circuit tape out with the contribution of several partners;
- fabrication of CMOS wafers using a multi-project wafer platform and 180nm CMOS base wafers provided by ST Microelectronics;
- integration of SOT-based memories on 200nm CMOS wafers.

To conclude, fabrication of several runs of single cell memory devices has been accomplished. Functional devices as small as 80nm have also been demonstrated. Ultra-fast magnetic switching has been demonstrated (400ps) and this validates the main advantage of this technology. Fabrication of first memory test chips on CMOS wafers has been completed and first results show that some devices can provide expected static performance but that process improvement is necessary to validate full CMOS integration.
SUPERAID7 Stability Under Process Variability for Advanced Interconnects and Devices Beyond 7nm node

Among the physical limitations which challenge progress in nanoelectronics for aggressively scaled Moore Moore, process variability is getting ever more critical. Effects from various sources of process variations, both systematic and stochastic, influence each other and lead to variations of the electrical, thermal and mechanical behavior of devices, interconnects and circuits. Correlations are of key importance because they drastically affect the percentage of products which meet the specifications. Whereas the comprehensive experimental investigation of these effects is largely impossible, modelling and simulation (TCAD) offers the unique possibility to understand process variations and trace their effects on subsequent process steps and on devices and circuits fabricated, just by changing the corresponding input data. This important requirement for and capability of simulation is among others highlighted in the International Technology Roadmap for Semiconductors (ITRS).

SUPERAID7 builds upon the successful FP7 project SUPERTHEME, which focused on advanced More-than-More devices, and is aimed at establishing a software system for the simulation of the impact of systematic and statistical process variations on advanced More Moore devices and circuits down to the 7 nm node and below, including especially interconnects. This requires improved physical models and extended compact models. Device architectures addressed in the benchmarks include especially TriGate/Gate FETs and stacked nanowires, including alternative channel materials. The software development can be benchmarked utilizing background and sideground experiments of the partner CEA. Main channels for exploitation include software commercialization via the partner GSS and support of device architecture activities at CEA. Furthermore, an Industrial Advisory Board initially consisting of GLOBALFOUNDRIES and STMicroelectronics will contribute to the specifications and will get early access to the project results.

SUPERAID7 at a glance

Project Coordinator
Fraunhofer IISB (DE)

Partners
AT: TU Wien
FR: CEA-Leti
UK: Gold Standard Simulans (Synopsys), University of Glasgow

Total budget
£ 3.4 m.

EC Contribution
£ 3.4 m.

Contract Number
688101

36 months
Jan. 2016 > Dec. 2018

Vertically stacked wire-based MOSFET architecture extends even further the scaling limits of CMOS technology. Now considered a possible extension to FinFET, this architecture offers multiple benefits. A low IDFF current is expected with high current drivability due to 3D vertically stacked channels. Obviously, there are still major roadblocks to reaching higher performance, especially introduction of stress boosters and reduction of parasitic capacitances. This is why vertically stacked wire-based MOSFETs featuring an inner spacer and SiGe:B source/drain (SiD) have been successfully fabricated using a replacement metal gate (RMG) process. Following epitaxial growth of SiGe:B multilayers, dense arrays of fins have been patterned using a sidewall image transfer process to produce 40nm-pitch fins. The dummy gate and inner spacer have subsequently been defined. The Si wires have been released during the RMG module. Figure illustrates cross-sectional TEM images of stacked wire FETs. On the other hand, strain engineering is one of the greatest challenges for GAA stacked-NWs FETs, so strain fields have been imaged at different stages of the CEA-Leti fabrication process. We have shown that SiGeB raised-S/Ds can be used to inject a significant amount of compressive strain in Si channels (deformation close to 1%). This suggests that a method involving optimized engineering of process-induced stress, such as SiGe S/Ds, can be efficient in 3D stacked-NWs devices. Electrical characterization of 25nm gate length devices has revealed high performance in terms of subthreshold slope (80mV/dec), DIBL (50mV-V) and ION current (400μA/μm at VDD=0.9V).

In the early stages of this technology’s development, design/technology co-optimization requires a physics-based compact model to ensure predictive extrapolation from hardware data. This is why CEA-Leti has developed a physical compact model (CEA-Leti-NSP) that is required for integrated circuit design. Based on a novel methodology for calculating the surface potential, this model can handle arbitrary nanowire cross-sectional shapes of vertically stacked-nanowire MOSFETs. The model accounts for quantization effects induced by small NW cross sections as well as additional physical features such as electrical field dependence on mobility, SCE/DIBL, channel length modulation, access resistances with bias dependence, velocity saturation, gate current, GIDL/GISL, self-heating effect and parasitic capacitances. This model has been validated on numerical simulation and experimental data. The physical compact model developed for both horizontal and vertical nanowire MOSFETs has been demonstrated to be highly efficient in all operation regimes. Close agreement between model and experimental data highlights that CEA-Leti-NSP is capable of providing a credible quantitative estimate of nanowire GAA MOSFET operation. This is implemented in Verilog-A language, respecting simulation robustness-related requirements. This model is now ready for designing initial circuits implementing nanowire-based GAA MOSFETs.

Publications
- “Carrier Scattering by Workfunction Fluctuations and Interface Dipoles in High-Metal Gate Stacks” Z. Zeng & al., SISPAD (2016), DOI: 10.1109/SISPAD.2016.7605223.
- “Size-dependent carrier mobility in rectangular silicon nanowire devices”, Z. Zeng & al., SISPAD (2016), DOI: 10.1109/SISPAD.2016.7605194.

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EC Programme
H2020-ICT-25-2015

Keywords
Chip design
Nanowires
Leti in THINGS2DO

The main objective of CEA-Leti in this project is to develop an innovative IoT node by leveraging the benefits of FDSOI technology. The innovation lies in the architecture of the node, which is split between an Always-Responsive part and an On-Demand part. The former part is composed of an asynchronous Wake-up controller and various wake-up sources, including a wake-up radio; this can react to interrupts with almost no latency, while consuming no energy (except leakage) in the absence of events. The second part is dedicated to compute-intensive tasks, handled by a microcontroller and specialized hardware accelerators. It is considered to be off mode most of the time. This architecture split brings the best of both worlds, namely ultra-low power dissipation and strong responsiveness.

CEA-Leti first developed the necessary building blocks in 28nm FD-SOI:
- a bandgap voltage and current reference used as reference for bias current generation and supply voltage regulation;
- a real-time clock, based on a low-frequency oscillator, used for duty-cycling the wake-up radio to reduce further its power dissipation;
- a linear voltage regulator (LDO) for regulating the supply voltage value;
- a low-voltage SRAM memory able to operate as low as 0.6V;
- an ARM M0+ microcontroller: a low-power, an ARM 32b RISC microcontroller, which incorporates 256kB of the SRAM voltage and can operate in a wide voltage range;
- a wake-up radio used to sense the radio spectrum and decode an opcode to determine whether an emitter is trying to communicate with the node and wake up the main radio;
- an asynchronous wake-up controller used to handle asynchronously the various wake-up interrupts and wake up the On-Demand part;
- an asynchronous service network used to configure the various platform parts and read status registers.

CEA-Leti is now assembling these IPs in order to implement an ultra-low power IoT node demonstrator.

EC Programme
ENAC

THINGS2DO

THIN but Great Silicon to Design Objects

The program THINGS2DO is focused on building the Design & Development Ecosystem for FD-SOI-technology. This technology is uniquely positioned to take advantage of some very distinct strengths of the European Semiconductor Industry. The baseline 28nm FD-SOI-technology is available at an inflection point in the semiconductor progression path and offers unique features at this particular point in time. 14nm-FD-SOI will then take the technology’s integration potential to unprecedented levels, utilizing the design/development ecosystem developed here.

The design/development ecosystem is based on 3 pillars:
- EDA - design automation is the basis to perform complex design creation and porting tasks. The EDA industry in Europe is particularly active in this domain;
- IP - availability of pre-designed building blocks is an absolute must for any emerging technology. The implementation environment is a vital part in conjunction with the IP needed for every complex SOC development;
- services are a combination of IP and EDA-tooling. There is a rich mix of SMEs in Europe focused on this topic, providing service offerings to bring the innovative potential of FD-SOI-technology into the leading systems and end-applications, of which Europe is so rich.

The application domains identified for THINGS2DO are: Biomedical, Aeronautics and spatial, Personal Portable Devices, among others. They all need energy efficient systems to meet market needs. The measurable results will show in the availability of a rich ecosystem of EDA-design flows, porting tools and design centering systems, a rich IP-portfolio of design building blocks from a number of -sometimes competing – Design houses.
WAYTOGO FAST
Which Architecture Yields Two Other Generations Of Fully depleted Advanced Substrate and Technologies

The pilot line project WAYTOGO FAST leverages European leadership in Fully Depleted Silicon on Insulator technology (FDSOI) so as to compete in leading edge technology at node 14nm and beyond preparing as well the following node transistor architecture. Europe is at the root of this breakthrough technology in extending Moore's law. The project aims at establishing a distributed pilot line between 2 companies:

- Soitec for the fabrication of advanced engineered substrates (UTBB: Ultra Thin Body and BOX (buried oxide)) with and without strained silicon top films;
- STMicroelectronics for the development and industrialization of state of the art FDSOI technology platform at 14nm and beyond with an industry competitive Power-Performance-Area-Cost (PPAC) trade-off.

The project provides the first phase of a 2 phase program aiming at establishing a 10nm FDSOI technology for 2018-19. A strong added value network is created across this project to enhance the competitive European value chain on a European breakthrough and prepare next big wave of electronic devices. The consortium gathers a large group of partners: academics/institutes, equipment and substrate providers, semiconductor companies, a foundry, EDA providers, IP providers, fabless design houses, and a system manufacturer. E&M will contribute to the objective of installing a pilot line capable of manufacturing both advanced SOI substrates and FDSOI CMOS integrated circuits at 14nm and beyond. Design houses and electronic system manufacturer will provide demonstrator and enabling IP, to spread the FDSOI technology and establish it as a standard in term of leading edge energy efficient CMOS technology for a wide range of applications battery operated (consumer, healthcare, Internet of things) or not. Close collaboration between the design activities and the technology definition will tailor the PPAC trade-off of the next generation of technology to the applications needs.

WAYTOGO FAST at a glance

Project Coordinator
STMicroelectronics (FR)

Partners
AT: EV Group, Global TCAD Solutions, Lam Research
BE: UCL
DE: Akrati-Polet, Bruker AXS, Fraunhofer, Fujitsu, GlobalFoundries, Hi-Dis-Electricics, IMEM, LAM Research, Matria, Siltronic, Stedinet, Sony SE
ES: Universidad Granada
FR: Picomun OY
IT: AMAT, CEA-Leti, CNRS IEMT, INFSO, STMicroelectronics Grenoble 2 SAS, STMicroelectronics 5A, TEI, General Electric
GB: GSS Ltd.
GR: ISO
IL: IVA-Tensor, NVMe Measuring Instruments
NL: FEI Electron Optics

Total budget
€ 99.4 m.

EC Contribution
€ 25.8 m.

Contract Number
ECSEL-662175

WAYTOGO FAST’s main objective for CEA-Leti is to extend as far as possible FDSOI scalability (towards 10nm), while maintaining good performance in terms of power consumption, reliability, compatibility with advanced CMOS and cost. More specifically, CEA-Leti is developing all the modules needed to step up FDSOI performance to meet the requirements of advanced 14FD+ SOI demonstrators as well as examining path-finding solutions to push 14FD+ performance characteristics and increase density.

To achieve the technological requirements, two main architectures have been developed: a first based on stepping up to 14FDSOI, the main solution for pilot line integration, and a second based on M3D (Monolithic 3D Integration). CEA-Leti is also supporting Strained Silicon-on-Insulator (SSOI) substrate development to push 14FDSOI performance characteristics.

The first 14 FDSOI+ dedicated process modules have been developed specifically with respect to electrostatic and mobility boosters. Some specific work has also been performed on local tensile stressors. Moreover, several technology blocks for producing SSOI substrates have been initiated.

In line with the project’s new orientation towards extending the 28FDSOI domain, CEA-Leti has implemented a stressor solution already developed for 14FDSOI to push the Ultra-Low Power properties of 28FDSOI. Furthermore, specific work is ongoing in relation to RF and higher voltage capability to manage embedded non-volatile memories on 28FDSOI.

CEA-Leti is also developing M3D integration (CoolCube) to provide a real proof of concept based on 28FDSOI technology. These research activities were started in 2016 with the first low temperature transistor processes and will continue throughout 2017.

Publications

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Photonics Devices
COSMICC
CmOs Solutions for Mid-board Integrated Transceivers with breakthrough Connectivity at ultra-low Cost

The COSMICC consortium gathers key industrial and research partners with world-leading positions in the fields of Silicon photonics, CMOS electronics, Printed Circuit Board-Packaging, Optical transceivers and Data-Centers around a strong vision: mass commercialization of Si-photonics-based transceivers is possible starting in 2019 by enhancing the existing photonics integration platform of one of the partners, STMicroelectronics.

COSMICC will develop optical transceivers that will be packaged on-board. Combining CMOS electronics and Si-photonics with innovative-high-throughput fiber-attachment techniques, the developed solutions are scalable to meet the future data-communication requirements in data-centers and super-computing systems. The demonstrator will feature high aggregated data rate up to 2.4 Tb/s with 200 Gb/s per fiber using 12 fibers, low electrical energy consumption not exceeding 2 pJ/bit and low-cost of around 0.2€/bit.

With performances improved by an order of magnitude as compared with current VCSELs transceivers, COSMICC developed technology will answer tremendous market needs with a target cost per bit that the traditional WDM transceivers cannot meet. The early setting up of a new value chain will enable exploitation of the developed technologies.

CEA-Leti in COSMICC
CEA-Leti is contributing to COSMICC project at demonstrator device and circuit levels. The institute has launched technological developments to enhance its 200mm R&D Silicon Photonics platform with additional SiN material. This SiN layer, which is integrated to top of the Si layer with an intermediate SiO2 spacing layer, ensures greater flexibility. In particular, the refractive index of SiN is less sensitive to temperature than that of Silicon and this is an advantage for low-cost applications with no temperature control. CEA-Leti is using this line to develop Si/SiN photonic devices, which are key to 4-wavelength coarse WDM applications used at data centers: typically thermally insensitive multiplexers/demultiplexers and broadband fiber grating couplers. CEA-Leti is also working on the development of compact, low-operating voltage silicon modulators based on slow-wave light to reduce energy consumption and ease co-integration with driver electronics. Work is also being performed to design and integrate hybrid II-V lasers into the institute’s SiN-enhanced Silicon Photonics platform for developing advanced fully integrated transmitter circuits.

CEA-Leti’s aim is to transfer fabrication of high-performance Si/SiN key photonic devices to the 300mm line at STMicroelectronics for integration in the two project demonstrators. Demonstrator packaging will be shared among the project partners. CEA-Leti will be responsible for optical packaging (connection of 4 optical fibers to the photonic integrated circuit) of the first project demonstrator, which features a 200Gb/s aggregated data rate. This demonstrator comprises a 2-wavelength CWDM mid-board, integrated silicon photonics transceiver integrating 50Gb/s photonic and electronic components. At the second stage of the project, a full demonstrator with 4-wavelength CWDM and 24 connected fibers will be developed to provide a 2.4Tb/s aggregated data rate.
IRIS
Integrated Reconfigurable Silicon Photonic Based Optical Switch

IRIS aims at fabricating a highly integrated, scalable, transparent and high capacity WDM Photonic Switch used as a Transponder Aggregator (TPA), a novel function which will be added to existing ROADM nodes without disrupting their architecture while adding attributes such as colourless, directionless and contentionless.

For Metro networks, this switch will provide flexibility, energy efficiency, very small footprint, low cost and faster reconfigurability. This novel integrated switch architecture is also suitable for Data Centre networking due to its capability to manage large throughput in a single chip with low cost, low footprint and low power consumption.

The new TPA will be based on a fully integrated electro-photonic device realized by using Silicon Photonics with an unprecedented density of photonic components (>1k on <30 mm² chip area) controlled by >2k electronic building blocks. The TPA target product is an optical sub-system for Metro applications driving 48 optical channels, with 100 GHz spacing in the C-band, 4 different directions and 12 add/drop channels. A fully packaged prototype will be implemented with 12 wavelengths, 4 directions and 8 A/D ports, it will be integrated with a commercial transport node and tested with 10G and 100G signals.

Leti in IRIS

CEA-LETI is contributing to the IRIS project:
- photonic component design on passive and active integrated optical devices;
- photonic integrated circuit fabrication using CEA-LETI’s 200mm clean room facilities;
- wafer-level testing for statistical analysis;
- electronic/photonic integration for next generation demonstration;
- 2nd generation optical devices as building blocks for the IRIS operational demonstrator;
- 1st generation matrix switch for the demonstrator photonic integrated circuit;
- micro-bumping of 1st generation driving electronics.
LEO
Low-cost /energy Efficient Oleds for lighting

LEO ambitious innovative manufacturing concept & routes toward high performance bendable and low cost OLEDs for general and mood lighting merging conventional and proven technologies with disruptive approaches (e.g. substrate, architecture, hybrid wet and vacuum processing, layouts). The project targets the introduction of novel materials combinations (conformable & functionalized metallic substrates, Indium free electrodes and solution-processable organic materials) in large area colour tuneable top emission white OLEDs.

R&D activities will be ramped-up from lab scale feasibility to pilot line scale demonstration, delivering show off lighting systems with the help of external lighting manufacturers (Artemide, Technology Luminaires).

With common and innovative building blocks substrate with integrated interconnecting, 80% transparent top electrode, 1E-6 g/m²/day WVTR scratch resistant thin film encapsulation, 50% out-coupling efficiency, these two complementary approaches will lead to demonstrations of large area warm/cold white macro-pixels and hybrid full colours RGB OLEDs. LEO will also address cost reduction at materials and process levels, for that LEO has gathered all stakeholders of the OLED lighting device fabrication value chain (except equipment supplier), including substrate and organic materials suppliers (Arceo for Mitata, Cynora, an OLED manufacturer (OSRAM) and recognized research centres in the field of OLEDs and life cycle analysis (CEA, CNR, Gaiker).

36 months
Jan. 2015 > Dec. 2017

LEO at a glance

Project Coordinator
CEA-Leti (FR)

Partners
BE: Advanced Coatings & Construction Solutions SGRL
ES: Fundacion Gaiker
GE: Cynora Gmbh, Osram Oled
IT: Consiglio Nazionale Delle Ricerche

Total budget
€ 4 m.
EC Contribution
€ 4 m.

Contract Number
644742

Leti in LEO

After two years of intense activity, development of the main technological building blocks within the scope of the LEO project has progressed well, in particular with several proofs of concepts and demonstrations achieved at CEA-Leti.

› Better performing electrodes. The advantage of vacuum-deposited Ag silver anodes has been confirmed by the demonstrating +30% additional luminance compared with conventional Au-based anodes. Similarly, an advanced top cathode concept using a WO3/Ag/WO3 multilayer stack has been theoretically and experimentally demonstrated to provide +50% light emission in mono-color, top-emitting OLEDs.

› Better encapsulation. A CEA-Leti proprietary Al2O3/hard coat thin film encapsulation coating has been demonstrated to offer outstanding protection efficiency against humidity together with excellent scratch resistance. The barrier performance achieved (WVTR= 1.6x10-6 g/m²/day at 85°C / 85%HR) is among the best demonstrated in thin film encapsulation.

› OLEDs on metal foils. Several operational OLEDs have been successfully made by vacuum deposition on low carbon steel foils functionalized by epoxy, using an upgraded resist processed at CEA-Leti. With regard to opening the way to upscaled OLED technology on metal foils, a first decisive step has recently been completed with successful manufacturing of top-emitting-Tandem OLEDs to provide fairly uniform lighting on a relatively large (25cm²) active area of low carbon steel foil. Even more interesting is the device's capacity for withstanding noticeable bending during operation (see illustration). This specifically demonstrates this technology's novelty and its advanced device lifetime, which will require a very high control of metal sheet surface quality to suppress any potentially fatal defect.

› Rare-earth, metal-free OLED emitters (TADF). Initial integration of these innovative materials has started at CEA-Leti’s 200mm OLED platform using green and blue emitting devices first. However, stack optimization is still required to achieve the exceptional performances announced by partner CYNORA (blue emission approximately 3 times higher than conventional Al-based anodes).

› Better performance at low carbon steel foils. An advanced top cathode concept using a WO3/Ag/WO3 stack has been theoretically and experimentally demonstrated to provide +30% additional luminance compared with conventional Au-based anodes. Similarly, an advanced top cathode concept using a WO3/Ag/WO3 multilayer stack has been theoretically and experimentally demonstrated to provide +50% light emission in mono-color, top-emitting OLEDs.

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Leti in PIXAPP

In this project, CEA-Leti is developing and transferring an innovative technique for self-aligning microlenses arrays on top of Photonic Integrated Circuits. This leads to inexpensive, mass production-compatible optical assembly of photonic devices for various applications ranging from optical fiber high-speed modules to biosensors. Copper micropillars (microbumps) are processed on top of Photonic Integrated Circuits. These structures ensure accurate alignment (<1μm) of the microlenses used to collimate or refocus an output beam.

This work will lead to a preliminary phase, during which the proposed technology will be assessed. Current results from the IRT Nanoelec project indicate that a back-end process will be performed on reference wafers processed at IMEC. This involves growing copper micropillars and eutectic solder caps on the top of Photonic Circuits. At the same time, microlens arrays will be purchased from an external company as full wafers and post-processed at CEA-Leti. The reference chips will be used to assess the self-alignment process and characterize the residual misalignment, which is expected to be submicrometric.

Additional optical characterization will be performed to analyze the output beam and validate the microlens optical design. This assembly process will be used SET equipment at CEA-Leti and will be subsequently transferred to the Argotech company. The method will also be applied to functional devices taken from various application fields including optical Datacom communications and biosensors.

Once the method has been demonstrated on reference chips and demonstrator chips, it will be proposed as an available assembly technique within the framework of the PIXAPP platform.

PIXAPP Photonic Integrated Circuits Assembly and Packaging Pilot Line

PIXAPP will establish the world’s first open access Photonic Integrated Circuit (PIC) assembly & packaging Pilot Line. It combines a highly-interdisciplinary team of Europe’s leading industrial & research organisations. This project provides Europe’s SMEs with a one-stop-shop, enabling them to exploit the breakthrough advantages of PIC technologies. PIXAPP bridges the “valley of death”, providing SMEs with an easy access route to take R&D results from lab to market, giving them a competitive advantage over global competition. Target markets include communications, healthcare & security, which are of great socio-economic importance to Europe. PIXAPP’s manufacturing capabilities can support over 120 users per year, across all stages of manufacturing, from prototyping to medium scale manufacture. PIXEL bridges missing gaps in the value chain, from assembly & packaging, through to equipment optimisation, test and application demonstration. To achieve these ambitious objectives, PIXAPP will:

- develop an innovative Pilot Line operational model that coordinates activities between consortium partners & supports easy user access through a single entry point;
- establish packaging standards that provide cost-efficient assembly & packaging solutions, enabling transfer to full-scale industrial manufacture;
- create the highly-skilled workforce required to manage & operate these industrial manufacturing facilities;
- develop a business plan to ensure Pilot Line sustainability & a route to industrial manufacturing.

PIXAPP will deliver significant impacts to a wide stakeholder group, highlighting how industrial & research sectors can collaborate to address emerging socio-economic challenges.
REDFINCH

Mid-InfraRed Fully Integrated Chemical Sensors

Mid-infrared photonic integrated circuits (mid-IR PICs) are the subject of increasing interest due to the large amount of sensing applications in the 2-20μm wavelength range. Most molecules exhibit absorption fingerprints in the mid-infrared (MIR) wavelength range corresponding to their rotational/vibrational energies. Tunable-diode laser absorption spectroscopy thus allows detection and concentration measurements of many biological and chemical species. This is of crucial interest for many societal applications such as health monitoring and diagnosis, detection of biological compounds, monitoring of toxic gases, or of greenhouse gas emission responsible for global warming, to name but a few. However, state of the art sensing systems are large and delicate which greatly hampers potential applications.

REDFINCH will use hybrid and monolithic integration of III-V diode and Interband Cascade/Quantum Cascade materials with silicon to create high performance cost effective sensors based on Photonic Integrated Circuits. Integration creates extremely robust systems, in which discrete components are replaced by on-chip equivalents, giving a simultaneous improvement in ease of use and a reduction in cost.

Leti in REDFINCH

In REDFINCH, two approaches will be followed: in the first phase, a hybrid mini-PA approach on Si and then a fully integrated μ-PA. Used with QCL, a hybrid mini-PA approach allows to reach sub ppm detection capability range in the MIR region. This platform is only compatible with small handmade production and limited in cost reduction. REDFINCH will bring the platform to mass production facility in order to:
- increase the manufacturing accuracy;
- access surface processing for harsh environments;
- reduce the cost.

In the second phase, initial work on M&NEMS technology applied to acoustic detection will be extended to produce a proof of concept of a fully integrated photoacoustic sensor including M&NEMS microphone. The QCL on Si and coupling required for both of these will be advanced in REDFINCH from work (proof of concept) done in other projects, to hybrid die-to-wafer bonding with evanescent coupling. In the continuity of previous european projects, CEA-Leti will bring its competencies on heterogeneous integration, photoacoustic cell and microphone fields.
Leti in SEQUOIA

CEA-Leti brings its Silicon technology know-how and Grenoble-based infrastructures to the SEQUOIA project. The institute’s infrastructures include state-of-the-art CMOS 200nm and 300nm wafer-processing lines. Design clusters have been extensively used to provide the main building blocks of high speed hybrid III-V on silicon transmitters, including silicon modulators, multiplexers and low loss grating couplers (Figure 1(a)). CEA-Leti infrastructures also include two 300nm wafer probe testers ensuring extensive electro-optical statistical analysis.

CEA-Leti’s major outcome is validation of frequency comb generation with quantum dot/dash materials (on the hybrid III/Si platform) as well as design, fabrication and characterization of 400Gbps transmitters. At the current project stage, most of the building blocks have been demonstrated with the exception of functional hybridization of quantum dot/dash materials, which have been partially demonstrated to date.

Design of the hybrid laser cavity has been experimentally validated (Figure 1(b)) using a distributed feedback laser unit fabricated within the SEQUOIA project scope. The corresponding optical spectrum (Figure 1(c)) reveals an excellent 40dB side mode suppression ratio with approximately 1mW emitted power.

Another example of building block demonstration is shown in the Figure 1(d) showing the experimental spectrum of a high density silicon multiplexer with a channel spacing of 100GHz and insertion losses below 2dB, which represents a new state of the art.

Combination of all building blocks is schedules for the next project phase to demonstrate fully integrated high speed (16x25Gbps) hybrid III-V on silicon transmitters.

The technology developed within the SEQUOIA project can be extended to other types of transmitters, e.g. with extended link ranges, higher bit rates, higher WDM channel numbers and other modulation formats. A broad range of applications, such as sensing, health-care, safety and security, will benefit from the technology developed in SEQUOIA.

Publications


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48 months

SEQUOIA at a glance

Project Coordinator

III-V Lab (FR)

Partners

DK: DTU
FR: CEA-Leti, University of Rennes 1
GE: INViLUM, University of Kassel

Total budget
€ 5 m.
€ 3.3 m.

Contract Number
619626

SEQUOIA

Energy efficient Silicon transmitter using heterogeneous integration of III-V Quantum dot and quantum dash materials

The SEQUOIA project intends to make significant new advances in silicon photonic integrated circuits by heterogeneously integrating novel III-V materials, namely quantum dot and quantum dash-based materials on silicon wafers, through wafer bonding. Thanks to the superior properties of those innovative materials, hybrid III-V lasers with better thermal stability, higher modulation bandwidth and the possibility of generating a flat wavelength-division-multiplexing comb will be demonstrated. Moreover, the hybrid integration of nanometric structures on Si allows to exploit the advantages provided by silicon. In particular, optical filters can be directly integrated with hybrid quantum dot/quantum dash/Si lasers to create chip-managed lasers, which have an enhanced modulation bandwidth and extinction ratio compared to directly modulated lasers. As an illustration of the technology developed in SEQUOIA, transmitters with a total capacity of 400Gbit/s (16x25Gbit/s) will be designed, fabricated and characterized.

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II-V Lab (FR)

Keywords

Heterogeneous integration

Laser diodes

OptoElectronic Integrated Circuits (OEICs)

Quantum dots

Semiconductor technology

Publications

Power Electronics
ATHENIS3D provides the industry’s first 3D heterogeneous integration technology platform for harshest automotive conditions with Through Silicon Vias (TSV) and Wafer Level Packaging (WLP). A demonstrator car proves the functionality of the 3D integrated electronics for an electrical machine with start/stop function and the industry’s first 3D/TSV/WLP DC/DC converter with integrated inductor for the new 48V standard. Cost savings from integration and a 5x reduction of PCB area with improved reliability are expected. For this purpose substantial technological barriers such as flipchip mounting of a 90nm CMOS FPGA on a 180nm HVMOS Si interposer with integrated inductor for the new 48V standard. Cost savings from integration and a 5x reduction of PCB area with improved reliability are expected. For this purpose substantial technological barriers such as flipchip mounting of a 90nm CMOS FPGA on a 180nm HVMOS Si interposer with integrated inductor for the new 48V standard. Cost savings from integration and a 5x reduction of PCB area with improved reliability are expected. For this purpose substantial technological barriers such as flipchip mounting of a 90nm CMOS FPGA on a 180nm HVMOS Si interposer with integrated inductor for the new 48V standard. Cost savings from integration and a 5x reduction of PCB area with improved reliability are expected. For this purpose substantial technological barriers such as flipchip mounting of a 90nm CMOS FPGA on a 180nm HVMOS Si interposer with integrated inductor for the new 48V standard. Cost savings from integration and a 5x reduction of PCB area with improved reliability are expected. For this purpose substantial technological barriers such as flipchip mounting of a 90nm CMOS FPGA on a 180nm HVMOS Si interposer with integrated inductor for the new 48V standard.

CEA-Leti is coordinating the work package involving heterogeneous integration technologies for chip packaging. This includes:

- engineering and Development of 3D modules for harsh conditions:
  - thick copper Redistribution Layer (10μm),
  - thick copper Through Silicon Vias (TSV) with aggressive aspect ratio (40μm diameter 200μm depth),
  - Chip-to-Chip interconnections,
- high thermal storage reliability and electromigration test campaigns;
- wafer level overmolding process development and first demonstrator.

Process development for the copper Through Silicon Vias (TSV) has provided interesting results for power application in a harsh environment:

AR 2.5:1 (TSV 80x200μm): fully integrated samples featuring front side rerouting / TSV 080xH200μm / backside rerouting have been successfully processed and are now being tested for thermal reliability and electromigration (2A per TSV).

AR 5.1 (TSV 40x200μm): using a robust chemistry process, fully integrated samples featuring front side rerouting / TSV 040xH200μm / backside rerouting have also been successfully processed (see figures) and are now being tested for thermal reliability at 200°C and electromigration (2A per TSV).

Overmolding and screen-printing studies have been successfully conducted right up to full integration. As the figures illustrate, the molding studies allowed us to perform underfilling and molding in one single step with a single material comprising stacked dies. This represents a significant time saving in the process flow from capillary underfill die level to collective vacuum lamination wafer level.

The screen printing process has been shown to be compatible with 100-300μm thick wafers with a bow in the range of several hundreds of microns to samples mounted directly on an application board or PCB.

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E2COGAN
Energy Efficient Converters using GaN Power Device

E2COGAN examines GaN-on-Si as a disruptive High Voltage technology for Schottky Barrier Diodes and High Electron Mobility Transistors (HEMTs) through the whole value chain up to demonstrators. More precisely the capability of GaN-on-Si is shown to provide a well-balanced and application specific trade-off between the “corner” benefits given by higher efficiency, higher switching frequency, smaller footprint and weight and competitive cost on system level with respect to Si or SiC. The consortium provides an industry-centric approach implying the whole GaN power electronics value chain from the substrate provider, GaN device manufacturer, assembly house to the end user, supported by top academic institutes and other tool or service providers (simulation software, measurement tools, etc.). Concerning the GaN power devices the process is to consolidate 600V, 10A and gradually explore higher voltages up to 1500V) and currents (up to 100A) at the end of the project, giving priority to the early exploration of applications below 10kW. Reliability issues and parasitic effects are investigated through a combined approach based on advanced electro/optical measurements and electro/thermo/mechanical TCAD simulations to understand and identify the Safe Operating Area and to develop a robust and reliable GaN-on-Si power device technology platform. Demonstrators are focused on two application domains of strategic relevance: Photovoltaics and Automotive.

36 months

E2COGAN at a glance

Project Coordinator
ON Semiconductor Belgium BVBA (BER)

Partners
AT: CISC Semiconductor
BE: EpiGAN, NXP, ON Semiconductors
CH: Synopsis CH
DE: Audi, Azzurro Semiconductors, Fraunhofer, Robert Bosch, Semikron, University of Kassel
FR: CEA-Leti, CIRTEM, EADS, MC2 Technologies, Schneider Electric
IT: Bitron SPA, IUNET, STMicroelectronics SRL
NL: TU Eindhoven
SK: NanoDesign, Slovenian TU Bratislava
UK: University of Bristol

Total budget
€ 26.1 m.
EC Contribution
€ 3.9 m.

Contract Number
ENIAC-324280-2

Leti in E2COGAN

A major challenges for GaN-on-Si technology is the quality of epitaxial growth on the silicon substrate. CEA-Leti has primarily focused efforts on investigating and developing material processing for high performance GaN-on-silicon substrates and device technology. The institute has conducted fundamental research into extended defect types caused by buffer, epitaxy or device technology (edge and screw-type dislocations, stacking faults, grain boundaries, particles and other 3D defects), defect densities and their influence on device performance and degradation mechanisms.

CEA-Leti has also investigated the use of in-situ SiN capping layers to reduce surface states and provide better surface passivation. The impact of different capping layers (GaN, SiN) on device reliability and the use of in-situ SiN to reduce possible cross-contamination in CMOS fabrication have also been studied. Research activity has included modeling, device testing and correlation of phenomena with device performance.

Fundamental studies of epitaxial layer structures, SiN passivation and device performance now provide the basis for significantly improved GaN devices. Testing up to 1200V shows stable performance with promising potential for future commercial devices.

New current collapse models have been validated, while the tools needed for characterization and testing are in place and the technology is well positioned for near-term market entry. Through its several demonstrators, the project has proven that GaN-on-Si as a disruptive high voltage technology has tremendous added value and huge potential for developing high voltage devices offering higher efficiency and switching frequency, smaller footprint and competitive cost at system level compared with Si and SiC.
The aim of the EnSO project is to demonstrate the competitiveness of new energy solutions implementing microbattery and energy harvesting technologies for powering autonomous Smart Objects in Smart Society, Smart Health, Smart Mobility and Smart Production key applications.

During Year 1 of the project, Autonomous Micro Energy Source (AMES) requirements were defined and two types of demonstrator were designed and built for evaluation. These combine microbattery energy storage and energy harvesting (photovoltaic, thermoelectricity, mechanical harvesting). CEA-Leti is mainly involved in developing microbattery technology. Regarding this aspect, a number of technical issues have been addressed, ranging from advanced material development to process industrialization and reliability. A microbattery manufacturing process has been optimized on a Gen5 pilot line and has been shown to be robust. Handling solutions for very thin substrates (50μm) compatible with high temperature processes have been studied and prospects are considered good. Moreover, an advanced patterning process for Free Form Factor microbatteries has been developed and proof of concept of new electrolyte materials for reducing internal resistance by a factor of 3 has been achieved. First 3V electrode materials have been manufactured and tested, while up to 15 microbatteries have been stacked to improve capacity and reduce internal resistance. Finally, prototypes have been delivered to end-users for integration into autonomous modules based on energy harvesting solutions and power management.

**EnSO at a glance**

**Project Coordinator**
ST Microelectronics (FR)

**Partners**
BE: Hermet, Prayon SA, Université de Liège
CZ: CTU Prague
DE: AED Engineering, Airbus, Applied Materials, Fraunhofer IIS & EMFT, 0-Flexx, Van Ardenne
DK: GN Forsand
ES: CSG, Gas Natural SDG, idneo, Gijmar
FR: Alinéo, CEA-Leti, CNRS, Edisys, Enerbee, Gemalto, Optimativa, SKF, Soledes, Université FR Tours
NL: Eutax, High Centre, Maastricht Instruments, Meyer Burger, Nardonis, SKT, Universiteit Maastricht

**Total budget**
€ 82 m.

**EC Contribution**
€ 18.7 m.

**Contract Number**
692482

**Contractor**

EnSO (Energy for Smart Objects) provides a unique European ecosystem in the field of high-performance autonomous miniature energy-harvesting power sources that enables development of new innovative microelectronic systems for the IoT market in Europe.

The scope of the project encompasses energy solutions for powering “smart” objects in Smart Society, Smart Health and Smart Energy key applications. EnSO develops automated assembly technologies of shapable and customisable micro batteries, energy harvester and power management building blocks, with scale up of a competitive, high volume production capacity.

The main EnSO objectives are to:
- demonstrate the competitiveness of EnSO energy solutions for powering autonomous Smart Objects;
- disseminate EnSO energy solutions with easy to use demonstration kits to foster the take-up of emerging markets;
- develop high reliability assembly technologies of shapable micro batteries, energy harvester and power conditioning building blocks for Autonomous Micro Energy Sources (AMES);
- develop and demonstrate very high capacity and very high density rechargeable micro battery product family;
- develop customizable smart recharge and energy harvesting enabling technologies for AMES;
- demonstrate and evaluate the AMES design and manufacturing capability based on generic key enabling building blocks.

**EnFilm microbatteries.**

**Microbatteries on thin substrate.**

**EnSO at a glance**

**Project Coordinator**
ST Microelectronics (FR)

**Partners**
BE: Hermet, Prayon SA, Université de Liège
CZ: CTU Prague
DE: AED Engineering, Airbus, Applied Materials, Fraunhofer IIS & EMFT, 0-Flexx, Van Ardenne
DK: GN Forsand
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NL: Eutax, High Centre, Maastricht Instruments, Meyer Burger, Nardonis, SKT, Universiteit Maastricht

**Total budget**
€ 82 m.

**EC Contribution**
€ 18.7 m.

**Contract Number**
692482

**Contractor**
Leti in EPPL

Building on recognized experience in 3D integration, CEA-Leti provides packaging technology for power components. The main EPPL project topics include: silicon interposer technology and wafer level package for power applications, high current density/peak current TSVs, Cu RDL and Cu pillar technology for power devices, UBM and bumping for power applications, D2W for power devices and high temperature temporary bonding.

Within the scope of the EPPL project, a new fully 3D integrated H bridge device has been proposed, designed and processed based on cooperation between Infineon, AMS and CEA-Leti. This device has been designed with a 500μm pitch for the back side solder balls and 250μm pitch for TSVs. All the patterns have been designed in honeycomb array to optimize integration of TSVs, pillars, passivation openings on the front side and solder ball on the back side. Dedicated process modules have been developed and applied for this power application in the kilowatt range including thick copper recruting. The set-up’s excellent electrical performance is reflected by a very low Kelvin TSV contact resistance of 2.1mΩ and by fully functional DMOS devices. CEA-Leti’s results confirm the way forward for new types of 3D applications in the field of small power devices.
Monitoring -Wireless sensors
CLEANSKY JTI-CS-2013-2-
SAGE-02-034 - Health
EC Programme
Keywords
Sensor node
Rfid
of physical parameters inside the engine, and so requires a large
Reduction of emissions in such jet engines requires a deep knowledge
airplane engines).

HiTEAS
High Temperature Energy
Autonomous System

In the European project Clean Sky, SAGE 2 (Sustainable And Green
Engines) project aims at designing, manufacturing and testing an
energy efficient Counter-Rotating Open-Rotor Demonstrator (with a
drastic reduction of CO2 and NOx emission compared to conventional
airplane engines).

Reduction of emissions in such jet engines requires a deep knowledge
of physical parameters inside the engine, and so requires a large
number of sensors to be implemented in the engine. Current aeronau-
tic-compatible sensors require cables to wire-connect the sensor to
the FADEC. Number of cable becomes an issue when many parame-
ters need to be acquired. Moreover rotating part in jet engines cannot
be monitor with wired sensors.

Objective of HiTEAS project is to demonstrate it is possible to wire-
lessly acquire data from a cable-free sensor node during jet engines
ground testing, withstanding aeronautics temperature and vibrations
constraints. The targeted temperature is from -30°C up to 250°C.

HiTEAS’s demonstrator includes the complete acquisition chain, inclu-
ding a Wireless Sensor Node (WSN), an interrogator with its antenna,
and a host controller (PC). The demonstrator is developed for being
mounted and tested in SAGE2’s demonstrator in Istres.

Leti in HiTEAS

The final HiTEAS demonstrator is a complete acquisition chain compatible with a jet
engine environment.

The complete demonstrator is made of building blocks that have been independently
developed and characterized.

A battery-less Wireless Sensor Node (WSN) integrating an Application Specific In-
tegrated Circuit (ASIC), a wind micro-turbine and a RFID antenna, ensures physical
parameter sensing, data coding and interrogation over the air from an RFID reader. The
WSN is supplied from the UHF RFID’s electromagnetic field or from a low-frequency
AC signal emitted by the wind micro-turbine.

The ASIC is fabricated using a high-temperature CMOS SOI silicon process provided
by XFAB. It integrates a versatile 85ps-1Kps sensor interface to address both pressure
and strain sampling rate requirements. In addition, a dynamic excitation scheme
lowers the transducer excitation current, thus enabling cable-less power supply to aero-
nonautical grade 350 - 3kΩ resistance bridges. The ASIC also integrates an ISO18000-
63 front-end, which is connected to a dedicated antenna. An automatic mechanism
embedded in the ASIC selects the most efficient power source and generates the in-
ternal voltage supplies.

The silicon process is qualified up to 175°C, so the ASIC is limited to jet engine loca-
tions at which the temperature is below 175°C.

A wind micro-turbine has been developed and tested. I can power the WSN with only
a 3m/s air flow, is compatible with high temperatures (up to 250°C) and withstands
specified vibrations. The main characteristics of the wind-turbine are:
- size: 45x40x48mm³;
- weight: 50g;
- maximum vibration level: 20G;
- maximum operating temperature: 250°C;
- output power at 2.5m/s (23°C): 1000μW;
- output power at maximum power point at 2.5m/s (25°C): 2.2Wms;
- reversible temperature loss (alternator efficiency) -8% at 180°C and -34% at 250°C.

The WSN is interrogated using a standard RFID reader, nevertheless specific RFID an-
tennas have been developed to cope with temperature constraints. Two reader and tag
antennas have been simulated, fabricated and measured. They cover a 15MHz band-
width (905MHz-920MHz) and have a maximum gain of 4.9dBi for the reader antenna
and 1.4dBi for the tag antenna. These antennas have been printed on a high-tempe-
tature Rogers RO4003C dielectric substrate. Measurements have confirmed that the
reflection coefficient of both antennas is stable over the temperature range. Finally, link
budget studies have shown it is possible to communicate between a >2 m tag-to-reade-
ter distance and to power remotely the WSN up to 30cm away.

The system developed within the scope of the HiTEAS project is versatile since building
blocks can be arranged or programmed in different ways to address a wide range of
usage scenarios. Current demonstrator maturity level is low but no showstopper to
increasing the system maturity level has been identified.

The work initiated in HiTEAS continues in the framework of the CEASSARlab, which is a
SATRAIN and CEA-Leti joint research laboratory.
ModuLED
Modular Electric Drivetrains

Project ModuLED aims at developing a market-driven new integrated electric propulsion system with new e-machine design, advanced motor electronics and improved transmission system.

The powertrain itself will be modular to address multiple configurations for electric and hybrid vehicles. The project targets:

- Powertrain related losses reduced by 50%;
- Power density increased by 5% with energy recuperation and mass reduction, and also the development cycle of next generation electrical powertrain modules shortened by 25%.

ModuLED is based on Permanent Magnet Synchronous Motor (PMSM) and will develop new electrical machine using ferrites-based buried permanent magnets resulting in a lower content of rare earth material.

ModuLED at a glance

- **Project Coordinator**
  CEA-Leti (FR)
- **Partners**
  BE: Punch Powertrain  
  CH: Brusa  
  DE: RWTH Aachen, ZG  
  NL: Eindhoven Technical University  
  SW: Chalmers University
- **Total budget**
  € 7 m.  
  **EC Contribution**
  € 7 m.
- **Contract Number**
  769953

36 months

Leti in ModuLED

CEA-Leti is the project coordinator. Within CEA, the project also involved the CEA-Liten institute.

Several outcomes are expected:

- Modular design of powertrain components for hybrid and electrical vehicle, including e-motor, inverter, transmission and powertrain cooling systems (all partners);
- The inverter integrates new high bandwidth GaN transistors (CEA-Leti, Tu/e, Brusa);
- The electric motor uses ferrite based permanent magnets to lower the content of rare earth metals (CEA-Liten, Brusa);
- A new 6 phase electric motor using less rare-earth magnets;
- A new transmission design with a two-stage speed reduction;
- A high level regenerative braking system with extended range of energy recuperation (Chalmers, Punch Powertrain);
- An integrated thermal system using phase change materials - PCM (RTWH Aachen, CEA-Leti, ZG);
- Vehicle simulation solution and services supporting high speed modular electric powertrain (Siemens, RTWH Aachen).

Finally, a full scale demonstrator is planned with all the developments integrated within an existing electric vehicle (e.g. BMW i3).

Among those, CEA-Leti will specifically contribute to the design and realisation of the inverter for the multiphase motor. The challenge is to design the phase, integrate the GaN transistors, ensure proper cooling and reach the industrial requirement. The expected power for the motor is 70kW.

The modular design is key to ensure interoperability of all components with other vehicle configuration such as hybrid. All developments are linked to an industrial partner for its further exploitation. A scientific advisory board is set up and involves a car manufacturer.
Wireless Communications & Networks
CEA-Leti contributions to the 5G CHAMPION project involve antenna design and implementation of algorithms for high capacity mmWave backhauling/fronthauling. CEA-Leti is also involved in defining and implementing a test bed dedicated to an NB-IoT over-satellite channel and PHY layer definition, testing and validation using a channel emulator.

CEA-Leti is developing electronically reconfigurable transmit array antennas for backhauling and fronthauling at 28 GHz, designing RF impairment compensation algorithms resistant to high order modulation, investigating solutions to join use of high-order modulation and spatial multiplexing and to signal transmission in strongly time variant channels. CEA-Leti is also investigating advanced mobility management solutions based on the C/U plane split.

CEA-Leti is proposing and comparing various waveform candidates to fulfill the requirements of 5G NB-IoT including critical applications. As a starting point, consideration is given to the waveform used in existing or upcoming standards under 3GPP (e.g. LTE category-M, LORA, NB-IoT).

The 5G-similar waveform (e.g. filtered multicarrier) can then be adapted to the specific requirements of low cost, low power consumption and satellite constraints (RF characteristic/performance, satellite channel characteristics). CEA-Leti will investigate enhanced waveforms to lower the PAPR as much as possible, while maintaining acceptable complexity on the transmitter side. The outcome of the task will be new waveform proposals (or enhancement of existing ones), performance validation through simulations, algorithm design. The results of this task will be used for the definition of the proof of concept demonstrator.

CEA-Leti is taking part in integrating 5G CHAMPION PoC work for the backhauling solution. Furthermore, CEA-Leti will implement the specified experimental satellite access test bed on its flexible hardware platform (a dedicated hardware design facility offering a WP split).

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CEA-Leti is developing new solutions for millimeter wave (mmWave) communications and mobile edge cloud technologies. The institute plans to extend its system level simulator to characterize and assess future mobile networks. CEA-Leti’s projected outcomes in 5G MiEdge for each Work Package (WP) are:

- to contribute to defining the 5G ecosystem and to its usage through detailing possible user cases, scenarios and system architectures;

- to focus on investigating fundamental analytical trade-offs in future mobile networks. This will ensure parameterization of a complex, dense network, in which multiple radio access technologies are used in combination with macro and small cells;

- to continue investigating joint beam steering and beam forming mechanisms to improve user data rate and minimize co-channel interference based on machine learning tools. CEA-Leti is already designing learning mechanisms to construct real-time context aware maps that describe available communication/computation resources, together with clustering techniques aimed at finding a suitable clustering of communication/computation nodes;

- to assess proposed mechanisms through system level simulations. CEA-Leti, as a dissemination and communication leader, intends to co-organize promotion at international conferences and scientific events, and to publish results in conference papers and journals.

One year after project start-up, CEA-Leti has disseminated its results in an invited IEEE magazine, two journal submissions and a conference paper. Moreover, a patent is now being drafted.
CLEAR 5G
Converged Wireless Access for reliable 5G MTC for factories of the future

CLEAR5G objective is to design, develop, validate, and demonstrate an integrated converged wireless network for Machine Type and Mission Critical Communication (MTC/MCC) services for Factories of the Future (FoF). CLEAR5G will deliver technical solutions addressing the challenges of massive deployment of connected devices, security, ultrafast latency and ultra-high reliability in FoF applications, like remote maintenance and closed loop control systems. The requirements of these complex scenarios will be met through the convergence of different wireless technologies, enabled by protocol and architecture enhancements proposed by Clear5G.

Clear5G will focus on providing PHY, MAC, and architectural enhancements to meet the strict requirements of FoF applications in terms of KPIs: latency, reliability, connection density, spectrum, and energy efficiency, thus contributing to the ITU-R objectives (e.g. 1000 fold connection density) for the next generation mobile network. The Clear5G team comprises a combination of European and Taiwanese successful, innovative, and well known major corporations, SMEs, as well as research and academic institutions. The partners have proven know-how in architecture, resource management, protocol enhancements, standardization, prototyping, and demonstration. Proof of concepts will be tested on the 5GIC testbed in Europe, while the final system demonstration, showing the tight integration and cooperation of manufacturing and the Clear5G enhanced network, will be implemented on the II testbed in Taiwan.

Clear5G brings together a strong and diverse set of European and Taiwanese partners, including partners from the FoF sector; the complementarity of team, skills and expertise will bring added value to 5G research on both sides and will deepen international cooperation, serving as a showcase of 5G empowering vertical industries. The partners will contribute to relevant standardisation in both the communication and the manufacturing domains.

CLEAR 5G
Converged Wireless Access for reliable 5G MTC for factories of the future

30 months

Clear 5G at a glance

Project Coordinator
University of Surrey (UK)

Partners
FR: CEA-Leti
GR: WINGS ICT Solutions Ltd
NL: Netherlands Organisation for Applied Scientific Research
TR: Anapa, Turk Telekom
TW: ASSLINK Technology Inc., Fair Friens EnterpriseCo, Ltd, Hon Hai Precision Industry Co., Ltd, Hsinchu Science Park Branch Office (Foxconn), Institute for Information Industry, National Taiwan University
UK: Toshiba Research Europe, University of Surrey

Total budget
€ 3.4 m.
EC Contribution
€ 2.5 m.

Leti in CLEAR 5G

- CEA-Leti will contribute to the definition of the project use cases and requirements
- Physical Layer Security CEA-Leti will work on the security at PHY layers. CEA-Leti will also investigate to what extent physical attacks (side channel and fault attacks) on the physical layer can impact its security, especially for novel techniques based on lattices or error-correcting codes (or other “post quantum” techniques). Using the state-of-the-art physical characterisation equipment (power measurement test bench, Electromagnetic emission measurement test bench, laser fault injection equipment, Electromagnetic pulses perturbation test bench, voltage glitching equipment, etc.), practical attacks can be emulated to evaluate the degree of feasibility and threat of such attacks in this project’s context. Countermeasures mitigating those risks shall be studied and implemented.

- Heterogeneous Radio Access The use of multiple heterogeneous radio access technologies and spectrum bands brings new challenges to the MAC design. For example, how to select and switch among multiple radio access technologies is key to both resource utilization and individual performance in terms of throughput and latency. CEA-Leti will study performance and limitations of LPWA solutions such as SigFox and LoRa, in terms of reliability, scalability, medium utilization, energy consumption, mobility support, flexibility. CEA-Leti will also improve the scalability of such technology by extending star to mesh LPWA networks. The second step will be to propose a dual technology network in which 5G and long-range technologies can be jointly used. CEA-Leti will investigate how to exploit the best of each technology offering a low-power time synchronization and achieving highly reliable communication.
E3Network designs an E-band transceiver for the backhaul infrastructure of future networks. It works in the E-band, which enables highly focused “pencil-beam” transmissions and huge bandwidth. The pencil-beam property facilitates a high degree of frequency reuse in the deployment of backhaul links and reduces EMF exposure. The transceiver will use modern digital multi-level modulations to achieve high spectral efficiency. This together with the huge bandwidth will enable high capacities above 10 Gbps.

The RF analogue front-end of the transceiver will be a highly integrated circuit using advanced SiGe BiCMOS technology, which enables energy and cost effectiveness. However, a consequence of transistors length reduction is an exponential increase of process variations, leading to over-constrained designs to guarantee sufficient post-fabrication performance yield. In order to achieve the required performance, a mixed analogue-digital design approach together with novel signal processing methods is applied.

Leti in E3Network

- Development of a mmW design kit extension for BiCMOS 55nm technology to provide high-frequency, reliable IC design.
- Development of a system level simulation platform and behavioral models for phase noise simulation from circuit level simulations and measurements.
- Proposal of a frequency plan for the E-Band transceiver and design of a dual local oscillator (LO) mmW frequency synthesizer for transmission (Tx) and reception (Rx) front-ends.
- Positioning of CEA-LETI on the emerging field of integrated mmW transceiver solutions for applications in backhauling, small cell, 5G and other high-speed and high-data rate wireless communications.
- Contribution to leveraging a promising new SiGe BiCMOS technology developed by STMicroelectronics for high-speed, high-performance markets such as the cellular infrastructure, optical communications and radar ICs.
- Participation in first attempt to develop a fully integrated 10Gbps wireless transceiver for medium range communication (1km) in E-Band in partnership with major industrial partners (Alcatel-Lucent, now Nokia – STMicroelectronics).
- Experimental validation of CEA-LETI’s recently proposed new methods of generating mmW multiple-LO frequencies based on using pulsed and injection locked oscillators (1 Ph.D. thesis, 3 patents).
- Demonstration of 10 Gb/s, E-band wireless link implementing 64QAM modulation.
Leti in FANTASTIC5G

CEA-Leti is working on a flexible air interface for scalable service delivery, also known as new non-backward compatible radio access technology (3GPP NR).

Objectives are threefold:
1. Flexible, efficient use of all available non-contiguous spectra through an FBMC-based waveform (well localized frequency response);
2. Adaptation of the FBMC waveform to ensure compatibility with conventional LTE signaling and MIMO schemes;
3. Coexistence with legacy LTE systems.

CEA-Leti’s contributions comprise:
1. Proposing an FBMC-based PHY layer for MIMO (Mobile Broadband services) and short packets (Machine Type Communications) and ensuring compatibility with OFDM principles. This new waveform is called Block-Filtered OFDM (BF-OFDM);
3. Developing a real-time over-the-air HW demonstrator (digital base band FPGA/ARM and RF front-end) for assessing MIMO transmission performance in conjunction with the new 5G air interface.

CEA-Leti achievements to date:
1. Demonstration of an FBMC-based waveform compatible with MIMO;
2. Demonstration of spectral efficiency up to 12 bit/s/Hz (256-QAM, 2x2, 3/4);
3. Demonstration of coexistence with legacy OFDM-based transmission.

Fragmented spectrum usage can be addressed digitally:
1. A built-in digital filter of filterbank modulation allows for spectrum pooling;
2. A flexible frame structure and adaptive resource block allocation can be envisaged.

Proposed waveform features:
1. Prototype filter optimized for time and frequency localization trade-off;
2. Low adjacent leakage;
3. Quasi-orthogonality in complex domain;
4. Efficient IFFT/FFT implementation.

Benefits of the approach are its suitability for fragmented spectrum usage, its suitability of coexistence with the legacy, limited guard band standard and its compatibility with LTE concepts and well-known OFDM algorithms.
Leti in FLEX5GWARE

CEA-Leti is contributing to the following project areas:

- LDPCs are high-performance coding schemes designed for 5G. They are recognized as comparing favourably with turbo-codes for high-throughput applications because of the intrinsic capacity of their Message-Passing (MP) decoding algorithms to accommodate high degrees of parallelization. In Flex5Gware, CEA-Leti is working on the implementation of cost-effective, high-throughput LDPC decoders. The proposed approach relies on the use of imprecise computing and storage mechanisms designed to reduce the size of LDPC decoder memory and interconnect blocks, recognized as dominating overall performance of the hardware design. Implementation results show that proposed decoders allow significant improvements in terms of both throughput and hardware resources consumption compared with a baseline decoder and offer even better or only slightly degraded decoding performance;

- full Duplex Radio offers a capacity gain depending on the level of Self Interference Cancellation, which should be at least 65dB. Hybrid architecture is proposed, which combines an RF-digital canceller with a pure digital canceller. First experimental results show a 55dB gain. Simulations show that the limiting factor is transmitter noise, which creates the need for an additional IF self-interference stage and this will be considered in future work;

- OFDM/FBMC comparison in terms of implementation complexity. The FBMC architecture working flow has been studied and flexible FBMC receiver architecture has been reviewed. A flexible memory-based implementation approach has been investigated along with architecture-imposed requirements for hardware implementation. An area estimation and comparison (memory and combinational logic) of OFDM and FBMC has been performed for CMOS 65nm technology.

Publications

References

1. EC Programme H2020-ICT-14-2014 - Advanced 5G Network Infrastructure for the Future Internet

2. FLEX5GWARE Flexible and Efficient Hardware/software Platforms for 5G Network Elements and Devices

3. The overall objective of Flex5Gware is to deliver highly reconfigurable hardware (HW) platforms together with HW-agnostic software (SW) platforms targeting both network elements and devices and taking into account increased capacity, reduced energy footprint, as well as scalability and modularity, to enable a smooth transition from 4G mobile wireless systems to 5G. As argued in the proposal, this approach will be necessary so that 5G HW/SW platforms can meet the requirements imposed by the anticipated exponential growth in mobile data traffic (1000 fold increase) together with the large diversity of applications (from low bit-rate/power power for M2M to interactive and high resolution applications). Flex5Gware adopts a holistic approach, performing research and implementations on key building blocks of 5G (and cooperations among them) to provide versatile, flexible, reconfigurable, efficient operations for HW/SW platforms.

4. The development of this concept entails many system design challenges that will be solved through disruptive technologies. E.g., analogue components to enable massive MIMO for mmWave, full duplex (simultaneous transmission and reception) for 5G waveforms, or reconfigurable SW architectures with interface abstractions for flexible control and management mechanisms across heterogeneous wireless devices and access networks. Flex5Gware evaluates and demonstrates the developed 5G technologies, in terms of proofs-of-concept, which will be showcased in a demonstration event where all the partners in the consortium will participate. The Flex5Gware consortium includes large industry leaders from infrastructure providers, semiconductor manufacturers and network operators as well as leading research institutions and academia and is reinforced with the participation of three SMEs. This powerful consortium, together with the measures detailed in the proposal, ensure a huge impact of the Flex5Gware results.

5. Total budget € 7 993 m.

6. Contract Number 671563
Intelligent transport systems

Vehicular ad hoc networks

Localization technologies

Cooperative ITS for safe, connected cars and sustainable mobility

Keywords

Autonomous driving

Connected cars

Intelligent transport systems

Localization technologies

Navigation

Road users safety

Vehicular ad hoc networks

HIGHTS

High Precision Positioning For Cooperative-Intelligent Transport Systems

Foreseen Connected Intelligent Transport System (C-ITS) applications will require a precise knowledge of vehicles’ geographical positions. Unfortunately, conventional satellite-based navigation systems (e.g., GPS and Galileo) cannot provide sufficient accuracy levels in common operating environments (e.g., urban canyons, tunnels) or they may suffer from too large convergence times (cold start).

This project addresses this problem by combining satellite-based systems with inter-vehicle wireless communication and ranging technologies (e.g., IEEE 802.11p/ITS-G5, IR-UWB, 5G millimeter wave radios...), as well as on-board sensing capabilities (e.g., laser-scanners, camera-based lane detector, inertial units, wheel speed counter...). Relying on hybrid data fusion algorithms and cooperative protocol transactions, the goal is to enable highly-accurate and secure positioning with a constant quality of service (e.g., within 0.25m), but also dynamic mapping (i.e., retrieving the relative positions of passive and cooperative entities around each car).

The results are intended for integration into the facilities layer of ETSI C-ITS architecture and should thereby become available for various C-ITS applications in challenging use cases such as safety of vulnerable users and autonomous driving/platooning.

The project therefore contributes to the development of an enhanced European-wide positioning service platform based on Local Dynamic Maps and built on open European standards. Proof-of-concept systems developed in the project will combine infrastructure-based and infrastructure-free devices, reference test vehicles, cooperative communication means between road users and offline processing, and will be evaluated in representative vehicular contexts. The project finally aims at pushing and promoting the proposed solutions towards standardization bodies.

36 months

May 2015 > Apr. 2018

HIGHTS at a glance

Project Coordinator

Jacobs University Bremen (DE)

Partners

DE: German Aerospace Center, Bremen Automotive Systems, T21, Objective Software, Robert Bosch, Zignos
FR: BeSpoon, Eurecom, CEA-Leti
LU: FIBConsulting
NL: PaulsConsultancy, Tenis International
SE: Chalmers University of Technology Gothenburg

Total budget

€ 6 m.

EC Contribution

€ 6 m.

Contract Number

636537 - H2020

HIGHTS

High Precision Positioning For Cooperative-Intelligent Transport Systems

CEA-Leti is contributing to each of the five main fields of research and development embraced by the HIGHTS project:

1) Design of cooperative algorithms enabling high-precision positioning of both “ego” and neighboring vehicles (within ~ 0.2m location accuracy) with limited vehicle-to-vehicle (V2V) communication footprint in terms of channel congestion, overhead and latency. Design based on:

- Fusion/Filling of:
  - asynchronous positional data received from neighboring vehicles seen as virtual anchors (e.g., over ITS-G5/EUCE 802.11p links);
  - V2V range-dependent metrics (e.g., received power over ITS-G5/EUCE 802.11p links or accurate time of flight using Impulse Radio - Ultra Wideband technology);
  - GNSS (supporting various classes of performance);
  - other on-board sensors (e.g. inertial units, camera-based lane detector, etc.).
- Selection mechanisms integrating only the most informative contributions from neighboring vehicles (e.g., based on Bayesian performance bounds);
- Optimized V2V broadcast policies (i.e. controlling transmit power, message payload and transmit rate) to ensure quasi-constant localization accuracy while complying with ETSI decentralized congestion control mechanisms;
- Mitigation of harmful effects inherent to V2V cooperation at both signal processing and scheduling levels (e.g. space-time correlations of fused observations under constrained vehicle mobility, particles depletion in high-dimensional fusion filters, etc.);
- parametric V2V message approximation limiting the size of localization-specific payloads in transmitted packets.

2) Integration of adapted co-simulation tools (e.g. long-term traffic/mobility simulations combined with V2V radio channel and sensor error models) for realistic performance assessment (in progress).

3) Refinement of existing V2V radio channel models (e.g., geometry-based stochastic model implementation) and unprecedented vehicle-to-pedestrian channel sounding/characterization (pending).

4) Studies regarding the integrity/security of cooperative V2V radio links against jamming and interception attacks (pending).

5) HW/SW devices integration with high-accuracy (i.e. mesh) ranging capabilities based on Impulse Radio - Ultra Wideband (BeSpoon’s integrated circuits), contributing to the demonstration of GNSS-enabled V2V cooperative localization (in progress).

Publications

- “Robust Data Fusion for Cooperative Vehicular Localization In Grenoble”, M. Huang, B. Denis, J. Härri, D. Stuck, IEEE Intelligent Vehicles Symposium 2017 (IV’17), Fort Worth, Texas, June 2017.

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TRL 1 2 3 4 5 6 7 8 9
Leti in IBROW

CEA-Leti is focusing on specific vital operations within the IBROW project: clean room process developments, including wafer bonding, and in-situ characterizations of wafer bonding.

CEA-Leti evaluates manufacturability techniques for implementing the RTD on a silicon platform. Specifically, the institute coordinates development of III-V substrate bonding on process silicon based on direct bonding technology. This involves characterization of the incoming wafer, evaluation of standard and advanced surface preparation methods as well as bonding quality evaluation.

In this way, CEA-Leti:

- extends III-V-on-Si bonding expertise to new applications (and possibly new specifications/needs for the bonding technique);
- improves the robustness and ensures total control of III-V-on-Si bonding technology in close cooperation with III-V LAB, which develops optimized III-V epitaxial layers.

IBROW at a glance

The IBROW project addresses the growing requirement for high bit rate short range wireless communication. It is expected that very soon data traffic from wireless devices exceed that from wired devices. Forecast suggest that wireless data rates of multiple tens of Gbps will be required with a few years and this demand cannot be met with current technology. Resonant tunnelling diode (RTD) transceiver technology could provide the solution:

- low cost simple wireless transceiver architecture;
- already 10 Gbps is possible by exploiting the mm-wave and Thz frequency spectrum;
- up to 100 Gbps is feasible in the longer term.

IBROW develops a novel short range wireless communication transceiver technology that is:

- energy-efficient, compact and ultra-broadband;
- seamlessly interfaced with optical fibre networks;
- capable of addressing future network requirements.

IBROW achieves a novel RTD device technology on a III-V on Si platform integrated with laser diodes and photo-detectors. This approach offers a simple technology that can be integrated into both ends of a wireless link, consumer portable devices and fibre-optic supported base-stations.

IBROW Innovative ultra-BROADband ubiquitous Wireless communications through terahertz transceivers

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INSIGHT

Integration of III-V Nanowire Semiconductors for next Generation High Performance CMOS SOC Technologies

The overall objective is to enhance advanced CMOS RF and logic capability through the use of III-V heterostructure nanowires monolithically integrated on a silicon platform. INSIGHT focuses on:

- development and evaluation of the performance of silicon based, 94GHz III-V nanowire MOSFET low-noise amplifiers. The technology opens a path for cost reduction of key mm-wave components for high bandwidth wireless applications;
- development of III-V nanowire MOSFETs on Si with breakdown voltage of 6V, and evaluation of their performance in millimeter wave (60 GHz) power amplifier circuits. These devices will increase output power available from Si CMOS compatible mm-wave technologies with benefits for transmitter range and sensitivity;
- realization of basic building blocks for future RF-circuits including mixers, Voltage-Controlled Oscillators, and frequency dividers for precursors using silicon based III-V nanowire MOSFETs;
- development of science and technology for all-III-V nanowire CMOS technology, c) Circuit design library, d) Circuit demonstrators with a clear technology path towards higher TRLs and commercialization.

Our main outcomes include:

- Technology toolbox for achieving high performance devices. CEA-Leti activities address the full development cycle with a complete investigation from materials through devices to full circuit design and circuit evaluation for 90+GHz RF and mmW applications.
- For the first time, we have demonstrated 3D Monolithic (3DM) integration of In0.53GaAs nFETs on FDSOI Si CMOS featuring short-channel Replacement Metal Gate (RMG) InGaAs n-FinFETs on the top layer and Gate-First Si CMOS on the bottom layer with TiNW inter-layer contacts. State-of-the-art device integration has been achieved with the top layer InGaAs using a Raised Source Drain (RSD) and the bottom layer CMOS having Si RSD for nFETs, SiGe RSD for pFETs, implants, silicidie and TiNW plug contacts. The top layer InGaAs n-FinFETs are scaled down to Lg ~25nm and both the Si nFETs and pFETs in the bottom layer are scaled down to Lg ~15nm. Finally, by means of inter-layer contacts, we have demonstrated a densely integrated 3D 8T-SRAM circuit with InGaAs nFETs stacked on top of Si pFETs. This ensures a considerable reduction in area compared with a 2D layout.

Leti in INSIGHT

CEA-Leti is providing baseline CMOS processing capability for developing next generation circuits for high frequency devices, such as radio communication amplifiers (LNAs and PAs). Co-integration of III-V technology with Si CMOS and all-III-V CMOS technology is performed in conjunction with the project partners to investigate the benefits of II-V nanowire technology and to compare it with other available technologies. We have demonstrated very high performance at the transistor level and have proposed the most promising approaches to exploiting transistor properties at circuit level. INSIGHT project work builds on initiatives targeting III-V integration in Si technologies, specifically focusing on trends in RF and mmW applications, which require new developments for achieving high performance devices. Leti activities address the full development cycle with a complete investigation from materials through devices to full circuit design and circuit evaluation for 90+GHz RF and mmW applications.

36 months
Dec. 2015 > Nov. 2018

INSIGHT at a glance

- Project Coordinator
  Lund University (SE)

- Partners
  CH: IBM Research
  DE: Fraunhofer IAF
  FR: CEA-Leti
  IE: University College Cork - Tyndall
  UK: University of Glasgow

- Total budget
  € 4.25 m.
  EC Contribution
  € 3.5 m.

- Contract Number
  688784

- Cross-section TEM images show:
  (a) InGaAs n-FET on Si FDSOI, (b) 22nm Lg InGaAs nFET, (c) 7nm Lg InGaAs nFET, (d) 25nm Lg InGaAs n-FinFET and (e) top-view of 2D and 3D inverter.

Publications
- “First Demonstration of 3D SRAM Through 3D Monolithic Integration of InGaAs n-FinFETs on FDSOI Si CMOS with Inter-layer Contacts.” V. Deshpande et al. 2017 Symposium on VLSI Technology, Kyoto.

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Hervé Boutry, herve.boutry@cea.fr
1.6 m.
EC Contribution
2.2 m.
Total budget
€ 2.2 m.
€ 1.6 m.
Contract Number
309129

Leti in i-RISC

CEA-Leti’s contributions to the i-RISC project is aimed at advancing knowledge and understanding of error-correcting codes in the context of unreliable systems from two complementary perspectives: (i) their ability to provide reliable error protection if they themselves operate on unreliable hardware, and (ii) the development of specific methods to embed error correcting techniques into the circuit design, such that fault-tolerant circuit design is achieved. A first contribution has been to develop the theoretical analysis and to propose practical designs of error correcting codes with fault-tolerant encoder and decoder architectures. A second contribution has been to develop the mathematical models and theory of error coding driven circuit synthesis to pave the way for new and more powerful fault-tolerance techniques, which will be inherently a prerequisite for designing forthcoming nanoelectronic devices.

The main outcomes can be summarized as follows:

- error models that cover the effects of crisp sub-powering, production imperfections, environmental deterioration and aging. The effects of energy consumption, clock frequency, environmental conditions and area requirements on circuit error probability has also been investigated;
- analysis and design of error correcting encoders and decoders able to provide reliable error correction even if they are made out of unreliable components. In contrast to the traditional use of error correcting codes, faulty hardware represents a new source of errors that can perturb the encoding and/or decoding process;
- design of fault tolerance techniques by combining the codec architecture with the hardware it protects. Proposed solutions exploit the links between graph representations of digital circuits and of error correcting codes, thereby generating fault tolerant implementations.

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The ongoing miniaturization of data processing and storage devices and the imperative of low-energy consumption can only be sustained through low-powered components. Lower supply voltages and variations in technological process of emerging nanoelectronic devices make them inherently unreliable. As a consequence, the nanoscale integration of chips built out of unreliable components has emerged as one of the most critical challenges for the next-generation electronic circuit design. To make such nanoscale integration economically viable, new solutions for efficient and fault-tolerant data processing and storage must now be invented. The i-RISC project aims at achieving these goals, by providing innovative fault-tolerant solutions at both device- and system-level that are fundamentally rooted in mathematical models, algorithms, and techniques of information theory. Proposed solutions will build on error correcting codes and encoder/decoder architectures able to provide reliable error protection even if they themselves operate on unreliable hardware. The project will develop the scientific foundation and provide a first proof-of-concept by validating the proposed solutions on accurate error models and energy measurement tools developed within the project. In the forthcoming challenge of nanoscale technologies, the i-RISC project is an essential prerequisite for preparing the European industry for this paradigm shift.

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Millimeter Wave Massive Arrays Enabling Rfid/Radar Applications on 5G Smartphones

MAPS

Nowadays, a rising interest is moving towards the fifth generation (5G) of wireless mobile communication, as numerous devices and different heterogeneous networks will be interconnected, guaranteeing zero-distance connectivity between people, devices and objects. To deal with the ever increasing data traffic demand and the low power consumption requirements in the perspective of a sustainable growth, smart solutions have to provide energy- and cost-efficient services. In this context, the massive antenna arrays deployment in base stations, access points or mobile devices, appears like a viable solution to meet these new challenges. Besides communication, the availability of such a technology can also offer interesting applications such as accurate simultaneous localization and mapping (SLAM) performed by a personal radar integrated in smartphones, enabling new services in the device-to-device communication. In addition, the interrogation of tagged objects placed in the environment through radiofrequency identification (RFID) technology will allow a mapping of the real world into the Internet space, enabling environment-related applications and constitute the so called smart space within the Internet of Things concept. Moreover, the reduced wavelength at millimeter-waves (mmWaves) opens the way for packing a large number of antenna elements into a small area, overcoming the difficult integration of laser-based or mechanical steering devices into mobiles. Thus, the MAPS main objectives can be summarized as follows:

- models assessment for propagation and backscattering from objects in indoor environments at mm-waves;
- development of personal radar using mmWaves massive arrays;
- development of mmWaves passive RFID using massive arrays;
- development of environment-learning radar algorithms exploiting massive arrays capabilities.

The general aim of MAPS is to study the feasibility and opportunities offered by integrated mmWave massive arrays in 5G smartphones for personal radar and RFID capabilities for environmental mapping and tagged object identification. This will enable different users to share their maps and information collected from integrated sensors and objects, thereby offering the potential for people, objects and devices to connect in real time. The aim is to go beyond the current state-of-the-art by introducing the innovative mmWave-based network, which is expected to be a major player for upcoming 5G technology.

CEA-Leti’s main outcomes in relation to the project objectives are:

- adoption of massive arrays for simultaneous localization and mapping (SLAM) or personal radar applications, enabling detection and localization of surrounding objects through an accurate beamforming procedure. When a conventional constant false alarm rate approach to an ideal-pencil beam pattern is adopted, signal detection ambiguities can arise because of side-lobes, which can cause significant errors in target detection and ranging.

The impact of massive array side-lobes on detection performance in personal radar applications has been demonstrated. To maintain antenna array complexity and minimize cost, simpler array architectures are must be considered at the expense of higher side-lobe level. This issue has been investigated using simulated data to provide evidence of the need to adopt a more robust detection and localization approach.

- joint conception of a massive array mask and a thresholding strategy robust in relation to interferers in the side-lobe direction has been shown to combat the above issue the proposed algorithm has been validated through simulated and measured data;

- a robust channel characterization of environment has been proposed starting from an office- and corridor-based measurement campaign. The most significant angular and temporal intra-cluster parameters have been derived and the inter-cluster statistics have been related to the environment characteristics with the objective to reproduce the channel, when the environment geometry is given as in mapping applications. Based on the given channel characterization, this offers the possibility of statistically reproducing the cluster and path distribution as required for environment mapping applications;

- the impact of different design parameters on mapping performance has been investigated, when mmwave massive arrays are used for personal radars applications. Using measured data and a grid-based Bayesian state space for map reconstruction, we have demonstrated the impact of different design parameters and of the cleaning approach for measured data;

- the feasibility and opportunities potentially offered by joint adoption of mmWave and radio-frequency identification (RFID) technologies have been studied. Firstly, an ad hoc reader-tag architecture has been proposed to describe the considered scheme. Secondly, we have used a 866GHz measurement campaign to ensure preliminary system validation. Subsequently, the possibility of localizing tags using beamsteering-based readers has been demonstrated.

Publications


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Beyond 2020 Heterogeneous Wireless Network with Millimeter Wave Small Cell Access and Backhauling

Providing broadband wireless communications to a majority of European citizens is a major objective of the EC at the horizon of 2020. With a current annual growth rate in the range of 70%, the mobile data traffic of smartphones, tablets, machine-to-machine and other portable devices dramatically challenges the 4G wireless cellular network currently under deployment. To sustain this growth, high data-rate millimeterwave (mmW) technologies, that demonstrate striking capabilities for short- and medium-range wireless communications, can bring a tremendous performance improvement.

MiWaveS develops the key technologies for the implementation of mmW wireless access and backhaul in future 3rd Generation heterogeneous cellular mobile networks, taking advantage of the wide unlicensed or light-licensed frequency bands available to allow flexible spectrum usage as well as peak capacities above 10 Gbit/s aggregated throughput, well beyond the LTE-Advanced system. Installed in dense urban environments, miniature mmW small-cell access-points connected to the cellular network through optical fibre or mmW wireless backhaul will support massive data exchanges for mobile users with low latency, low interferences, high QoS and low power consumption per bit. They will also contribute to a reduced exposure to the relevant areas for designing and demonstrating heterogeneous cellular networks with mmW access and backhaul.

MiWaveS at a glance

Project Coordinator
CEA-Leti (FR)

Partners
CH: OptiPrint AG
DE: Inter Mobile Communications, Signalon, Technische Universität Dresden
ES: Tecnologías Servicios Telemáticos y Sistemas
FI: Nokia Solutions and Networks
LV: Technologian Tutkimuskeskus
FR: CEA-Leti, Orange, ST-Microelectronics S.A., Université de Rennes 1
GB: University of Surrey
IT: Telecom Italia, ST-Microelectronics SRL
SE: Sivers

Total budget
€ 11.3 m.
EC Contribution
€ 7.4 m.

Integrated 60 GHz user terminal module: top and bottom side

CEA-Leti is contributing to development and demonstration of new concepts of flexible mmW phased-array and transmit array antennas with beam-switching and beam-steering capabilities for reconﬁgurable backhaul and mobile access in V-band. CEA-Leti has generated the following outcomes:

- development and demonstration of a V-band transceiver module for user terminal applications. This module includes a CMOS transceiver integrated with transmit and receive antennas in a compact organic package providing small-size, low-power and low-cost connectivity compatible with hand-held terminals requirements;
- based on the same CMOS transceiver chip, development of a new phased array architecture for V-band access points. Multi-chip front-end implementation, in which the transceiver is associated with multiple phase-shifting ICs to give cost effective, low power consumption, scalable architecture. BICMOS technology is used for the phase-shifting ICs to ensure higher transmit power and linearity; the phased array will be integrated into multi-layer organic technology through integrated antennas;
- development of beam-switching, high-gain, transmit array antennas for backhauling applications requiring auto-alignment functions. These antennas are composed of a transmit array panel on standard PCB technology and an active focal array including switching and phase-shifting functions. A dual structure of this type is needed to achieve the high gains required in backhaul applications.

Publications

- "Millimeter-wave access and backhauling: the solution to the exponential data traffic increase in 5G mobile communications systems?", F.C. Dehos et al., IEEE Communications Magazine, vol. 52, no. 8, Sept. 2014, p.88-95.
- "A strategy for research projects to impact standards and regulatory bodies - The approach of the EU-funded project MiWaveS", F. Francioso et al., IEEE Conf. on Standards for Communications and Networking (CSCN 2015), Tokyo, Japan, 28-30 Oct. 2015.

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MiWaveS
Beyond 2020 Heterogeneous Wireless Network with Millimeter Wave Small Cell Access and Backhauling

40 months
MiWEBA

Millimeter Wave Evolution for Backhaul and Access

Due to the explosion of mobile terminals, the data traffic on conventional networks could increase by 1000 times in next 10 years. To face capacity shortage, 5GPP studies heterogeneous networks (HetNet) with a mix of low-power base stations (BS) in the area of conventional ones. Alternative mmW systems like 802.11ad are not connected to cellular networks and restricted to AV equipment or bridge across buildings. This project conducted R&D of mmW overlay HetNet in which mmW ultra-broadband (UB) BS employs state-of-art technologies of mmW devices and integrated them into conventional networks. Through system design, standardization, and validation experiments, the project aimed to extend network capacity by 1000 times with reasonable cost and no loss of convenience to users. The mmW overlay HetNet consists of the backhaul/fronthaul (FH) connecting mmW UB-BS with the cellular network, an access link (AL) integrating both conventional LTE cellular AL and the novel mmW link, and a central controller to achieve seamless UE handover and dynamic BS resources’ control. With careful design of this system and performance numerical simulations, we aim to standardize FH at the ETSI C-u plane split. Data/control split: data plane was based on mmWave frequencies, control plane was assumed to be a typical 5G low-frequency link.

CEA-Leti’s major outcomes in the field of radio resource management:
- development of radio resource management solutions to raise energy efficiency in dense heterogeneous networks with millimeter wave small cells;
- extension of CEA-Leti’s system level simulator by integrating the mmWave environment and technologies (e.g. channel model and directive antennas) into legacy 4G systems;
- realistic characterizations for assessing future 5G mobile networks.

CEA-Leti’s major outcomes in the field of front and backhaul link design:
- MiWEBA has stimulated close cooperation between CEA-Leti’s Antenna Design and Algorithms laboratories;
- elevation and azimuth gains in antenna arrays at 60GHz carrier frequencies were measured and used to assess the feasibility of a moving hotspot (HS) scenario;
- realistic deployment was simulated for this scenario: usage case was tramway backhauling, i.e. a high-rate link between a fixed BS and a HS deployed on the tram roof;
- beam switching requirements were specified based on several parameters including distance between BS and HS and tram speed;
- multi Radio Access Technology (RAT) was also considered through data/control plane splitting: data plane was based on mmWave frequencies, control plane was assumed to be a typical 5G low-frequency link.

36 months
Jun. 2013 > May 2016

MIWEBA at a glance

Project Coordinator
FRAUNHOFER-GESellschaft zUR FOERDERUNG DER ANGEWANDTEN FORSCHUNG GmbH, Munich, Germany

Partners
Francois Guth, Head of Radio Access, Corporate Department of Innovation, Orange Labs, France

Total budget
€ 2 m. for Europe partners, 297,503,000 JPY for Japan

Contract Number
608637
Infrastructure for the Future

NEW

Advanced 5G Network
H2020 ICT-14-2014: EC Programme

Millimiter wave

Keywords
Code design
Antennas
users, supporting UHD/3D streaming, immersive applications and
ject will thus enable ultrafast mobile broadband services for mobile
and will be used as a foundation for global standardization. The pro-
This is envisaged as a key component in the 5G multi-RAT ecosystem
bile radio access technology (RAT) for mm-wave band deployment.

The mmMAGIC project will develop and design new concepts for mo-
ile radio access technology (RAT) for mm-wave band deployment. This is envisaged as a key component in the 5G multi-RAT ecosystem and will be used as a foundation for global standardization. The project will thus enable ultrafast mobile broadband services for mobile users, supporting UHD/3D streaming, immersive applications and ultra-responsive cloud services.

A new radio interface, including novel network management functions and architecture components will be proposed, taking as guidance 5G PPP’s KPI and exploiting the use of novel adaptive and cooperative beam-forming and tracking techniques to address the specific challenges of millimeter wave propagation. The project will undertake extensive radio channel measurements in the 6-100GHz range, and will develop and validate advanced channel models that will be used for rigorous validation and feasibility analysis of the proposed concepts and system, as well as for usage in regulatory and stan-
ards fora. The use of such extremely high frequencies for mobile communications is challenging but necessary for supporting 5G’s extreme mobile broadband service which will require very high (up to 10 Gbps) data rates, and in some scenarios, also very low end-to-end latencies (less than 5ms).

24 months
Jul. 2015 > Jun. 2017

mmMAGIC at a glance

Project Coordinator
Samsung (UK)

Partners
DE: Aixtel-Lucent Deutschland AG, Fraunhofer HHI, Huawei Technologies Dusseldorf GmbH, Intel Mobile, Rohde & Schwarz, Technische Universität Dresden
DK: Keysight Technologies
FR: IMOGA Networks Institute, Télécom ParisTech
IT: Aalto Univ., Nokia Solutions and Networks Oy NOK-N
NL: CEA-Leti, Orange
PL: Nokia Solutions and Networks
SE: Chalmers Univ., Ericsson AB, Gammcom
UK: Samsung Electronics, Univ. Bristol

Total budget
€ 8.2 m.

EC Contribution
€ 8.2 m.

Contract Number
671650

Let in mmMagic

Main mmMAGIC project outcomes contributed by CEA-Leti:
• development of an mmWave channel sounder providing wide bandwidth and antenna steering;
• mmWave channel measurement in indoor environments in E and V band. Characterization of channel properties, including spatial characteristics and frequency dependence. Development of a geometric stochastic channel model for 5G applications based on measurement results, in collaboration with the consortium;
• antenna solutions for access, backhaul and fronthaul applications. Investigation of antenna impairments and models to be used in system-level simulations taking into account usage case conditions. Analysis and design of transmit and phased arrays for BS and user mobile;
• design of 5G waveforms such as Block Filter- Orthogonal Frequency Division Multiplexing (BF-OFDM) and Filter Bank Multicarrier Modulation (FBMC). Waveform optimization considering different channel conditions (e.g. mobility, Line of Sight/Non Line of Sight conditions) and radio frequency hardware impairments. Investigation of compatibility and performance of candidate waveform with beamforming aspects;
• investigation of robustness of LDPC (Low Density Parity Check) decoders in relation to computation unit imprecisions, improvement of latency and power consumption. Theoretical analysis and practical designs of imprecise iterative decoders;
• software-based channel coder/decoder (C code) for Hardware in the Loop demonstration;
• participation in 5GPPP initiatives, dissemination and demonstration.

Publications
• “5G: 6–100 GHz Channel Characterisation”, 2015.

Publications
• “5G: 6–100 GHz Channel Characterisation”, 2015.

Bernard Strée, bernard.strée@cea.fr
Spintronics
Memory
Storage and Security Applications

The MOSAIC project builds on existing spintronics device level knowledge to address system level requirements as a first crucial step toward industrialization. Future generations of nanoelectronic components and systems will be driven by nano-engineered semiconductor, magnetic and insulating materials. Disruptive More than Moore paths to systems are provided by nano-scale microwave spintronics components due to firstly their unique spin polarized transport properties that appear only at nanoscale dimensions (<100nm). Beyond previous device research, the project targets technological breakthroughs in generating, processing (mix, modulate, synchronize) microwave properties including signal generation, processing and detection properties that appear only at nanoscale dimensions (<100nm). Functional nanofabricated devices as small as 75nm have also been produced, while nanofabricated devices have also been fabricated from magnetic stacks deposited by partner INL in vortex and homogeneous configurations.

Working towards system level demonstrations, STNOs have been integrated within a compact phase locked loop (PLL), developed by TU Dresden, and based on custom-integrated circuits for validating the generation function. Significant phase noise reduction has been achieved, providing a positive step towards integrated, hybrid systems for accurate frequency generation using STNOs. Proof of concept for frequency detection in the 200-500MHz range using standalone vortex devices and the known rectification effect (RF current excitation converted into DC voltage) has also been demonstrated. A new phenomenon, namely resonant expulsion of a magnetic vortex, has been demonstrated by CNRS Thales and produces a sharp variation in voltage at the resonant frequency. Using this effect and resonant frequency dependence on device diameter, simultaneous detection of different RF signals has been demonstrated in a first proof of principle that will lead to development of a new type of nanoscale RF threshold detector. STDOs also provide a novel approach to signal mixing and modulation, in which the same device can generate the signal via DC current injection and modulate it through an additional RF current at frequencies that are below the STO generation frequency. For uniform devices, it has been shown that, under sinusoidal current modulation, the maximum modulation rate for frequency and amplitude modulation is determined by the amplitude relaxation frequency \( f_p \) of the order of a few tens to a few hundred MHz. Digital frequency shift keying has demonstrated data rates up to 60Mbps for various devices, providing insight into future wireless communication systems for wireless sensor networks.

Leti in MOSAIC EU

CEA-Leti is leading the Spintronics device production work. Together with other project partners, its role is to coordinate and develop the magnetic tunnel junction stacks and nanofabrication processes required to build nanoscale spin torque oscillators. The institute is specifically involved in demonstrating two magnetic configurations: free layers with a homogeneous magnetic configuration and free layers with a vortex configuration. Numerous runs of nanoscale spin torque oscillators have been produced. Magnetic stacks with a resistance/area ratio as small as 13μΩμm² and with a tunable magnetoresistance ratio (TMR) of 100% have been built and are reproducible. Functional nanofabricated devices as small as 75nm have also been produced, while nanofabricated devices have also been fabricated from magnetic stacks deposited by partner INL in vortex and homogeneous configurations.

Publications

Marie-Claire Cyrille, marie-claire.cyrille@cea.fr

Leti in MOSAIC EU

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With the advent of 5G, traffic exponential growth may lead to the concept of spectrum crunch. SPEED-5G proposes to rely on a 3-dimensional model (densification, multi-technology, additional spectrum) referred to as extended-DSA (eDSA), where several technologies are considered and managed in order to improve spectrum availability along with the exploitation of a collection of technologies to support capacity increase and service provision without impacting quality of experience or even with improving it. SPEED-5G develops innovative cloud-based architecture for ultra-dense networks based on a mix of centralised and decentralised resource management techniques, which coordinate a group of small cells so that interference can be managed taking into consideration opportunistic access on sub-6GHz spectrum resources having diverse licensing regimes. Small cells implement a multi-RAT MAC able to apply resource management decisions on a local basis and to efficiently steer traffic on these bands, considering new waveforms like filterbank multicarrier (FBMC). SPEED-5G is committed to investigate on the RRM/MAC framework and will implement the most promising solutions to show the gain improvement on broadband traffic patterns, using a testbed which integrates HW platforms covering real-time MAC, wireless backhauling and virtualised resource management.

Leti in SPEED-5G

CEA-Leti’s main contributions to SPEED-5G involve MAC design and resource management for 5G traffic. On the MAC side, the institute is extending research into a new FBMC-type waveform by defining medium access methods aimed at exploiting specific features of reduced out-of-band emissions. On the RRM side, CEA-Leti is contributing resource allocation mechanisms capable of coping with 5G traffic patterns with various Quality-of-Service (QoS) requirements.

Project outcomes are:
- specification and validation of a MAC protocol for broadband traffic supporting various qualities of service (QoS) requirements, operating on the 5 GHz band and complying with the European regulation;
- development of this protocol on a custom hardware platform to achieve its real-time implementation and its project testbed integration;
- over-the-air demonstration of the MAC real-time implementation; operation in 5GHz band is planned as well as the migration in the 3.5 GHz band, supporting the CEA-Leti 5G technology validation field trial;
- contribution to the IEEE 1900.7 standardisation process. The aim is to support QoS by defining new MAC extensions to the IEEE 1900.7-2015 standard (PHY/MAC specifications for TV WS operation).

Ensuring the design and validation by simulation of resource management algorithms for efficient heterogeneous traffic steering on unlicensed spectrum using reinforcement learning.

Development and performance assessment of dynamic channel selection strategy using the probabilistic framework of the multi-armed bandit.

Conducting a study comparing the performance provided by 5G waveforms and that provided by the LTE legacy waveform in realistic conditions of coexistence with Wi-Fi networks.
TOPAs

Tools for cOntinuous Building Performance Auditing

TOPAs will link building performance (prediction) models to operational Building Management Systems (BMSs) and measurement technologies to improve prediction model accuracy models and in-use building performance.

TOPAs adopts the principle of continuous performance auditing and considers not only energy use, but also an understanding of how buildings are used and their climatic state (environmental & air quality). The program implements a holistic performance audit process through supporting tools and methodologies that minimize the gap between predicted and actual energy use.

CEA-Leti is deploying LINC middleware to coordinate the TOPAs tools and data. Deployment will be undertaken on MSIL Remote Terminal Units and on a selected Cloud platform.

CEA-Leti will gain expertise in building modeling and management systems. This expertise could be transferred to CEA-Leti startup Bag-Era.

TOPAs at a glance

36 months
Nov. 2015 - Oct. 2018

Project Coordinator
Motorola Solutions Israel Ltd (MSIL)

Partners
DE: Fraunhofer Gesellschaft für angewandte Forschung e.V., Technische Universität Dresden
FR: Azimut Monitoring, EMBIX, CEA-Leti
IE: Cork Institute of Technology, Energy Solutions, IBM Research
IL: Motorola Solutions Israel Ltd

Total budget
€ 6.1 m.
EC Contribution
€ 5 m.

Contract Number
676760

Publications

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Leti in Wise-IoT

Within the scope of the WISE-IoT project, CEA-Leti is providing its IoT data collection and processing platform, sensiNact. This comprises a software platform enabling the collection, processing and redistribution of IoT data relevant to improving people’s quality of life via various applications from domains such as smart city, smart home, smart transport, etc. SensiNact provides programming interfaces for different data access modes (on-demand, periodic, historical, etc.) along with application development and deployment for easily, quickly building innovative applications on top of the platform.

The Wise-IoT project allows interoperability of sensiNact with other European and Korean IoT platforms, such as FIWARE, Mobius (open source OneM2M implementation) and Oliot (open source GS1 implementation), by creating specific adapters for each of these platforms.

CEA-Leti is more specifically involved in a smart ski usage case at a ski resort near Grenoble. The sensiNact platform is used in a scenario, in which skiers are fitted with LORA connectivity-enabled sensors that measure their performance and location, and provide them with personalized recommendations. sensiNact ensures easy integration with other collected data on detecting crowded areas, measuring snow quality and depth, detecting emergency situations, etc. The platform allows the ski resort to use the collected data for better managing resources.

Final simultaneous deployment of the smart ski usage case in France and Korea is planned for the 2018 Winter Olympic Games in Pyeongchang.
Leti in BEAT

Within the scope of the BEAT project, CEA-Leti is:

- Performing vulnerability analyses of biometric systems, defining countermeasures and providing tools to "spoof" fingerprinting systems.

Extensive testing of biometrics systems is required and a methodology for spoof creation has been developed and formalized in a database. This database is an extension of published state-of-the-art information and includes highly innovative materials and methods. All materials are freely available at “home improvements” or “artistic hobby” stores. CEA-Leti is the main contributor of methods of spoofing fingerprint systems.

- Working towards testing protocol standardization and Common Criteria (CC) evaluation of biometric systems. A document describing how a biometrics system can be evaluated under the Common Criteria context has been produced. This methodology covers the various aspects of an evaluation:
  - security target content requirements;
  - common criteria tasks to be included in an evaluation;
  - specific characteristics of biometric system testing;
  - methodology for vulnerability analysis and attack potential rating.

- Providing examples of applying this methodology to standard systems and example of attacks rating. CEA-Leti is the main contributor for the vulnerability analysis and assessment part of the methodology. This method and the examples show that biometrics systems can be certified at various levels of Common Criteria (EAL1 to EAL4) with resistance up to “enhanced basic” or “moderate”.

- Inputs to ISO for standardization. The methodology document has been submitted to ISO in the context of standardization of evaluation methodology. BEAT is mentioned as a main contributor for vulnerability assessment.
Leti in PRISMACLOUD

CEA-Leti has contributed to PRISMACLOUD as follows:

- performance of risk analysis for some pilot use cases to showcase the benefit of the new cryptographic tools developed within the project. Requirements for future Common Criteria (ISO/IEC 15408) evaluations will be issued;
- evaluation of the sensitivity of the cryptographic primitives developed in the project to physical attack (side-channel and fault injection). From the start, this will help identification of the critical portions of algorithms requiring special care to ensure secure implementation. Insertion of suitable countermeasures will then be considered at an early stage of implementation specification drafting;
- implementation of a redactable signature scheme that is robust to quantum computer attacks. This redactable scheme will serve as a selective disclosure component that could be used in the e-health or smart-cities use cases. Redactable signature uses a conventional signature as a core component, but it is vulnerable to attacks based on Shor’s algorithm implemented over a quantum computer. The post-quantum resistance requirement prompts selection of different technology, namely lattice-based cryptography. The state-of-the-art of lattice-based signature scheme implementation was reviewed to select the most efficient algorithm for integration into CEA-Leti’s redactable scheme. The Bimodal Lattice Signature Scheme (BLISS) was finally selected because it is efficient, sufficiently mature and backed by the SAFECrypto project (ICT-644729, http://wwwSAFEcrypto.eu);
- hardware implementation for a redactable signature scheme designed to ensure tamper resistance and high speed. Correct hardware implementation of a strong cryptographic algorithm is not necessarily secure because secret key data may leak through physical measurements such as power consumption, electromagnetic radiation or the timing of operations. This vulnerability has led to a large number of attacks, denoted side-channel attacks. The literature proposes countermeasures to defeat such attacks. CEA-Leti’s hardware specifications will take into account major attacks and incorporate adequate countermeasures. Specific measures dedicated to the main BLISS modules (e.g. NTT and Gaussian sampler) have been identified;
- implementation has started and a demonstration is planned for/was performed in August 2017. Implementation security will be evaluated by penetration tests (side-channel attacks).

EC Programme
H2020 ICT-32-2014 - Cybersecurity, Trustworthy ICT

PRISMACLOUD Privacy and Security Maintaining Services in the Cloud

Today, cloud computing is already omnipresent and starts pervading all aspects of our life, whether in the private area or in the business domain. In order to address the challenges and to enable the implementation of services with the intended security properties, a set of goals for the PRISMACLOUD project has been identified. In particular, the goals are:

- development of cryptographic tools to protect the security of data during its lifecycle in the cloud;
- development of cryptographic tools and methods to protect privacy of users;
- creation of enabling technologies for cloud infrastructures;
- development of a methodology for secure service composition;
- experimental evaluation and validation of project results.
Sociotal
Creating a socially aware citizen-centric Internet of Things

SOCIOTAL addresses a crucial next step in the transformation of an emerging business driven Internet of Things (IoT) infrastructure into an all-inclusive one for the society by accelerating the creation of a socially aware citizen-centric Internet of Things. It will close the emerging gap between business centric IoT enterprise systems and citizen provided infrastructure. SOCIOTAL will establish an IoT eco-system that puts trust, user control and transparency at its heart in order to gain the confidence of everyday users and citizens. Providing adequate socially aware tools and mechanisms that simplify complexity and lower the barriers of entry will encourage citizen participation in the Internet of Things. This will add a novel and rich dimension to the emerging IoT ecosystem, providing a wealth of opportunities for the creation of new services and applications that address true societal needs and allow the improvement of the quality of life across European cities and communities. SOCIOTAL builds on the foundations of emerging IoT architectures and introduces the following innovative key target outcomes, ensuring that privacy and trust are deeply embedded in the resulting architecture:

1) A governance, trust and reputation framework combining a set of innovative enablers that addresses the challenges of massive crowdsourced IoT infrastructure
2) A privacy-preserving context-sensitive communication framework for IoT devices with adequate security enablers
3) A detailed understanding of technological and socio-economic barriers for citizen participation in an IoT
4) An intuitive environment inspired by social media tools that provides increased awareness and control and empowers citizens to easily manage access to IoT devices and information, while allowing IoT enabled citizen centric services to be created through open community APIs
5) Services piloted in two cities demonstrating the value of SOCIOTAL to real world communities

Leti in SocIoTal

Architecture specification: CEA-Leti is providing the final architecture of the Sociotal platform. Based on FI-Ware and integrating the IoT-A provided Architectural Reference Model (ARM), the Sociotal platform introduces new user-centric modules and enablers that offer security and privacy management services to manage the security and the privacy. New components have been introduced to hide the identity of persons or to manage their reputation. Sociotal therefore provides a consistent, integrated platform that ensures security and privacy through its design and end-to-end security guarantee.

Open API for service development: CEA-Leti is providing open API for integrating devices based on heterogeneous protocols and data models. Based on a strong framework, the programmer can focus on the protocol logic and data model alignment.

Reputation management: a radio location engine has been developed and integrated into the SenSiact gateway environment to feed location-based Reputation and Trust (RT) mechanisms. MDknaps can now be positioned in 2D, relying on received power (RSSI) measurements with respect to IEEE802.15.4-compliant anchor nodes disseminated in the environment. Time-stamped measurements and estimated position are thus pushed as context information. Field validations have been conducted in a typical indoor environment.

Geo-localization enabler: a demonstrator has been developed to geo-locate a person wearing a “sink”-type connected object in a building has been realized. Thanks to anchors disseminated in the environment, the 2D coordinates of a person are accessible to any person authorized to consult, so part of the user community. An enabler has been specially developed to follow the path of the person wearing the sink on the building map.

Secret key management: CEA-Leti has finalized Secret Key Generation (SKG) studies at radio physical layer level. This approach offers a flexible ad hoc alternative to conventional key distribution technique, thus contributing to secure group communications. More specifically, we have considered SKG out of reciprocal multipath channel information using real low-power integrated devices. A new quantization scheme has been proposed to adapt better the channel impulse responses acquired by real devices. Resulting raw keys exhibit fine randomness properties and fairly large length per channel probing.

Service Creation Environment: CEA-Leti has developed a studio for developing services for the Sociotal platform. Based on the well-known Eclipse IDE, this facility offers an intuitive way of guiding the user through best practices, helping him to select devices based on their trust and reputation. The application can be deployed and monitored in a few clicks, which gives a rapid feedback capability for rapid prototyping of IoT applications.

37 months

Sociotal at a glance

Project Coordinator
Université de Surrey (GB)

Partners
ES: Universidad de Cantabria, Universidad de Málaga
FR: CEA-Leti
NL: Van Ingeningen, Robbert Jan
NL: City of Nieuw Spaarne, Deltawoningen

Total budget
€ 3.5 m.
EC Contribution
€ 2.8 m.

Contract Number
609112
Image & Vision
Leti in EUROSKY

Conducted on simulation data, this study compares the performance of 3 detectors: a typical dual energy sandwich detector, a realistic model of the commercial ME100 V2 multi-energy detector provided by MULTIX and an ME100 «Cargo», which is an upcoming modified multi-energy version of the ME100 more suited to air freight inspection. The criterion used for this assessment is the Effective Atomic Number (Zeff) or contrast-to-noise ratio. Zeff is the physical parameter that allows material discrimination. The results reveal better performance in multi-energy detectors than in conventional dual energy «sandwich» (DE-S): a 1.5x factor in favor of the current ME100 V2 and a 2.2x factor for the ME100 (average value depending on the material pair tested). The ME100 V2 detector suffers from its small pixel size, which reduces the photonic statistics by a factor of 3 compared of the other 2 models.

The DE-S is logically favorable in relation to the penetration power criterion (the «DARC alarm») because of its higher stopping power.

CEA-Leti has also studied the case of overlapping materials in a dual view approach: one giving dimensional values, the other providing spectral data for assessing the effective atomic number (Zeff). The method developed by CEA-Leti for overlap correction has been extended to the multi-layer case with additional thickness simulating a container. We have shown that multi-energy detectors offer better performance than the dual energy «sandwich» detector due to noise reduction and more significantly lack of bias; a fundamental criterion for material identification.

Finally, a first approach multi-view system has been developed. The simulation result shows a performance breakdown of between 10 and 15 views.

EUROSKY
Single European Secure Air-cargo Space

EUROSKY will deliver a high impact program for improved air-cargo security and facilitation to safeguard international supply chains and the security of citizens whilst fostering international co-operation and a broad stakeholder engagement from all segments of the industry. The main project objectives are:

- provide systemic solutions for European air cargo security addressing prevailing complexities and vulnerabilities aligned with international initiatives and building on complementary on-going projects;
- offer different stakeholder groups enhanced capabilities for integrating preventive and reactive controls to address their threats in a timely and effective manner with optimized cost;
- secure air cargo supply chains whilst also facilitating the overall process (i.e. achieving security without stoppages, keeping the cargo movements unimpeded at all times).

EUROSKY at a glance

- Project Coordinator
  BMT GROUP LIMITED (GB)

- Partners
  BE: European Organisation for Security SCRL
  CH: Conceptivity SARL, Swissport International AG
  ES: Enide Solutions S.L., Idom Ingenieria y Consultoría S.A., Ingeniería Idom Internacional S.A.
  FR: CEA-Leti, Multix SA
  GR: Diethnis Aerolimenas Athinon AE
  IT: Consorzio IB Innovation, Fast Freight Marconi SPA
  PT: SPOH Servicos Portugueses de Hand, Urbanos-Grupo SGPS SA
  SE: Totalforsvarets Forskninginstitut

- Total budget
  € 18.9 m.

- EC Contribution
  € 11.7 m.

- Contract Number
  312649
HiLiCo
High Luminescence In Cockpit

Although the market demand of displays bright enough to allow the diffusion of readable information against a very bright landscape is important, in particular in the avionics application, existing technologies still do not allow the desired brightness combined with very low power consumption and very compact volume.

In this context, the HiLiCo project aims at developing a new generation of monochrome and full-color emissive GaN microdisplays with 1920x1200 pixel resolution (WUXGA), 8-μm pixel pitch, very high brightness (over 1MCD/cm²) and good form factor capabilities that will enable the design of ground breaking compact see-through system for next generation Avionics applications.

To achieve this aim, HiLiCo will address the following challenges:

- development of high-quality GaN based LED epilayers designed to fulfill targeted demonstrator performances;
- design and fabrication of an active matrix in advanced Complementary metal oxide semi-conductor (CMOS) technology to control each individual pixel;
- coupling of the LED structure and the CMOS, building a monolithic structure on which LED arrays will be fabricated with high precision, thus making monochrome, active-matrix, high-resolution GaN micro-displays;
- addition of colour converters (quantum dots and 2D Multi-Quantum Wells layers) on such blue emitting devices, for fabricating bi-color and full-color display demonstrators;
- design and manufacture of the electronics followed by the test and evaluation of the complete micro display device. First demonstrators will be qualified for future commercialisation.

The technology developed will contribute to the increase of European competitiveness, through the rapid and important deployment of innovative products on the microdisplays market, as well as Head-Up Displays, Head-mounted displays and smart Eyewears.

The consortium gathers 1 RTO, 1 large company and 2 SMEs. They will mobilise a grant of 4 091 583 € with an effort of 283 PM.

HiLiCo at a glance

- Project Coordinator
  CEA-Leti (FR)
- Partners
  CH: Novagan
  FR: CEA-Leti, Microoled, Nexdot
- Total budget
  € 4.1 m.
- EC Contribution
  € 4.1 m.
- Contract Number
  755497

EC Programme
NA

Keywords
Avionics
Brightness
CMOS
Cockpit
Full-colour
Gallium Nitride (GaN)
High small pitch
Integration
LED
Microdisplays
MicroLEDs
Monolithic
Quantum dot

High-resolution Monochrome GaN microdisplay:

Concept of Hilico’s color GaN microdisplay and high resolution monochrome GaN microdisplay:

Color Micro-LEDs

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TRL
36 months

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NEW
Lidar remote sensing of the earth’s atmosphere is one of the main challenges in coping with the effects and causes of global warming caused by the emission of greenhouse gases. The present operating Lidar missions are all implanted on large satellite platforms due to the size of the telescope and high energy laser modules required to ensure a sufficient collection of light to extract the signal from the detector noise. The principal objective of HOLDON project is to develop a new detection chain which will improve the performance of the Lidars on large platforms and/or reduce the Lidar payload to be integrated in the future micro and mini-satellites. The performance increase is obtained by the optimization of HgCdTe avalanche photodiodes that will be hybridized to a CMOS Readout Circuit providing two operation modes and designed to meet the most demanding requirements for Lidar applications in terms of sensitivity, dynamic range and temporal resolution.

To achieve these goals, a team of 7 partners, leaders in the different fields related to Lidar missions, will collaborate (4 represented EU member states). To this end, three ambitious objectives are defined: design and build a cutting-edge photon noise limited Lidar detection chain; validate adequation between detection chain key performances and future space mission requirements; demonstrate the improvement achieved with the cutting-edge detection chain for greenhouse gases detection.

HOLDON at a glance

- Project Coordinator
  CEA-Leti (FR)
- Partners
  CH: IDQuantique
  DE: Deutsches Zentrum für Luft- und Raumfahrt
  FR: Absiskey, Airbus Defence and Space, École Polytechnique
  CH: Laboratoire de Météorologie Dynamique
- Total budget
  € 2.5 M.
- EC Contribution
  € 2.5 M.
- Contract Number
  776390

Let in HOLDON

A Lidar detection chain based on HgCdTe APD directly hybridized with a custom designed CMOS ROIC will be designed and fabricated by CEA-Leti. This detection chain will enable to detect the signal with a photon noise limited SNR over the full optical dynamic range of space Lidar signals, up to 60 dB, down to signal fluxes below a single photon per observation time. In addition, the observation time and corresponding bandwidth of the detector is intended to be adjustable and on chip functionalities will be available in order to provide a versatile detector that can address a wide range of Lidar applications.

HgCdTe APDs have the unique advantage to combine a high quantum efficiency with a close to deterministic avalanche gain that enables to amplify the signal to a level that is higher than the electronic amplifier noise, with a close to negligible loss of information. The optimization of the APD performance in terms of increased quantum efficiency and useful APD gain, reduced excess and dark noise, reduced remanence (temporal lag induced by a strong signal) and increased spectral range will be addressed by the optimization of the APD architecture, technology and optical coupling. This optimization will add to the functionality of the detector and increase its versatility. This optimization aims in particular to use hetero structure APDs made with molecular beam epitaxy to reduce diffusion dark and tunnel currents, which limit the operating temperature and the maximum gain. The use of heterostructures will also enable the study of new APD architectures which should minimize the temporal lag. In addition, the quantum efficiency of the APDs will be maximized while minimizing the response time and dark current by the optimization of the optical coupling to the APD using μ-lenses that will be manufactured directly on the backside of the detectors.

The achievement of a dynamic range of 60 dB with a minimal signal level less than a single photon for variable temporal resolutions constitutes disruptive performances which will be achieved by direct hybridization of optimized HgCdTe APDs with a specifically designed CMOS ROIC providing two modes of operation: an on-chip sampling mode with variable observation time, gain and accumulation capability; a continuous mode for conventional sampling on the proximity electronics.
Leti in LOMID

CEA-Leti research teams are focusing on the following activities to ensure improved flexible OLED microdisplay performance and life:

- strengthening of thin-film encapsulation of OLED circuits;
- development of a reliable hard coat packaging layer based on sol-gel technology to replace the OLED microdisplay glass top;
- successful development of a die-scale thinning process to reduce chip silicon thickness to 100µm;
- demonstration of a curved OLED circuit (passive) thinned to 100µm and curved to a 45mm radius of curvature;
- implementation of CEA-Leti’s proprietary thin-film encapsulation technology in the 1” diagonal, LOMID display demonstrator.

© CEA-Leti
MESMERISE
Multi-Energy High Resolution Modular Scan System for Internal and External Concealed Commodities

Most people are familiarized with the inconvenience of having to go through a “hand search pat down” in airports check points. Apart from being invasive and privacy disruptive, the whole procedure significantly slows down the flow of passengers, which means even longer waiting queues. Additionally, in the case of wave body scanners the use of sexually explicit images that have to be interpreted by an agent arises some concerns about user’s privacy and dignity. The main challenge of MESMERISE is to develop a new scanning technology improving the respect for intimacy and privacy rights as well as the efficiency and reliability. In order to achieve this, the project first objective is to develop a high-resolution non-intrusive scanner able to automatically detect and identify both internal and external concealed prohibited or restricted commodities sought by customs. Mesmerise proposes two complementary technologies to fill the current gaps: ultra-low dose Multispectral X-ray transmission and Infrasonic interrogation. Both systems have the goals of improving privacy, convenience, sensitivity and reliability posing no risk for users, providing automatic identification or classification and assuring that no human operator needs to watch privacy-breaking images.

36 months
May 2016 > Apr. 2019

MESMERISE at a glance

Project Coordinator
Universidad de Alcala (SP)

Partners
BY: Adani UE
DE: BPE International Dr Hornig GmbH
FR: CEA-Leti, MultiX SA
GB: Home Office
NO: Customs region Oslo
RD: University «Dunarea de Jos» of Galati
SP: Centro De Investigaciones Energeticas, Medioambientales Y Tecnologicas-Ciemat, Ministerio del Interior, San Jorge Tecnologicas S.L.

Total budget
€ 5 m.
EC Contribution
€ 5 m.

Contract Number
700399

MESMERISE
Multi-Energy High Resolution Modular Scan System for Internal and External Concealed Commodities

Leti in MESMERISE

CEA-Leti has recently developed a sensitive photon-counting X-ray detector based on Cd(Zn)Te semi-conductor technology, which has been transferred to MULTIX (spin-off company of Thales and CEA). This company now offers a commercial product called ME100 for baggage screening. Innovative X-ray detectors of this type count individual photons and sort them into selected energy bins. The information provided is more complete, the analysis more thorough and the capacity for discriminating different objects and materials is enhanced. MultiX detector technology is able to discriminate liquids from solids: it can even distinguish regular from diet Coke, for example!

CEA-Leti’s task with the MESMERISE project is to develop an algorithm for embedding in the multi-energy X-ray sensor to optimize sensitivity of illicit product detection (e.g. cash, swallowed drug packet, surgically implanted bomb, etc.) concealed in or on the body. The aim is to adapt the multi-energy method to human body inspection. The challenge is to conciliate a very low dose X-ray scan and automatic detection with a low false alarm rate.

A first approach using X-ray simulation tool Sindbad and a model of human body will enable better calibration and scanning conditions to be established. An experimental gantry, equipped with multi-energy energy detectors, will also be developed with the project partners. This will provide experimental measurements for assessing multi-energy detector potential in relation to the need for rapid, reliable, sensitive detection of externally and internally concealed objects.
Leti in MIRTIC

CEA-Leti’s involvement in the MIRTIC project is targeting a breakthrough in infrared imaging detection, which addresses the major cost drivers of well-established microbolometer technology. The institute has developed three advanced technologies to achieve this:

- silicon-based vacuum packaging;
- new highly sensitive bolometer material;
- low cost infrared optics.

Among these developments, CEA-Leti has created unique vacuum Pixel Level Packaging (PLP). In this exclusive CEA-Leti technology, each bolometer pixel is isolated under vacuum by an infrared transparent thin film of amorphous silicon deposited at wafer level around the pixel (see Figure 2).

PLP offers unparalleled cost reductions since a vacuum is generated directly inside the silicon wafer. Ageing tests at over 90°C (up to 260°C) for several months have also demonstrated that PLP meets perfectly reliability and lifetime requirements. These key results confirmed the relevance of the technology and led to its industrial transfer to our partner ULIS in 2016, immediately followed by ULIS’ launching of a first commercial PLP-based IRFPA product (see Figure 1).

Development of a second generation of PLP technology has started at CEA-Leti. The goal is to improve performance and reduce pixel pitch. Encouraging first results have been obtained with an approximately 40% increase in sensitivity comparing with first generation PLP technology. Further research is ongoing to improve the maturity level of this new process.

MIRTIC at a glance

- **Project Coordinator**
  - ULIS (FR)

- **Partners**
  - FR: CEA-Leti, Schneider Electric
  - GE: Optris
  - GR: ISD

- **Total budget**
  - € 28.4 m.

- **EC Contribution**
  - € 4.1 m.

- **Contract Number**
  - 304653

60 months


**Micro Retina Thermal Infrared**

The MIRTIC project goal is to respond to a market expectation by developing and providing a new type of affordable low resolution infrared sensor. This new line of IR sensors is designed to fill an unmet need in applications seeking to achieve maximum efficiency in the everyday use of energy, for example heating or lighting systems. The market trend is oriented on replacement of single IR sensor element by a small 2D array which enables an “understanding” of the scene in order to be able to give not only temperature indication but also spatial information. This information will improve efficiency of management system in charge of air cooling (HVAC), automatic lighting or security (access control, people counting), health care (IR endoscopy) or queue management. This information will improve efficiency of management system in charge of air cooling (HVAC), automatic lighting or security (access control, people counting), health care (IR endoscopy) or queue management.

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**Publications**


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Laurent Fulbert, laurent.fulbert@cea.fr

**TRL**

The First Thermal Activity Sensor (TAS) designed for smart buildings based on the unique patented Pixel Level Packaging (PLP) technology.
POLIS Pilot Optical line for imaging and sensing

Today the imaging market is dominated by mobile applications and by digital still cameras. However, the dynamics of emerging applications reveals enormous growth in new markets, exhibited both by imaging product penetration in existing domains, like automotive, medical and consumer products (TV, gaming,...) and also by the explosion of brand new applications. Innovation in photonic sensor technologies, particularly those with on-board intelligence, has triggered an array of new products for things like proximity sensing, optical navigation and various human-machine interfaces based on optical systems.

In that respect, POLIS incorporates a unique consortium consisting of large corporations, SMEs, institutes and universities from all over Europe and focuses on the following core objectives:

- to push back the frontiers of the existing Imaging Market by devising new products, exploiting existing or new technologies, improving manufacturing and testing tools;
- to explore new opportunities for sensors and systems development in a wider spectral range (from gamma rays to Infrared), using innovative detection techniques (single photon avalanche diodes), materials and technologies (OLED-on-Silicon);
- to significantly improve the state-of-the-art and performance of existing technologies and work on yield and production cost;
- more specifically to implement at pilot line level specific technological modules to enable new products based on innovative technologies such as back-side-illuminated sensors, single photon avalanche diodes, silicon micro-bolometers, Time-of-Flight, OLED on silicon, through-silicon vias and 3D-stacking.

POLIS at a glance

Project Coordinator
STMicroelectronics (FRA)

Partners
AT: EV Group, Materials Center Leoben
DE: Audi
FR: Aldebaran Robotics, Encapsule, Fogale, CEA-Leti, MicroOled, Ifis, Umicore, STMicroelectronics
GB: Horto John Yon IBH, Polaris Vision Systems, STMicroelectronics, University of Edinburgh
HU: Mediso
NL: Delft University of Technology, Photonis

Total budget
€ 106 m.

EC Contribution
€ 16 m.

Contract Number
621200

48 months

Leti in POLIS

Multiple outstanding outcomes were achieved by CEA-Leti during the POLIS project. These include:

- Demonstration of the feasibility of low cost Infrared Thermal sensors for the consumer market: new ROIC design, new microbolometer technology and new packaging technology.
- Demonstration of a high luminance microdisplay based on novel OLED device architecture. The process were successfully transferred to Microoled for the pilot line. This technology is a key to addressing new fast growing markets in the augmented reality field.
- Ongoing development of Very High Luminance microdisplay technology for the next product generation. This new technology is based on the Direct Color Generation (DCG) process. Results obtained in a first demonstrator are very promising and will permit manufacturing of OLED microdisplays of the highest luminance and efficiency.
- Characterization of a functional SPAD in an advanced technology node for gesture recognition, depth-map camera based on Time-Of-Flight and medical imaging. Moreover, microsensors have been designed for implementation in SPAD technology to improve performance.
- Demonstration of a 3D-stacked imager with high bonding quality based on multiple process developments (e.g. bonding alignment under vacuum). Reliability tests are ongoing for a future pilot line. This work highlights the impact of 3D stacking for a CMOS Image Sensor from optical, thermomechanical and thermal standpoints.

These outcomes bear witness to the powerful research dynamic of this very ambitious project and the excellent collaboration between CEA-Leti and its partners.

Publications

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Agnès Arnaud, agnes.arnaud@cea.fr
VOSTARS
Video Optical See-Through Augmented Reality surgical System

The idea of integrating the surgeon’s perceptive efficiency with the aid of new augmented reality (AR) visualization modalities has become a dominant topic of academic and industrial research in the medical domain since the 90’s. AR technology appeared to represent a significant development in the context of image-guided surgery (IGS).

The quality of the AR experience affects the degree of acceptance among physicians and it depends on how well the virtual content is integrated into the real world spatially, photometrically and temporally. In this regard, wearable systems based on head-mounted displays (HMDs), offer the most ergonomic and easily translatable solution for many surgeries. According to the see-through paradigm, most of the AR HMDs fall into two categories they implement: video see-through (VST) and optical see-through (OST) HMDs. In OST systems, the user’s direct view of the real world is augmented with the projection of virtual information into the user’s line of sight. Differently, in VST systems the virtual content is merged with images captured by two external cameras anchored to the visor. With respect to technological and human-factor issues, both the approaches have their own strengths and shortcomings. In this project, we identified in a hybrid OST/VST HMD, a disruptive solution for improving surgical outcomes.

The application driven device will be developed from existing systems and exploiting the knowhow acquired within the consortium on photonics KET technologies. The resulting device will undergo three clinical trials whose results will be fundamental towards a straight industrial exploitation comprising economic viability analysis. Video-Optical See Through AR surgical System (VOSTARS) will be the first hybrid see-through HMD surgical navigator. Albeit it will be specifically designed for medical procedures, its design is aimed to evolve into a multipurpose AR platform for HMDs.

VOSTARS at a glance

- **Project Coordinator**: Universita di Pisa (IT)
- **Partners**
  - FR: CEA-Leti, Optinvent
  - GB: VREO Innovation
  - IT: Universita di Bologna, Scuola Superiore di Studi Universitari e di Perfezionamento Sant’Anna
- **Total budget**: € 4.4 m.
- **EC Contribution**: € 3.8 m.
- **Contract Number**: 731974

Leti in VOSTARS

CEA-Leti is contributing the Key Enabling Technology (KET) embraced in the VOSTARS proposal. This is the GaN LED micro display for implementation in the HMD device to be demonstrated prior to project completion. CEA-Leti is also demonstrating the performance of this innovative technology compared with standard microdisplay OLED, LCD and LCD technologies.

A family of innovative solid-state light-emitting microdisplays based on III-Nitride Semiconductor micro-size light emitting diodes (µLEDs) will be implemented. These devices have been developed by CEA-Leti. This technological achievement will be obtained by combining innovative technical solutions from GaN epitaxy to silicon-based circuit. This will allow demonstration of µLEDs matrices with luminance of at least 50000cd/m², exceeding by several orders of magnitude the present levels of 1000cd/cm² obtained using state-of-art OLED microdisplays.

Micro-LED performance will make it possible to reduce dramatically the power consumption of the optical integrator, thereby providing a key deliverable to the market place. This CEA-Leti micro-LED display, structured at 10µm pitch on sapphire wafers and hybridized on a silicon backplane, offers the following advantages:

- high brightness at high resolution with almost no limitation on lifetime, providing a significant margin for HMDs;
- low power consumption, lightweight and optical characteristics enabling integration into very compact systems, which conserve, indeed improve, the performance characteristics of the final product.

In comparison with state-of-the-art microdisplays, those used in the eMagin products (AMOLED matrix coupled to a silicon backplane) are capable of producing a luminance of 104cd/m², which is a couple of orders of magnitude lower than the target for the LED-based microdisplay contributed to the VOSTARS project by CEA-Leti.
Medical Devices
The key therapeutic issue in diabetes mellitus type I and II is glycaemic control. Reductions of constant self-control, of insulin injections, and of long-term complications would have tremendous benefit for quality of life. The best therapy option is the transplantation of allogeneic islet cells, but the current state of the art limits the applicability of this approach. Implanting unprotected grafts requires lifelong administration of immunosuppressants, and protecting the cells against adverse immune reactions by current encapsulation strategies reduces their functionality and survival to an extent that makes frequent ‘refresher’ implantations necessary. Currently, a maximum of 2 years glycaemia regulation has been shown for the encapsulated approach.

In BIOCAPAN, bringing experts from different fields all together, we aim at developing an innovative treatment, based on the implantation of allogeneic islet cells that are embedded in a complex microcapsule. We will design a GMP-grade bioactive microcapsule that will maximize the long-term functionality and survival of pancreatic islets by prevention of pericapsular fibrotic overgrowth, in situ oxygenation, innovative extracellular matrix microenvironment reconstruction and immune-system modulation. We will establish a GMP-grade microencapsulation platform to protect freshly harvested islets quickly in a standardized and reproducible way.

We aim for full preclinical validation and we will establish a complete protocol in accordance with the provisions of the Advanced Therapy Medicinal Products Regulation, in order to start clinical trials within one year after the end of the project. We aim for 5-years insulin injection free treatment, without immunosuppressants, which would tremendously benefit diabetes mellitus patients who require insulin (all Type I and about one in six Type II Diabetes Mellitus patients).

In vitro and in vivo validation of different biomaterials has started. Initial promising results require confirmation for more pancreatic islet samples for accurate assessment of the benefits of the developed biomaterials.

If successful, BIOCAPAN would lead to a therapy option that eliminates the need for daily controls and interventions for at least two years. At the same time the natural glycaemic homeostasis, supported by the implanted islets, would reduce the prevalence of comorbidities. A successful biotherapy with microencapsulated islets will fulfill patient expectations in terms of quality of life as well as public health requirements in terms of cost in use due to better glucose control and more efficient insulin level control than any other insulin delivery method.

**BIOCAPAN**

**BIOactive implantable CApsule for PANcreatic islet immunosuppression free therapy**

The strategy chosen to protect pancreatic islets from immune-rejection is to microencapsulate the pancreatic islets in soft, porous, biocompatible microcapsules. During this first period of the project, the research consortium agreed on definition of a reference microcapsule and an a priori bioactive microcapsule, based on a bibliographic study. Different biomaterials have been developed or are still under development. While initial biomaterials have been successfully synthesized to reduce pericapsular fibrosis and to enhance pancreatic islets oxygenation, new syntheses are on-going to improve further biomaterial performance.

The entire process chain has been assessed: every step has been depicted from biomaterial cell production to microencapsulation. Risk analysis is now planned. The process is being gradually optimized to be able to integrate a cell therapy unit by the end of the project. GMP production of candidate biomaterials has already started. A first prototype of a microencapsulation platform has also been designed and is currently under fabrication.

In parallel, the consortium has drawn up the clinical trial specifications and has received scientific advice from regulatory agencies to ensure IMPD completion by the end of the project. The final product requires further characterization but an in vitro and in vivo preclinical test strategy is now being defined.

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**EC Programme**

H2020 NMP-10-2014 - Biomaterials for the treatment of diabetes mellitus

**Keywords**

Bioactive microcapsule
Diabetes
Encapsulation platform
Good Manufacturing Process (GMP)
Nanocharacterization
BitMap

Brain injury and trauma monitoring using advanced photonics

Our vision is to develop a suite of standardised non-invasive devices that will provide essential information about brain health in neurocritical care and neuromonitoring, with a particular emphasis on traumatic brain injury; the “silent epidemic of the third millennium”, and on hypoxia in newborn children. Survivors present permanent neurological conditions that have a profound impact on the quality of life of individuals and their families, and hence a large socio-economic impact. The key factors influencing these conditions and their treatment are the avoidance of brain hypoxia and metabolic disturbances and this is driving the transfer of new neuromonitoring systems to the bedside where they are being shown to have a transformative effect on patient care.

BitMap will develop non-invasive photonics-based monitoring technologies and data analysis methods to provide biomarkers that could guide patient management. A cohort of multi-disciplinary Early Stage Researchers (ESRs), embedded in leading laboratories across Europe, will work together on a programme designed to address the key technological and clinical challenges in neurocritical care. The ESRs will benefit from the diverse range of expertise in advanced photonics and clinical application which will substantially enhance their research competitiveness and employability, and will together form a critical mass of skilled people working together towards new technological and clinical challenges in neurocritical care. The ESRs will work together on a programme designed to address the key technological and clinical challenges in neurocritical care. The ESRs will benefit from the diverse range of expertise in advanced photonics and clinical application which will substantially enhance their research competitiveness and employability, and will together form a critical mass of skilled people working together towards new technological and clinical challenges in neurocritical care.

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BitMap at a glance

**Project Coordinator**
The University of Birmingham (GB)

**Partners**
- DE: Physikalisch Technische Bundesanstalt, PicoQuent GmbH
- FR: CEA-Leti
- GB: University College London, University Hospital Birmingham
- IT: Politecnico di Milano
- PO: Institute of Biocybernetics and Biomedical Engineering
- SP: Fundacio institut de Ciencies Fotoniques (ICFO), HemePhotonics, Vall d’Hebron University Hospital

**Total budget**
€ 3.8 m.

**EC Contribution**
€ 3.8 m.

**Contract Number**
675332

BitMap

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The challenges involved are fundamentally multi-disciplinary and therefore ESRs trained in a multi-disciplinary environment are essential if progress and clinical impact is to be made. There is currently no graduate programme producing researchers with these attributes, but there is a significant market for such PhDs in the rapidly developing area of biomedical optics and in general in medical imaging technology development. The BitMap project therefore addresses both a clinical and economic need.
ENATRANS
Enabling NANoMedicine TRANSlation

ENATRANS’ main objective is to network and support SMEs in translation of nanomedicine in Europe by providing a one-stop-shop service to interact and share information, experience and advice with up-to-date information and interactive tools, but also enabling personal contacts.

ENATRANS will gather and provide information about approval processes, regulatory authorities and agencies, clinical and market data, and specific nanomedicine value chain analysis, relevant SME support projects and organisations. ENATRANS will convert this critical information in dedicated learning programs and tools dedicated to translation of nanomedicine.

ENATRANS aims at implementing the concept of a Translation Advisory Board (TAB) as central element of the European Technology Platform for Nanomedicine (ETPN) White Paper. A TAB will be set-up with senior experienced translation experts to guide R&D teams (in SMEs and research institutes) along the translation process to successfully make it to clinical trials and later to the market. ENATRANS will build bridges to clinical trial centers, investors and large companies.

ENATRANS at a glance

36 months

Project Coordinator
VDVDE Innovation (DE)

Partners
DE: Gesellschaft für Bioanalytik Münster, Technik GmbH, VDVDE Innovation
FR: CEA-Leti, Nanobiotix
IS: Tel Aviv University
IT: Fondazione Don Carlo Gnocchi ONLUS
PT: TecMinho

Total budget
€ 2 m.

EC Contribution
€ 2 m.

Contract Number
646113

Leti in ENATRANS

CEA-Leti’s main contribution to the ENATRANS project embraces:

➤ showcasing SMEs with the most translatable projects to investors and industrial business organizations;
➤ hosting the Nanomed Awards in 2015 and 2017;
➤ preparing ENATRANS / ETPN sessions at international conferences;
➤ disseminating information on the ETPN/ENATRANS Nanomedicine Translation Hub at European scientific conferences;
➤ defining a strategy for Nanomedicine Translation Hub sustainability (as part of ESTHER).

Achievements after one year:

➤ ENATRANS supports and encourages nanomed SMEs in the translation of their products under the umbrella of the Nanomedicine Translation Hub and more specifically its Translation Advisory Board. At the end of 2016, 52 teams from 16 countries in EU and beyond have already applied to the Nanomedicine Translation Advisory Board and half have been selected and are currently benefitting from coaching over time;
➤ ENATRANS and ETPN (European Technology Platform on Nanomedicine) announced the 2 winning projects of the Nanomedicine Award 2015 at the BIO-Europe conference. The goal of the Award is to promote and rewards two excellent innovative nanomedicine-based solutions that could help physicians change the way diseases are treated and diagnosed, bringing significant benefits to patients.

ENATRANS at a glance

36 months

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Partners
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FR: CEA-Leti, Nanobiotix
IS: Tel Aviv University
IT: Fondazione Don Carlo Gnocchi ONLUS
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Total budget
€ 2 m.

EC Contribution
€ 2 m.

Contract Number
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ENATRANS at a glance

36 months

Project Coordinator
VDVDE Innovation (DE)

Partners
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Total budget
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The primary aims of the ENLIGHTENED project evolved significantly during its first half. Main progress has been development of a new mass spectrometry system for detecting and identifying traces of biological species for biomedical applications. The novel aspects of the project activities are three-fold. Firstly, the system architecture transfers efficiently the sample in solution to a vacuum chamber without the need for ionization as in today’s mass spectrometry techniques. Secondly, the detector in the vacuum chamber is a series of nanomechanical resonators, which capture as much of the particle beam as possible through the use of resonators featuring optical transduction. Lastly, there is major progress in work dedicated to understanding the limiting source of noise of the nanoresonator to increase its detection limits.

A significant achievement has been demonstration of the system architecture using samples containing massive biological species; these are typically next to impossible to analyze using conventional mass spectrometers. Optomechanical resonators have been fabricated and successfully tested and they show excellent performance. Finally, CEA-Leti has shown that the detection limit of most nanoresonators in the field is different to the commonly accepted theory by several orders of magnitude. A finding that has attracted much attention as mentioned in this article: [http://www.eetimes.com/document.asp?doc_id=1329165].

ENLIGHTENED at a glance

60 months
Jun. 2014 > May 2019

ENLIGHTENED Nanophotonic Nanomechanical Mass Spectrometry For Biology And Health

Mass Spectrometry has become a routine analytical tool in modern biological research, and in recent years in clinical diagnostics and screening. ENLIGHTENED demonstrates a breakthrough concept based on Photonic Nano-Mechanical Mass Spectrometry, able to perform analysis of bioparticles of high biomedical significance, of ultra-high mass, never so far characterized, with single-molecule sensitivity and unprecedented resolution. The long-term vision beyond the current project is to provide biologists with a tool which will be transformative for fundamental knowledge, and to make possible cheap, handheld devices for personalized medicine.
CEA-Leti is responsible for general infrastructure and trans-national access coordination. EU-NCL offers a solution that goes beyond the state of the art by establishing an integrated infrastructure comprising national centres that join forces to offer a comprehensive portfolio of assays in full coordination. Among the testing facilities included, CEA is responsible for physical and chemical characterization and provides a number of physical and chemical characterization tools such as DLS (Dynamic Light scattering), AFM (Atomic Force Microscope), SEM (Scanning Electron Microscope), TEM (Transmission Electron Microscopy), FFF (Ffled Flow fractionation), EDS (Electron Dispersive X-ray Spectroscopy), ICP-MS (Ion Coupled Plasma Mass Spectroscopy), UV-VIS AS (Ultra Violet and Visible light Absorption Spectroscopy), FTIR (Fourier Transform Infrared Spectroscopy), NME (Nuclear Magnetic Resonance), Pro-inflammatory cytokine detection, Endotoxin, and Microbial and Mycoplasma contamination.

OUTCOMES

- EU leadership.
- Strong attractiveness for Grenoble (France).
- Alignment with US-NCI’s NCL (world reference site for nanocharacterisation of nanomedicines).

Initial campaigns launched in 2016 have led to 9 applications from universities, SMEs and research institutes. Different material types have been submitted: organic nanomaterials (liposomes, dendrimers…), inorganic nanomaterials (GNP, iron carbide…) and various drugs loaded.

EU-NCL at a glance

- Project Coordinator: CEA-Leti (FR)
- Total budget: € 5.6 m.
- EC Contribution: € 5 m.
- Contract Number: 654190
**IDENTIFY**

**Improved Diagnosis By Fast Field-Cycling MRI**

Many diseases are inadequately diagnosed, or not diagnosed early enough by current imaging methods. Fast Field-Cycling (FFC) MRI can measure quantitative information that is invisible to standard MRI. FFC scanners switch magnetic field while scanning the patient, obtaining new diagnostic information.

The main objectives of the project are:

- **understand the mechanisms determining FFC signals in tissues**;
- **create technology to measure and correct for environmental magnetic fields, enabling FFC at ultra-low fields**;
- **investigate contrast agents for FFC, to increase sensitivity and to allow molecular imaging**;
- **improve FFC technology, in order to extend its range of clinical applications**;
- **test FFC-MRI on tissue samples and on patients**.

Achieved by:

- developing the theory of relaxation in tissue at ultra-low fields;
- developing magnetometers and environmental-field correction;
- creating and in vitro testing of new FFC contrast agents;
- improving technology to monitor and stabilize magnetic fields in FFC;
- improving magnet power supply stability;
- investigating better radiofrequency coils and acquisition pulse sequences.

**IDENTIFY at a glance**

- **Project Coordinator**
  University of Aberdeen (GB)
- **Partners**
  DE: Tull
  FI: Ico
  FR: CEA, Orst, Interm
  GB: Uniabdn
  IT: Siste, Unito
  PL: Uwm
- **Total budget**
  € 6.6 m.
  **EC Contribution**
  € 6.6 m.
- **Contract Number**
  668119

**48 months**


**Leti in IDENTIFY**

FFC-MRI requires measurement and elimination of interfering magnetic fields near the MRI system; this involves developing new active magnetic shielding. The aim of CEA-Leti and CNRS work is to compensate the surrounding static and time varying (<500 Hz) near MRI and NMR systems (NMR in Grenoble, and MRI in Aberdeen) and to ensure generation of a relaxation field for ultra-low intensity FFC-NMR/MRI measurements in the 2μT - 1mT range.

This work has been broken down into the following key steps:

- roll out magnetic sensors for measuring magnetic environments;
- develop mathematical models for magnetic interference sources (static and time varying);
- based these models, design coils for compensating DC and AC interfering fields and creating ultra- and very-low fields (2μT to 1mT and <500 Hz interference-free);
- develop and implement the coils in Grenoble (NMR system) and Aberdeen (MRI system);
- implement automatic compensation software in FFC-NMR and FFC-MRI systems.

This project will allow the CEA-Leti to:

- strengthen relations between CEA-Leti partners (INAC / Clinatec) and Grenoble partners (G2ELAB from Grenoble INP, CNRS) and build new partnerships with other scientific organizations in Germany, Poland and Italy;
- develop cutting edge technology in terms of magnetic shielding; this will be reusable in other projects requiring cancellation of magnetic interference;
- pursue multiple scientific publications and patent applications;
- develop CEA-Leti expertise in medical imaging;
- export the technology to industrial applications such as material analysis (concrete, polymers, food analysis);
- develop a new generation of portable NMR systems at ultra-low field allowing previous analysis to be conducted on site.

**IDENTIFY at a glance**

- **New**
  - Many diseases are inadequately diagnosed, or not diagnosed early enough by current imaging methods. Fast Field-Cycling (FFC) MRI, can measure quantitative information that is invisible to standard MRI. FFC scanners switch magnetic field while scanning the patient, obtaining new diagnostic information.
  - The main objectives of the project are:
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- **Identify**
  - 48 months
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**Improved Diagnosis By Fast Field-Cycling MRI**

- 48 months
- **Project Coordinator**
  University of Aberdeen (GB)
- **Partners**
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  IT: Siste, Unito
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  € 6.6 m.
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  - develop a new generation of portable NMR systems at ultra-low field allowing previous analysis to be conducted on site.
CEA-Leti is leveraging its expertise to develop novel 3D packaging of miniaturized medical devices, in support of R&D transfer to the industrial partners (e.g. IPDIA, Philips and Silex).

Special adaptation of the packaging technologies to the medical device is generally necessary to meet the specific needs and requirements of the medical application. Another CEA-Leti contribution is development and characterization of new material interfaces for micro-electrodes to ensure efficient recording and stimulation. In the context of fabricating working demonstrators, CEA-Leti provides materials science expertise in biocompatible coatings and access to miniaturized packaging technologies (3D capacitors and interconnects).

CEA-Leti has manufactured a test vehicle and has defined a method to quantify degradation of packaging thin films in a biological medium. These developments are suited to medical technology demonstrators, which are potentially in contact with human cells. The institute has taken part in the inventory of Chip-in-Tip needs for deep brain stimulation. Cooperating closely with the core team of INFOMED project partners, we have defined the initial architecture and selected appropriate materials and processes to achieve a demonstrator.

CEA-Leti has drawn up a detailed inventory of different options and processes, including deposition of organic PEDOT: electrodeposition, screen printing, spin on, 3D macroporous PEDOT-PSS films obtained by freeze-drying. Finally, CEA-Leti has designed and fabricated a platinum/parylene test structure representing final electrode configuration in terms of size, shape and density.

**Publications**


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**Prototypes**

Prototype of next generation diagnostic probe.
InNaSERSS
Development of Integrated Nanoray based SERS system for Leukemia biomarker detection

The monitoring of patients suffering from acute myeloid leukemia (AML) constitutes a challenge which has yet to be adequately addressed by modern medicine. Following chemotherapy residual malignant cells, undetectable by morphologic examination, may remain in the bone marrow of AML patients. This condition is known as “minimal residual disease” (MRD) and is linked to the high rate of relapse (30%) for AML patients. Several studies have shown that the WT1 gene can serve as a biomarker to predict MRD and determine patient response to treatment. Polymerase Chain Reaction (PCR) is currently the most common method for examining WT1. In MRD patients, however, WT1 expression is extremely low and difficult to detect. The aim of InNaSERSS is to develop a new, ultrasensitive diagnostic test based on Surface Enhanced Raman Spectroscopy for the detection of the WT1 gene. This will be possible through the use of new kind of nanostructured surfaces, like nanoholes arrays, capable of significantly enhancing the spectroscopic signal emanating from the target molecule. The project will also contribute to the development and test of a new generation of high resolution, low price portable Raman spectrometers based on stationary wave integrated Fourier-transform spectroscopy (SWIFTS).

OUTCOMES
The first part of the project focused on optimization of a Surface Enhanced Raman Spectroscopy (SERS) substrate based on the use of nanoholes-gold arrays. This kind of nanostructured material was previously purported to be capable of supporting the presence of localized surface plasmon (LSPR) and to thereby generate hot spots. The work performed during this project has led to development of a particular type of nanostructure, featuring polymeric nanopillars embedded in a gold layer, whose properties are superior to those of “standard nanoholes” in terms of production process stability and reproducibility. These new nanostructures have been used to develop WT1 bio-assays. The detection performance characteristics have been validated using both conventional Raman microscope (LabRam Aramis, Jobin-Yvon) and the compact Raman reader developed at the CEA-Leti. A detection limit for the target sequence of 2 picomolar has been determined when using red laser line of conventional equipment. The compact reader has shown its efficiency in measuring the SERS effect arising from bio-detection assays, but with poorer sensitivity due to the green laser line used.

In parallel, a SWIFTS-based demonstrator has been designed and built and it is now being integrated into the Raman probe. Use of SWIFTS allows building of a cheap, portable Raman spectrometer offering performance characteristics similar to those of existing bench top research systems. Merging these innovative tools to create a new point-of-care diagnostic platform will contribute to the development of more personalized medicine based on a sensitive, specific detection test for disease biomarkers with a realistic prospect of industrial translatibility.

InNaSERSS at a glance

24 months

Project Coordinator
Fondazione Don Carlo Gnocchi ONLUS (IT)

Partners
FR: CEA-Leti, Resolution Spectra Systems
GB: BioSypher

Total budget
€ 0.8 m.
EC Contribution
€ 0.44 m.

Contract Number
635867

Publications
• S. Picciolini et al., ACS Nano. 2014, 8 (10) 10496-506

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The objective of the MFManufacturing project is to bring the manufacturing of microfluidic devices to the same level of maturity and industrialization of electronic devices, enabling them to address more widely in the healthcare needs. Electronic devices, which have been on the market for many years, have benefited from the long going standardization of electronic components, and were therefore easily integrated in the production process of the major foundries.

MFManufacturing

European initiative for the standardization and manufacturability of complex microfluidic devices

The project consortium has reached a consensus on design guidelines to be standardized and has published two whitepapers on the project website [1]. One of the main objectives of these guidelines is to allow reliable, easy connection of a MicroFluidic Building Block (MFBB), which integrates a fluidic function (e.g. a pneumatic valve), to a Fluidic Circuit Board (FCB). These guidelines will enable the microfluidic designer to access a design kit library and off-the-shelf components, thereby saving product development time.

Promoted by these whitepapers, an International Workshop Agreement (IWA) was held in London in April 2016. This open workshop was the chance to present these guidelines to international microfluidic players outside the project and to list 7 resolutions, described in an ISO document [2].

Widespread dissemination is important to gain the acceptance of the microfluidic community. In this connection, CEA-Leti played an active part in several major international conferences and workshops in 2016 [3,4].

To illustrate the impact of the guidelines, CEA-Leti has designed a generic bench to test all the MFBBs developed within the project or described in the whitepapers under specific conditions (cf. figure).

PERSPECTIVES

As an AFNOR member, CEA-Leti has drafted, jointly with MFManufacturing partners, the formal document required for creation of an ISO standard. Standardization will be monitored by ISO technical Committee TC48, leading to a first international microfluidic standard.

The project consortium will continue to implement the standards through the Distributed Pilot Line.
ML² - MultiLayer MicroLab provides a design and manufacturing platform for the production of sophisticated devices which combine microfluidics, optics and microelectronics.

Design and develop a novel and highly cost-effective and versatile production platform based on the concept of roll-to-roll printing for an innovative and integrated Lab-on-Chip systems.

Design and develop a fully functional and integrated Lab-on-Chip microfluidic and detection system that will combine existing market solutions nowadays only present separately enhancing therefore the performance and multi-parametric-sensing capabilities (i.e. electronic, optic, integration of multiple bioactive components, etc.).

Define and execute realistic test case experiments and scenarios that will demonstrate the detection capabilities (pathogen detection, point of case diagnostics, disease diagnostics, etc.) and open the path to full commercialization of the system.

**OUTCOMES**

- Development of a disposable fluidic chamber made of PMMA for detection based on fluorescent target-probe recognition:
  - immobilization process compatible with roll-to-roll process,
  - generic, robust, reliable process for immobilizing amine probes on PMMA,
  - light guide inside PMMA substrate from «probe zone» to sensor,
  - successful transfer to a roll-to-roll machine.
- Validation of immobilization process for substance P detection: < 1 ng/ml in 5 minutes (x2).
- Detection level of 1 μg/mL for ethinyl oestradiol.
- Sensitive detection method: typically 100 times more sensitive than scanner detection (TECAN LS200).
- Light conveyed from PMMA edge to PMT sensor by fiber bundle (rectangular to circular transformation).
- Rapid detection (<10 minutes), automation possible, wavelength adaptable, continuous mode detection (real-time, kinetic, etc.),…
- Small, low cost pumps and electrovalves (roll-to-roll: pick and place).
NanoAthero

Nanomedicine for target-specific imaging and treatment of atherothrombosis

NanoAthero aims to demonstrate the preliminary clinical feasibility of the use of nanosystems for targeted imaging and treatment of advanced atherothrombotic disease in humans.

In acute coronary syndrome and stroke, atherosclerotic plaque disruption with superimposed thrombosis is the leading cause of mortality in the Western world. Nanosystems for both the imaging and the therapy of thrombus and plaque are developed.

I) New nanoimaging agents will allow non-invasive molecular imaging of key pathological processes in vulnerable plaques.

II) Nanosystems will be used for delivery and improved efficacy of drugs for plaque and stroke treatments in humans.

EC Programme
FP7 NMP.2012.1.2-2 - Development and phase-I clinical trials of novel therapeutic nanotechnology-enabled systems for the diagnosis and treatment of atherosclerosis

Key Nanomedicine

Keywords

www.nanoathero.eu

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5 years
Feb. 2013 > Jan. 2018

NanoAthero

at a glance

Project Coordinator
INSERM (FR)

Partners
AT: Medical University of Graz
CH: CLINAM – European Foundation for Clinical Nanomedicine
DE: Max Planck Institute of Colloids and Interfaces, NanoPET Pharma GmbH, Universitätsklinikum Erlangen
DK: Lundbeckfonden Center of Excellence in Nanomedicine NanoCAN FR: CEA-Leti, CEA-DSV, Hopitaux de Paris (FR), Inserm, Inserm-Transfer SA GB: Edinethics Ltd NL: Academic Medical Center, University of Twente

Total budget
€ 12.8 m.
EC Contribution
€ 9.8 m.

Contract Number
309820

Leti in NanoAthero

CEA-Leti is performing the following two principal tasks in the NanoAthero project.

I) Development of new contrast agents for atherosclerotic plaque imaging: these contrast agents have been designed based on the well-established Lipidots™ technology. Lipid nanoparticles have been modified to insert on their surface chelating moieties for Gd³⁺ labeling for Magnetic Resonance Imaging, or 68Ga labelling for Positron Emitting Tomography. Furthermore, the particle surface has been functionalized by ligands targeting the atherosclerotic plaques at different stages of development (fucoidan targeting endothelial cells at initial plaque development stage and RXP470, a peptide targeting MMP12 protein overexpressed in plaque macrophages at more advanced plaque development stages).

II) Screening of drug-loaded lipid nanoparticles for plaque treatment: an anti-inflammatory drug (budesonide) and a LXR agonist for lipid metabolism regulation (GW3965) have been loaded in Lipidots™ for plaque therapy. The particles’ ability to target efficiently the atherosclerotic plaques has been demonstrated in an ApoE mouse model (see figure).

Significant results have been reported at the project mid-term.

I) Relevance of Lipidots™ nanosystems for plaque and thrombus targeting: proof-of-concept for atherosclerotic plaque targeting by Lipidots was demonstrated by in vivo fluorescence imaging in apoe mice model using fluorescent dye-labelled nanoparticles (see figure). Nanoparticle accumulation in atherosclerotic plaques was observed only 2 hours after intravenous injection and increased after 24 hours. These findings pave the way to future clinical studies.

II) New contrast agent for plaque imaging ready to enter preclinical studies: fast and efficient labelling of Lipidots™ by radionucleides such as 68Ga or 64Cu was achieved. These radiolabeled agents designed for Positron Emitting Tomography imaging are presently tested in preclinical model of atherosclerotic plaques (apoE mice) in collaboration with APHP/Bichat Hospital.
NAREB
Nanotherapeutics for Antibiotic Resistant Emerging Bacterial pathogens

The extensive use of antimicrobials in human medicine over the past 70 years has now led to a major threat to clinical practice due to a relentless rise in the number and types of microorganisms resistant to these medicines.

The aim of this project is to fight against Multi-Drug Resistant (MDR) Mycobacterium tuberculosis (M. tuberculosis) (TB) and Methicillin Resistant Staphylococcus aureus (MRSA), leading to serious diseases which usually require intensive care treatment with a long hospitalization. The project proposes nanotechnology solutions to this problem by the design, the preparation and the optimization of several nanofunctions of current antibiotics and novel antibacterial drugs.

The objectives of the NAREB project are:
1/ to select antibacterial molecules and design nanocarriers with strong antibacterial activity,
2/ to test in vitro and in vivo the best therapeutic combinations including innovative genomic and bioimaging approaches,
3/ to assess safety, regulatory and production (GLP/GMP) aspects for the most promising nanofunctions, and
4/ to establishing the Clinical Development Plan for the preparatory work for the subsequent clinical testing of the selected nanofunctions.

CEA-Leti designed smart nanocarriers based on lipid particles with antibacterial activity and contributed to their in vitro validations. Several antibacterials have been tested for being loaded into lipid nanoparticles, including Methicillin Resistant Staphylococcus aureus (MRSA) drugs such as vancomycin, daptomycin or linezolid or Multi-Drug Resistant Mycobacterium tuberculosis (MDR-TB) drugs such as amikacin, bedaquiline or meropenem. Up to now, 3 antibacterials agents have been successfully loaded in lipid nanoparticles by preserving their activity on Multi-Drug Resistant Mycobacterium tuberculosis (bedaquiline and a new lead from GSK) or on Methicillin Resistant Staphylococcus aureus (daptomycin).

These drug-loaded lipid particles present a high colloidal stability even in biological media and CEA-Leti in collaboration with Kuecept has developed injectable IV formulations through freeze-drying processes and resuspension. These new candidates of nanotherapeutics are under investigation in terms of their in vivo efficacy and toxicity at the preclinical level. In parallel, a clinical development plan has been initiated addressing the preparation of a future Phase I clinical testing.

OUTCOMES
The success of the utilization of nanoparticles in the improvement of drug targeting in other diseases opens the way for novel applications in nanotechnology-based antimicrobial treatments aimed at controlling Multi-Drug Resistant Mycobacterium tuberculosis and Methicillin Resistant Staphylococcus aureus.
REFINE
Regulatory Science Framework for Nano(bio)material-based Medical Products and Devices

REFINE proposes a Regulatory Science Framework for the risk-benefit assessment of medical products and medical devices that are based on nanomedicines and biomaterials. The heart of our framework is the development of a product-specific Decision Support System that identifies the most efficient way to deliver the data required by regulation by the best-fitting methods. The decision tree will explicate the product’s specific regulatory challenges and the priorities of both missing data and missing methods to match these challenges. It will thus allow planning a cost-and-time efficient strategy both for necessary measurements and for the advancement of methods. Our approach is aligned with the industrial R&D practice of stage gating. We will demonstrate the relevance of the framework for the most pressing regulatory challenges, which are: borderline products, nanosimilars, and products combining several functionalities. In order to do so, we will identify the regulatory challenges with regulation authorities from Europe and abroad, and design methods for tiered decision tree, guided by the latest scientific knowledge. We will study/predict physiological distribution of nanomedicines and biomaterials, as well as develop and validate new analytical or experimental methods and assays requested by the regulators. These latter development will be performed in a quality management system, ensuring the possible standardisation of our assays. REFINE will gather a wide community of stakeholders in regulation, industry, science, technology development, patients, and endusers, into a Consortium for the Advancement of Regulatory Science in Biomaterials and Nanomedicine.

Leti in REFINE

CEA-Leti’s role in the project:
- global coordination of the project and interface with the European Commission;
- coordination of the “Management and Coordination” part;
- coordination of the “Bridging communities” part.

CEA-Leti’s activities in the project:
- provider of lipid nanoeumulsions as reference materials (Lipidots®) for the validation of new analytical assays, using our scale-up manufacturing platform;
- developer of new analytical assays like Mass Spectrometry Imaging for the analysis of the biodistribution of nanomedicines in human tissues;
- developer of new tools for the preclinical validation of novel nanomedicine and nano-biomaterials, using the Organ-on-Chip technologies under development in our labs, for an animal-free evaluation of new nanomaterials;
- connection of our professional network in nanomedicine industry and in regulation (like the European Medicine Agency EMA and the EU Innovation Network);
- interface between the Nanomedicine and the Nanosafety Communities, in connection with CEA-Liten Institute.

CEA-Leti has been nominated as coordinator of the project due to its successful leadership in EUNCL which is considered now as the reference infrastructure in Europe in Nanomedicine Characterization. CEA-Leti will bring its technical and analytical expertise to the REFINE partners, and expect in return a stronger expertise in the forefront of analytical sciences applied to novel nanomaterials used in medical applications, whether as medicinal forms or as medical devices. This leadership will reinforce our position as a European leading institute in nanomedicine and its regulatory aspects.
Leti in SWAN-iCare

CEA-Leti is performing the following tasks:

- development of a sensor for wound status assessment: impedance measurement is a non-invasive way to characterize the biological structure of living tissues. Wound structure is, by hypothesis, quite different of the healthy skin one. Therefore, it should be possible to monitor the healing status of a wound thanks to impedance measurement;
- development of a sensor for detecting wound infection: the purpose of the bacterial sensor is to screen MRSA in wounds. Screening is performed within a separate closed reaction chamber: an enzymatic substrate generates a volatile compound, if bacteria are present. Then volatile compound is trapped in the sensor and a continuous monitoring of the absorbance of the sensor is performed;
- development of a smart dressing for delivery of healing-promoting drugs: collagen-based biomaterials are designed by loading lipid nanoparticles into collagen gels followed by a freeze-drying process. These materials combine with the water-absorbent, tissue-structuring and reconstruction properties of the collagen as well as with the healing properties of the lipids. The lipid nanoparticles can also be loaded with anti-inflammatory or antibacterial drugs as well as growth factors that encourage healing.

Developments at project completion:

- a wearable device for for impedance measurement (a miniaturized impedance meter). Tests reveal close agreement with measurements taken on the device and on a commercial, non-wearable device;
- optical sensors for non-invasive detection of bacteria in complex matrices such as blood, exudate and food;
- collagen-based biomaterials with better healing properties: hybrid collagen/lipid materials have been designed and demonstrated to promote cell attachment and adhesion, thereby encouraging rapid, safe wound healing.
Metrology

3DIM
3DStack
E450EDL
Holoview
METRO4-3D
NFFA - EUROPE
SEAKET
SOLCELL
ThinErgy
Leti in 3DAM

CEA-Leti’s main contributions to 3DAM are delivery of advanced technology node test wafers to project partners and providing access to its nanocharacterization platform offering a wide range of characterization techniques including:

- a 300mm silicon technology platform supplying test wafers to selected partners, thereby allowing development of in-line methodologies (COSEM, 3D-AFM, OCD):
  - front End Of Line (FEOL): different length and width nanowire arrays, stacked nanowires and nanowires inside dummy gates,
  - back End Of Line (BEOL): TSV with 5 - 20μm top CD and medium to high aspect ratio.
- collaboration with other partners in developing complementary structural characterization techniques such as Electron Tomography in a TEM for FEOL qualification, X-ray tomography in a SEM for BEOL qualification, Cathodoluminescence (CL) and Photoluminescence (PL) techniques for defect characterization and identification, Nanobeam Electron Diffraction in a TEM and micro-RAMAN for strain analysis;
- composition and doping measurements of SiGe and III-V materials using micro-RAMAN spectroscopy, TEM Energy Dispersive X-ray and Electron Energy Loss spectroscopies (EDX &EELS), low-impact-energy SIMS protocols and Atom Probe Tomography;
- development of PL and CL mapping for MX2 materials to extract information on thickness and crystal quality;
- in conjunction with project partners, contribution to development of hybrid, correlative metrology and characterization protocols and workflows. The study aim is to combine two or more complementary metrology or analytical techniques to improve further the overall capabilities of technology development and ramp-up phases;
- organisation of a public workshop in March 2019 at MINATEC Grenoble to disseminate project findings.

3DAM at a glance

- Project Coordinator
  - FEI Electron Optics B. V. (NL)
- Partners
  - BE: Imec
  - CH: ATT
  - DK: CAP, DTU
  - FR: AM-F, CAM, CEA-Leti, FEI-FR, ST
  - HU: SEMIL
  - IE: ADA
  - IL: AMI, BRUKER JV, NOVA
  - NL: FEI, TNO, TU/e
- Total budget
  - € 13.9 m.
- EC Contribution
  - € 6.5 m.
- Contract Number
  - 692527

3DAM
3D Advanced Metrology and materials for advanced devices

The objective of the 3DAM project is to develop a new generation of metrology and characterization tools and methodologies, needed to enable the development and introduction of the next semiconductor technology nodes. To follow Moore’s law for the next decade, breakthrough developments in lithography, device architectures and new materials are needed. As nano-electronics technology is moving beyond the boundaries of (strained) silicon in planar or even FinFETs, new 3D device architectures and new materials (e.g. nanowires, MX2 and 2D materials) bring major metrology and characterization challenges which cannot be met anymore by pushing the present techniques to their limits.

NEW

http://ecsel.eu/web/projects/3DAM.php
Leti in 3D Stack

The JRP addresses the following scientific and technical objectives:

> development of reliable 3D characterization and metrology techniques for:
  > • Cu filled TSV samples and arrays with aspect ratios from 10 to 15 /1,
  > • wafers of different thicknesses and interconnection diameters before bonding and after CMP;
  > • development of methods to accurately measure electrical and thermal transport properties of nanostructured copper TSV interconnects;
  > • development of metrology tools, protocols and standards for high lateral and z resolution;
  > • characterization of post bonding overlay alignment on the available sample using IR microscopy and laser scanning IR. Preparation of a report on metrological assessment of IR microscopy and laser scanning IR limits in relation to post bonding overlay alignment for micron size interconnects;
  > • inspection of the bonded/thinned wafers to characterize defect type (particle, voids, material residue), and defect distribution during the bonding process;
  > • consideration of wafer/die bonding and thinning process aspects. Dimensional characterization of samples and other properties (using confocal measurements, IR scan mode interferometry, confocal chromatic scan mode and spectral domain IR interferometry);
  > • provision of traceable metrology for thickness uniformity control and surface quality of wafers/dies;
  > • based on inputs from other partners, delivery of a documented recommendation on the strategy for measuring dimensional properties of TSVs using confocal microscopy, IR interferometry and optical microscopy traced to metrological 3D atomic force microscopy (AFM);
  > • engagement with the semiconductor industry and others to facilitate technology take-up.

3D Stack at a glance

- **Project Coordinator**
  - Lne (FR)

- **Partners**
  - BE: Imec
  - CH: Metas
  - DE: Fraunhofer Izm, Ptb
  - FR: Fogale, CEA-Leti

- **Total budget**
  - € 1.4 m.

- **EC Contribution**
  - € 1.4 m.

- **Contract Number**
  - Grant Agreement No. 14IND07

18 months


The evolution of the More than Moore approach has introduced 3D objects at the micron scale, the through silicon via (TSV) and 3D heterogeneous integration. 3D characterization, metrology, and inspection with micrometric to nanometric resolution and capabilities of large-field analysis to inspect and measure groups of vias are required as well as controlling wafer/chip thinning and bonding processes. The current state-of-the-art measurement techniques suffer from a lack of traceability, accuracy and quantification. This project will focus on establishing traceability of existing instruments (optical based methods) by developing new standards and reducing uncertainty through new measurement protocols and methodologies. It proposes to develop new instrumentation (Scanning Probe Microscopy, Scanning Acoustic Microscopy and Synchrotron based methods) to characterize the TSVs before and after filling as well as characterization of the bonding and thinning quality of wafers and dies.

The Joint Research Project (JRP) objective is to develop the metrological infrastructure and facilities for calibration standards and measurements of qualified material and cell devices.
Leti in E450EDL

During the E450EDL project, CEA-Leti has actively contributed to the controlled exchange of wafers between different wafer partner facilities. These are required for the KET demonstration line that implements the Flying Wafer concept, specifically through study and support in metallic and molecular contamination characterization and expertise. CEA-Leti has successfully achieved the following in cooperation with project partners ECP, Imsc and Recif among others:

- defining guidelines and specifications for packaging, shipping and re-introducing wafers at partner facilities and in wafer fabrication;
- implementing characterization methods for metallic and molecular contamination (organic and ionic) measurements inside 450mm FOUPs and MACs and on 450mm wafers stored/shipped in carriers. These analysis methods use GCMS, IC and VPD-ICPMS techniques and have been applied to support the project partners;
- assessing metallic and molecular cross-contamination transferred from 450mm containers through wafers during wafer storage;
- supporting ECP for cleaning process qualification of 450mm FOUP and MAC;
- in close collaboration with ECP, defining “Particles, metallic and molecular contamination cleanliness specifications for 450mm wafer carriers”;
- supporting Recif in determining the metallic contamination control performance characteristics of the 450mm sorter;
- evaluating a subcontractor for reclaiming 450mm wafers, whose metallic contamination requirement has not been met;
- participating in the successful application of the inter-fab Flying Wafer® concept through 3-site (Imsc, Recif and CEA-Leti) exchanges of implemented procedures for contamination control.

E450EDL at a glance

- Project Coordinator
  ASML (NL)

- Partners
  AT: LAM Research AG
  BE: ASML-B, Imsc
  CZ: Artemis
  CH: FEI-CZ, IBS, PSI, CEA-Leti, ECP, Imsc, ASML, Demco, FEI-NL, Lexitec, Prodrive, Reden, TNO, TU-Delft, VDL-ETG, Xylab
  IE: Intel
  IL: AMIL, JVS, KIT, Novia
  NL: ASML, Demco, FEI-NL, Lexitec, Prodrive, Reden, TNO, TU-Delft, VDL-ETG, Xylab

- Total budget
  € 189 m.
- EC Contribution
  € 28.4 m.
- Contract Number
  325613

The aim of the E450EDL project is to continue the engagement of the European semiconductor equipment and materials industry in the 450mm transition that started with the ENIAC JU EEM450 initiative and proceeded with subsequent projects funded with public money, amongst others NGC450, SOI450, EEM450PRO. In the frame of E450EDL project the ESM (equipment and materials) solutions for manufacturing shall be developed according to the market needs as defined in the ITRS roadmap and according to the state of the art manufacturing practices. Different technologies are scheduled, which drive the ITRS towards 1X nm nodes, for instance lithography, metrology, thin film deposition, water preparation and handling according the mentioned for 450mm equipment and material standards.

The following topics are covered to support the realization of the KET pilot line:

- integration and wafer processing;
- lithography;
- front end equipment;
- metrology;
- water handling and facilities.

The demo line resulting from this project is considered as an enabling for first critical process module development by combining cleanroom infrastructure with tools remaining at the site of the manufacturers. This distributed demo line allows the adapted protocols (ex. Flying Wafer) and very performance characterization for the equipment and wafers control. CEA-Leti supports the project partners in advanced analysis and characterization methods.

EC Programme
ENIAC call 2012-2

Keywords
Nanoelectronics
Scaling
**Leti in Holoview**

CEA-Leti is developing methods to detect single dopant atoms in semiconductor devices using different TEM-based techniques such as scanning TEM for measuring dopant presence and off-axis electron holography for measuring related electrical potentials.

A new electron biprism has been manufactured using CEA-Leti cleanroom-based techniques. This replaces conventional quartz-based technology and provides a better low cost method of performing electron holography.

The sensitivity and spatial resolution required to detect the fields around single dopant atoms has now been achieved. Provision of perfect specimens and better vacuums are nevertheless required to make this a routine characterization technique.

Enhanced electron holography allows magnetic and piezo-electric fields to be measured with nm-scale resolution and this technology is now being used to improve the performance of new types of microelectronic device.

Deformation mapping techniques have been developed and are now being used to measure strain in technologically relevant devices with nm-scale resolution.

Methods have been designed for switching microelectronic devices in situ within the TEM system so it is now possible to observe changes in working conditions in real time. For example, we can now observe the movement of oxygen vacancies in resistive memories.

Furthermore, specimen preparation techniques have been improved to allow accurate observations of studied materials.

All these methods can be combined to provide measurements of the structure, composition and fields in nano-scaled devices and to observe their changes in-situ as they operate within a TEM system.

---

**Holoview**

**Single dopant atom detection in electrically operated devices**

**Holoview at a glance**

- **Project Coordinator**
  - CEA-Leti (FR)

- **Partners**
  - NA

- **Total budget**
  - € 1.5 m.

- **EC Contribution**
  - € 1.5 m.

- **Contract Number**
  - Stg 306535

**60 months**


As the dimensions of the components that are used in the semiconductor industry are reduced in size, innovation becomes more and more a key parameter. Doped semiconductors are used as components to build nano-electronic devices, light sources, detectors and for photovoltaic applications. As these devices are reduced in size, the location of individual dopant atoms becomes more important and the behavior of only one or two atoms can dominate their properties.

Today there is no method that can routinely measure the presence of the single dopant atoms. Their detection is now within reach, using a transmission electron microscopy based technique known as off-axis electron holography. The phase of the electrons is recovered to allow the electrostatic potentials in the specimen to be measured with atomic resolution. It is the goal of Holoview to electrically connect and operate a range of microelectronic devices in situ in the TEM in order to assess the electrical characteristics whilst observing the changes in electrostatic potential caused by the individual active dopants. The ability to see individual dopant atoms and to observe working devices to single dopant atoms has now been achieved. Provision of perfect specimens and better vacuums are nevertheless required to make this a routine characterization technique.

Enhanced electron holography allows magnetic and piezo-electric fields to be measured with nm-scale resolution and this technology is now being used to improve the performance of new types of microelectronic device.

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All these methods can be combined to provide measurements of the structure, composition and fields in nano-scaled devices and to observe their changes in-situ as they operate within a TEM system.

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**Publications**

- “Strain mapping of semiconductor specimens with nm-scale resolution in a transmission electron microscope”, D. Cooper et al. Micros 50 145-165 (2016).
- “Electronic mapping of semiconductor specimens with nm-scale resolution in a transmission electron microscope”, D. Cooper et al., Micron 50 145-165 (2016).

**Contact**

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Leti in METRO4-3D

CEA-Leti’s main contribution to the METRO4-3D project is evaluating and developing new TOF-SIMS protocols as well as designing and supplying test structures. Two major developments are addressed. Combining AFM with TOF-SIMS. CEA-Leti is taking part in evaluating a combined instrument, installed at IMEC, in which AFM and TOF-SIMS can be performed on the same sample without removing it from the vacuum chamber. The idea behind this is that the surface topography measured by AFM can be used to correct the 3-D TOF-SIMS data set for initial surface topography and the difference in sputter rate of difference materials. The AFM can also be used to give precise depth scale measurements. This in-situ approach is being compared with an approach at Leti, where the sample is transferred between AFM and TOF-SIMS instruments in a transfer capsule (vacuum or inert gas atmosphere). More advanced AFM modes will also be investigated to correlate materials properties such as elastic modulus with chemical information from the TOF-SIMS.

FIB-TOF-SIMS. A second major development entails using a Ga-focused ion beam (FIB) in situ in the TOF-SIMS. Protocols are being developed at Leti to cross-section TSV samples in-situ and image the cut face using the TOF-SIMS. This will be extended to the use of slice and view tomography where successive FIB cuts and images are performed allowing a 3-D volume to be generated. This work will be correlated with METRO4-3D data from Gigahertz acoustic microscopy.

METRO4-3D

Ion-Irradiation-Induced Si Nanodot Self-Assembly for Hybrid SET-CMOS Technology

Within the food chain of equipment delivery for the semiconductor industry, Europe has kept a very strong position in the metrology area with many companies establishing themselves as main leaders in the field. Hence in line with the objectives of the ICT25 call for innovation action to overcome the (initial) barriers for the successful commercialization of novel European products, this project aims at exploring for a number of metrology solutions their technological readiness, reliability and relevance of the developed protocols, and the COO. The portfolio within the project covers new metrology concepts addressing specifically the processing challenges linked to 3D-Devices and range from probing basic layer properties (composition, electrical properties) in FEOL to control of metallization in BEOL, up to issues linked to die stacking. For each of these tools, the basic metrology concepts are existing and validated in the lab on selected applications but their general applicability field within the semiconductor industry still needs to be established.

EC Programme
Horizon 2020 research and innovation programme under grant agreement No 688225

Keywords
3D technologies
Characterisation
Metrology

METRO4-3D at a glance

36 months

New
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By using AFM data acquired at several points during the TOF-SIMS analysis the 3D data set can be corrected for the different sputter rates of the materials present to achieve the data set on the right.

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Keywords
3D technologies
Characterisation
Metrology

EC Programme
Horizon 2020 research and innovation programme under grant agreement No 688225

www.metro4-3D.eu

New

METRO4-3D

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By using AFM data acquired at several points during the TOF-SIMS analysis the 3D data set can be corrected for the different sputter rates of the materials present to achieve the data set on the right.

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Leti in NFFA - EUROPE

CEA-Leti’s contribution is to develop advanced nano-object transfer and positioning. Two major developments are expected in this project: to address integration and large-scale-facilities of laboratory to allow structural, chemical, magnetic or electronic analysis:

- in identical nanoscale sample areas;
- by several complementary fine analysis and large scale facility techniques;
- in various applications and industry relevant environments.

The purpose is to enable users from a broad range of scientific fields to conduct novel nanoscience based on one to one structure-property-relationship of single nano-objects or nano-assemblies. It involves establishing a standardized protocol and the corresponding platform to provide novel capabilities for the user, who wants to analyze the same nano-object with different equipment at different research facilities.

Participation in this first development provides CEA-Leti with the necessary hardware for analyzing a nano-object at the same nano-location within different equipment: DB-FIB, P-FIB, SEM, CL, AFM, …, It is also a good opportunity for strengthening links with different research institutes throughout Europe. The second contribution part is by performing infrastructure nano-characterization in conjunction with 11 partners (CNR, CNRS, PSI, PRUB-ICMAB, ICN2, JULICH, TUG, DESY, FORTH, LU). This infrastructure ensures integrated access to advanced characterization of nanosystems as grown and/or nano-fabricated at other NFFA-EUROPE facilities and ensures collection of experimental data for simulation or interpretation with respect to the theoretical installation. Each installation includes a unique combination of laboratory based methods including atomic resolution imaging, electron transport measurement, optical magnetometry or XPS, synchrotron X-ray or neutron beamlines for scattering and spectroscopy, table-top or perspective ultrashort pulses and FEL beamlines.

Within the framework of this transnational access, CEA-Leti provides access to TEM, SEM, DB-FIB, P-FIB, Nano-AES, CL, PL, AFM, APT, XCT, XR/D/XRF, Raman, ToF-SIMS, XPS, PEEM.

This allows CEA-Leti to enhance the visibility of the PFNC, establish new relations with other nanocharacterization centers (in particular with other large scale facility) and consolidate existing relations.

Atom-Probe Analysis (APT) of a material.
SEA4KET
Semiconductor Equipment Assessment For Key Enabling Technologies

SEA4KET (Semiconductor Equipment Assessment for Key Enabling Technologies) is an IP proposal taking the consequent step from equipment R&D to equipment assessment experiments. The strategic objective is to effectively combine resources and expertise in a joint assessment of novel equipment for key enabling technologies to foster and accelerate the successful transfer of novel European equipment into the world-wide market.

SEA4KET builds on the proven principle established in previous European SEA programs and projects: to take novel, innovative and promising equipment that has left the R&D phase into a joint assessment activity – this bridges the well-known gap between the phase of having an engineered tool available and finding the “first user” and finally success in the market for it.

While proven principles from previous SEA activities are kept, SEA4KET takes them to the new field of assessing equipment for Key Enabling Technologies. SEA4KET concentrates on process and metrology systems for important enablers of future technologies: 450 mm wafer equipment, SiC materials and 3D processing. The proposal comprises 14 sub-projects each dedicated to specific equipment. The assessment activities were to a lesser extent chosen by “high S&T excellence,” but by their expected chance on the market.

While leading R&D institutes are active in each assessment experiment to support individual final developments, several cross-cut R&D activities leading to support on other subprojects; these include contamination issues with new substrates and materials, and metrology and specification development for implementation of the flying wafer concept in the wafer exchanges subproject.

Through assessment and evaluation of different tools, SEA4KET has enabled CEA-Leti to build stronger relationships with Fraunhofer and other partners within the European industrial network (process and characterization) in view of future cooperation. Overall, the program has allowed CEA-Leti to increase its tool pool with:

- New metrology and material handling tools.
- New inspection-on-chip resources.
- New XRD measurement resources for KET applications.

CEA-Leti’s major contribution to this program is evaluating innovative adaptation of semiconductor standard equipment to Key Enabling Technologies and its improvement.

3D integration, in particular, is considered a key technology for increasing the functionality of devices based on nanotechnologies, photonics and nanoelectronics.

In this context, CEA-Leti is taking part in the following three metrology and process tool-related to the project involving innovation, adaptation and improvement dedicated to 3D technology:

- < CovBond: this subproject focuses on evaluation of innovative add-ons to EVG tool for bonding. Innovative surface treatment chambers for direct covariant bonding have therefore been evaluated and their performance characteristics have been assessed;
- < 3DPICS: this subproject involves adaptation of an AMAT tool for inspecting dies on holders (and wafers) for defectivity in photonic die bonding for CMOS applications. This is currently one of the only available tools for performing this inspection, which is crucial to photonics applications;
- < XMeck: this subproject led in conjunction with Bruker XRR-XRD tool innovative improvement to allow difficult measurements on KET advanced materials for Enabling Technologies. CEA-Leti is also contributing to the overall project through its cross-disciplinary activities leading to support on other subprojects; these include contamination issues with new substrates and materials, and metrology and specification development for implementation of the flying wafer concept in the wafer exchanges subproject.

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Leti in SEA4KET

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- New inspection-on-chip resources.
- New XRD measurement resources for KET applications.

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SOLCELL

Metrology for III-V Materials Based High Efficiency Multi-Junction Solar Cells

Multi-junction solar cells (MJSC) based on III-V materials are part of the third generation of photovoltaic cells. They are designed so that each p-n junction absorbs a separate portion of the solar energy spectrum, allowing for solar energy conversion with efficiencies as high as 44%. In the last two decades concentrated photovoltaics (CPV) based on MJSC has rapidly advanced from a proven space technology to become a feasible clean energy technology.

The Joint Research Project (JRP) objective is to develop the metrological infrastructure and facilities for calibration standards and measurements of qualified material and cell devices.

36 months

SOLCELL at a glance

Project Coordinator
LNE (FR)

Partners
CH: METAS
DE: Agilent, Azur Space, Fraunhofer ISE, PTB
ES: Inta-Spasolab
FI: MIKES
GB: Imperial College, NPL
FR: LAAS, CEA-Leti
PL: MIG
TR: Tubitak

Total budget
€ 3.6 m.
EC Contribution
€ 1.6 m.

Contract Number
Grant Agreement No. 217257

CEA-Leti’s role in SOLCELL project is to furnish expertise in characterizing the structural, optical and electrical properties of III-V alloys. Knowledge gained on single layers and simple structures is therefore used to characterize and better understand the properties of III-V multi-junction cells with increasing number of junctions. CEA-Leti takes full advantage of its nanocharacterization platform to provide a comprehensive set of characterizations, which have enabled:

- obtention of optical constant for various III-V alloys using spectroscopic ellipsometry over a wide spectral range and as a function of temperature;
- extraction of layer composition, elemental depth profiles, interfacial specialiation and metal contamination tracking by SIMS profiling;
- mapping of structural defects using photoluminescence and cathodoluminescence;
- measurement of band gap and doping efficiency, and study of electronic properties using ellipsometry and luminescence;
- checking of morphology and layer composition.

By combining characterization techniques, different types of single and dual multi-junction solar cells have now been successfully characterized. The materials involved are binary, ternary and quaternary alloys: GaAs, GaInP, AlGaAs, AlInP, AlGaInP, InGaAs, GaAsSb, GaInAsN and InAs. Results obtained will extend knowledge of these materials and encourage better optimization of complex solar cells for developing the next generation of MJSCs.

Publications

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LETI

Leti in SOLCELL

SOLCELL at a glance

- Project Coordinator: LNE (FR)
- Partners:
  - CH: METAS
  - DE: Agilent, Azur Space, Fraunhofer ISE, PTB
  - ES: Inta-Spasolab
  - FI: MIKES
  - GB: Imperial College, NPL
  - FR: LAAS, CEA-Leti
  - PL: MIG
  - TR: Tubitak
- Total budget: € 3.6 m.
- EC Contribution: € 1.6 m.
- Contract Number: Grant Agreement No. 217257

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Publications

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TRL
ThinErgy

Traceable Characterization of Thin-film Materials for Energy Applications

This project aims to solve those challenges and develop the necessary metrology framework to ensure an energy efficient Europe and to extend Europe’s leadership in energy technology and innovation. The goal of the project is to develop complementary metrology tools for thin film characterisation, including:

- development of models for the interpretation of advanced materials measurements and their correlation to product performance;
- traceable determination of the correlation between material composition and electronic structure over a broad spectral range. This should include the production of reference standards, calibration samples and reference measurement techniques;
- validation of measurement techniques for elemental depth, selectivity and sensitivity for thin film energy materials such as novel compound materials with matrix elemental depth gradients, organic/inorganic hybrids, multi-layered structures and nano-structured surfaces, layers and interfaces;
- development of validated methods for the thermal characterisation of thin films as a function of temperature and for multi-parameter characterisation of energy thin film materials under specific stress conditions;
- development of large-area characterisation methods for process optimisation in thin-film energy material production, including fast contact and non-contact methods.

ThinErgy at a glance

- Project Coordinator: Npl (GB)
- Partners:
  - CZ: Cmi
  - DE: Darm, Hbr, Pbth
  - DK: Ditte
  - FI: Aalto, Mikes
  - FR: CEA-Leti, Lne, Lne-Lnb
  - NL: Npl
  - NL: Vsl
- Total budget: € 3.6 m.
- EC Contribution: € 3.6 m.
- Contract Number: JRP-ENG53

CEA-Leti is contributing to the ThinErgy project within different perspectives that will further its existing expertise through:

- development of accurate non-destructive strategies to probe elemental depth-profiles in InDium-free transparent conductive oxide thin layers (Ga-doped ZnO). These strategies are based on combining Grazing Incidence X-ray Fluorescence (GIXRF) and X-Ray reflectometry (XRR) which is emerging as a fabrication compatible solution for measuring thickness, density and elemental profile in complex thin layered stacks. GIXRF samples are difficult to investigate using XRR-only analysis since in-depth variability of gallium content would have a limited impact on the electronic density, whereas the impact on the atomic density (probed by GIXRF) is significant;
- correlation of optical properties (far ultraviolet to far infrared spectral range), structural and electrical properties of InDium-free transparent conductive oxide thin layers (Al-doped and) grown by atomic layer and physical vapor deposition. This has been investigated using transmission measurements, wide spectral range ellipsometry, Fourier transform infrared spectroscopy in attenuated total reflection mode, photoluminescence, X-ray techniques (fluorescence, reflectometry, diffraction) and Hall effect as a function of temperature. The influence of thermal budget on the properties of ZnO/Al thin materials is also being studied;
- investigation of substrate-induced strain in thin high-k layers grown on AlGaN and GaN substrates for power electronics. Near Edge X-Ray Absorption Fine Structure spectroscopy (NEXAFS) have been used to probe the Al-K edge. Results suggest that ultrathin alumina layers (< 2 nm) grown by atomic layer deposition on GaN substrate are subjected to strain, whereas no substrate-induced strain is revealed in similar layers grown on AlGaN films.

Publications
- Emmanuel Nolot, emmanuel.nolot@cea.fr
Lithography
Directed Self Assembly (DSA)

Block CoPolymer (BCP)

EC Programme
FP7 ICT-2013.3.1 - Nanoelectronics

Keywords
Block CoPolymer (BCP)
Directed Self Assembly (DSA)
Lithography

Directed self-assembly (DSA) of block copolymers is one of the most promising techniques to enable the continued miniaturization of ICs and to boost the performance in More Moore. It combines top-down photolithography for creation of guiding patterns with engineered new materials and processes to facilitate cost effective bottom-up techniques for pattern density multiplication and defect rectification. An industry scale application of DSA still faces two challenges: i) The host substrate heavily impacts DSA. The resulting pattern formation must be well understood and modeled in order to optimize its efficiency and avoid defects. ii) The specific properties of DSA must be considered early in the design process.

CoLiSA.MMP develop new material and process models and a computational lithography framework for DSA. Existing and new, specially designed atomistic and coarse-grained models are combined with experimental data to develop and calibrate efficient predictive reduced models, seamlessly integrated in lithographic process simulation. A new modeling capability is used to establish new design flows which include the lithographic generation of guiding patterns and the resulting patterns after DSA. Inversion of the problem is predicting lithographic manufacturable guiding patterns and process conditions for given target structures. The extended capabilities of computational lithography are also used to improve materials and processes which are still under development, to study the root causes of DSA specific defects and to propose strategies to avoid or reduce them.

CoLiSA.MMP combines European expertise in soft matter physics, block copolymer chemistry, lithographic process and computational lithography. This helps to bridge the gap between the multifaceted research activities on DSA and the integration of DSA in future processes and design flows for More Moore IC manufacturing and for new functionality in More than Moore.

Contact hole shrink by directed self-assembly contact patterning performances
A. Bhardwaj et al., MEMS-MOEMS 15(3), 031604, 2016.
“Contact hole shrink by directed self-assembly of block copolymers from material to integration”
R. Tiron et al., EMRS Spring Meeting, Lille, 2015.
“Graphoepitaxy DSA Process: Versatility: Template Affinity Role”
M. Argoud et al., ICPST conference, Tokyo, 2016.

Publications

CoLiSA.MMP at a glance

Project Coordinator
Fraunhofer IIsb (DE)

Partners
DE: Fraunhofer IIsb, Ulpce
FR: Arkema, Cnrs Lcpo, CEA-Leti, Ntua

Total budget
€ 4.9 m.

EC Contribution
€ 3.5 m.

Contract Number
FP7-ICT-2013-11

36 months

CoLiSA.MMP
Computational Lithography for Directed Self-Assembly: Materials, Models and Processes

CEA-Leti’s contribution is intended to implement DSA processes for graphoepitaxy firstly on PS-b-PMMA and secondly on high-chi materials.

Graphoepitaxy guiding structures have been defined by conventional optical 193nm lithography or e-beam lithography.

The process involves integration of the guiding structure into the resist followed by etching transfer into the CMOS stack. Application of the brush layer and block copolymer coating and finally the DSA process then follow.

The initial evaluation stage has been performed using small silicon samples on a standalone system to ensure rapid screening of material performance.

Best polymer and solvent candidates have been identified and studied in depth on a 300mm pre-pattern substrate.

Graphoepitaxy processes have been finally have been finally developed for line multiplication (lamellar morphology block copolymer) and contact hole shrink applications (cylindrical morphology block copolymer).

Optimal process parameters (time, solvent type, temperature, thickness…) have been determined and lithographic performance characteristics (resolution, pitch, CD uniformity, placement, defectivity, etc.) have been measured for contact hole shrink and line multiplication.

Process implementation output parameters have been used for model and software calibration and validation (resolution, pitch, defectivity, placement,…).

Finally, partner-developed software has been applied to guiding structure design and optimization, and to defectivity formation.

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Publications

“Process highlights to enhance directed self-assembly contact patterning performances”, A. Bhardwaj et al., MEMS-MOEMS 15(3), 031604, 2016.
“Graphoepitaxy DSA Process: Versatility: Template Affinity Role”
M. Argoud et al., ICPST conference, Tokyo, 2016.

Contact hole shrink by directed self-assembly contact patterning performances
A. Bhardwaj et al., MEMS- MOEMS 15(3), 031604, 2016.
“Contact hole shrink by directed self-assembly of block copolymers from material to integration”
R. Tiron et al., EMRS Spring Meeting, Lille, 2015.
“Graphoepitaxy DSA Process: Versatility: Template Affinity Role”
M. Argoud et al., ICPST conference, Tokyo, 2016.

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“Graphoepitaxy DSA Process: Versatility: Template Affinity Role”
M. Argoud et al., ICPST conference, Tokyo, 2016.
Leti in CONNECT

CEA-Leti is contributing to different aspects of the CONNECT project. We offer many different features spanning a few nanometers in length and depth by applying an advanced ebeam lithography technique followed by specific dry etching know-how. Subsequently, we deposit multiple materials (including SiO2, HfO2, Al2O3, Si3N4, etc.) of different thickness to identify the best layer for optimized Carbon Nanotube growth within the minute design features. After preparing the Carbon Nanotube “forest” for metatllization, we conduct electro-chemical deposition-based experiments for evaluating different metal sources and deploy CEA-Leti’s specific know-how in catalyzing advanced chemical reactions of this type. Materials are then screened for ranking at electrical test level after final process integration.

CONNECT’s principal benefit is its evaluation of combined specific carbon nanotubes and adaptive metatllization for advanced interconnexion. It contributes to the prospect of so far unreached current density for future intrachip connexion. Metal line characteristics are investigated in depth to assess this non-conventional approach in relation to future microelectronics.

CONNECT at a glance

Project Coordinator
Fraunhofer (DE)

Partners
CH: IBM
FR: CEA-Leti, CNRS
GB: Aixtron, Gold standard simulations, University of Glasgow

Total budget
€ 4 m.
EC Contribution
€ 3.4 m.

Contract Number
686612
IONS4SET

Directed Self Assembly (DSA)

http://www.ions4set.eu/

Finally, a power saving hybrid SET/CMOS device with a vertical gate-all-around narrow nanowires is crucial for IONS4SET. Through a few tens of nm thin Si pillars with an embedded SiO₂ layer of ~6nm thickness, the fabrication process of the Si nanodot involves (i) ion irradiation of each nanodot with source and drain at tunneling distances of ~2…3 nm required for RT operation. CEA-Lei has recently achieved production of the first nanopillars smaller than 50nm (down to 30nm) by e-beam lithography (EBDW). This is still too thick for single Si quantum dot self-assembly. The work is still in progress in order to obtain pillars of the required dimensions (CD and height). The first goal is to increase the resolution capacity of the Gaussian or shaped beam exposure tool for the 10nm structure using of negative resist. The second is to produce as quickly as possible the first pillar structure fabrication for project partner requirements to allow in-depth investigation of Si dot formation into tiny pillars to start and development of the ensuing process steps required for hybrid SETFET device fabrication.

Another approach to nanopillar fabrication is Directed Self-Assembly (DSA) of block copolymer and this is also investigated within the scope of the IONS4SET project. This also investigated in the frame of IONS4SET project. DSA emerges as a promising patterning technique that could be used to demonstrate dense pillars and extend the resolution limit of conventional lithography (down to 10nm). It is a smart and simple way to structure 10nm pillars on a large array structure for SET operation. Furthermore, DSA is considered as a potential manufacturing patterning technique rather than E-beam approach due to its throughput and cost-effectiveness. During the first months of the project, the work has focused on investigating materials and associated process options to pattern the surface. Different DSA approaches have been identified and initial production of 30nm pillars has been demonstrated. The IONS4SET work includes the lithography and associated etching process steps. Manufacturability is the roadblock for large-scale use of CMOS-based hybrid SET-CMOS architectures. To assure room temperature (RT) operation of hybrid SET-CMOS technologies, SETFET device fabrication.

IONS4SET is aimed at developing reliable technology to generate ion-induced self-assembled single Si nanodots in nanopillars (<20nm) and using these structures for CMOS-based hybrid SET/FET devices operating at room temperature. CEA-Lei is leading a project task that involves producing a nanopillar array on an embedded thin oxide layer. The work includes the lithography and associated etching process steps. Fabrication of Si nanopillars with an embedded SiO₂ layer of ~6nm thickness is the prerequisite of a successful development of a hybrid SETCMOS technology for extremely low-power electronics. The pillar diameter must be of the order of 10nm to fulfill the criteria for self-assembly of a single quantum dot (volumeSiO₂<10nm³). CEA-Lei has recently achieved production of the first nanopillars smaller than 50nm (down to 30nm) by e-beam lithography (EBDW). This is still too thick for single Si quantum dot self-assembly. The work is still in progress in order to obtain pillars of the required dimensions (CD and height). The first goal is to increase the resolution capacity of the Gaussian or shaped beam exposure tool for the 10nm structure using of negative resist. The second is to produce as quickly as possible the first pillar structure for project partner requirements to allow in-depth investigation of Si dot formation into tiny pillars to start and development of the ensuing process steps required for hybrid SETFET device fabrication.

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PLACYD

Pilot Line For Self Assembly Copolymers Delivery

PLACYD aims at developing and industrializing a series of nanostructured materials, devoted to sub 20 nm lithography, together with the required ecosystem (including metrology, design tools, integration processes) that will secure its adoption into manufacturing. It is focused on developing a program that links the production of the polymer materials used for directed self-assembly and lithographic pattern development with wafer level fabrication to originate a robust process that can be used in commercial manufacturing. For the first time it integrates polymer material development into critical development such as pattern defectivity, metrology, circuit design and performance so that a fully developed large scale manufacturing process consistent with ITRS targets is evolved.

36 months

PLACYD at a glance

Project Coordinator
Arkema (FR)

Partners
ES: CNM-CSIC
FR: CNRS/LEP, CNRS/LTM, CEA-Leti, Mentor Graphics, STMicroelectronics
IE: Intel, Tyndall National Institute
NL: ASML

Total budget
€ 14.8 m.
EC Contribution
€ 2.2 m.

Contract Number
ENIAC-ED-126-13

PLACYD

Implementation of Directed Self-Assembly (DSA) materials and processes in a 300mm CMOS wafer scale, clean room environment.

Setting up Statistical process Control (SPC) for lithographic process parameters.

Statistical quantification and monitoring of the impact of material physical characteristics on patterning performances.

Possession of an industrial, reproducible source of material (including both production and characterization methods and metrology) for Polystyrene (PS)-b-Polymethylmethacrylate (PMMA) systems as well as high chi materials likely to be used for the following node.

Selection of materials and lithographic processes for implementation of DSA in CMOS technology.

Development of new DSA-dedicated industrial in-line metrology (dimensional and placement) and inspection (defectivity) tools compatible with sub-10nm critical dimensions.

Understanding, quantification and modeling of material intrinsic properties and material impact on application performance through statistical data.

 Provision of an efficient design tool enabling transparent integration of technology with limited impact on design rules.

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TRL

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