Laboratoire d'électronique
et de technologie
de l'information

UTSOI Model 1.1.3

Surface Potential Model for Ultra Thin Fully Depleted SOI MOSFET

Model Description

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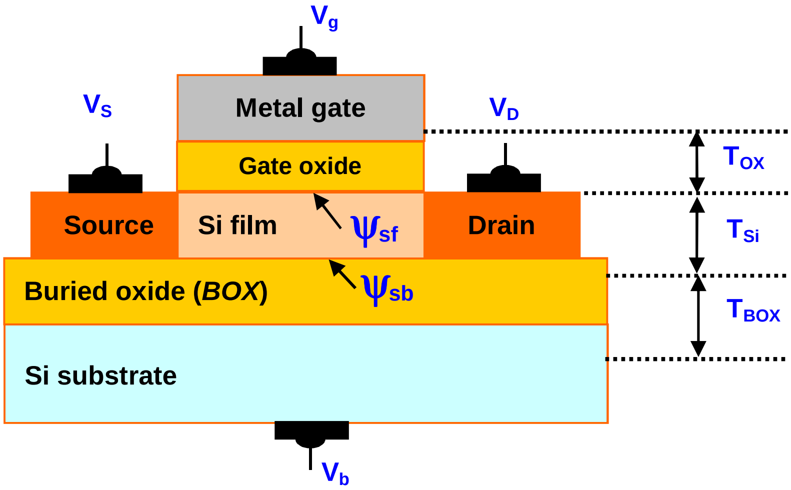
This model is based on the works of the PSP-model developers (PSP model reference: version 102.3)

Contents

1. Device physics and model description

1.1. Device description

The present model was developed by the CEA-LETI for ultra-thin fully depleted SOI MOSFET. The device structure is illustrated by the following figure:



UTSOI model was designed for transistors with a lightly doped silicon film. The silicon film thickness is typically lower than 10nm.
This model is compatible with the use of thin buried oxide (typically 10nm). However, this one is not designed for double gate transistor where the back Si-SiO2 interface can be in inversion.

1.2. Physical background

From the previous schematic, V_g, V_d, V_s, V_b, Ψ_{sf}, Ψ_{sb} are the gate, drain, source, bulk, front surface and back surface potentials, respectively. T_{OX}, T_{Si} and T_{BOX} are gate oxide, silicon film and buried oxide thicknesses, respectively.
In the undoped silicon film region for long channel transistor, the potential is given by the 1-D Poisson's equation:

$$\varepsilon_{si}\frac{d^2\psi}{dy^2} = q \cdot n_i \cdot \exp\left(\frac{\psi - V_c}{u_t}\right) \qquad (1.1)$$

ε_{si} is the silicon permittivity. Ψ, the potential in the film under the gate. q, the electron charge. n_i, the intrinsic doping. V_c, the channel voltage. u_t the thermal voltage given by:

$$u_t = \frac{k \cdot T}{q} \qquad (1.2)$$

Where, k is Boltzmann's constant and T is the temperature.

The first integration of the equation (1.1) between both Si-oxide interfaces gives:

$$E_{sf}^{\,2} - E_{sb}^{\,2} = \frac{2 \cdot q \cdot n_i \cdot u_t}{\varepsilon_{si}} \cdot \left(\exp\left(\frac{\psi_{sf} - V_c}{u_t} \right) - \exp\left(\frac{\psi_{sb} - V_c}{u_t} \right) \right) \quad (1.3)$$

E_{sf} and E_{sb} are the surface electric fields.

Using boundary conditions:

$$E_{sf} = -\frac{C_{ox}}{\varepsilon_{si}} \cdot \left(V_g - V_{FB} - \psi_{sf} \right) \quad (1.4.a)$$

$$E_{sb} = -\frac{C_{box}}{\varepsilon_{si}} \cdot \left(V_b - V_{FBb} - \psi_{sb} \right) \quad (1.4.b)$$

Where $C_{ox}=\varepsilon_{ox}/T_{ox}$ and $C_{box}=\varepsilon_{ox}/T_{box}$. V_{FB} and V_{FBb} are flatband voltages of the metal gate and Si substrate, respectively.

Including the Equations (1.4) in the Equation (1.3):

$$\left(V_g - V_{FB} - \psi_{sf} \right)^2 - \frac{C_{box}^{\,2}}{C_{ox}^{\,2}} \cdot \left(V_b - V_{FBb} - \psi_{sb} \right)^2 = \gamma^2 \cdot u_t \cdot \left(\exp\left(\frac{\psi_{sf} - V_c}{u_t} \right) - \exp\left(\frac{\psi_{sb} - V_c}{u_t} \right) \right) \quad (1.5)$$

With:

$$\gamma = \frac{\sqrt{2 \cdot q \cdot \varepsilon_{si} \cdot n_i}}{C_{ox}} \quad (1.6)$$

The back interface is considered in depletion in all regimes. Then, the double gate mode (where the back interface is in inversion) is not modeled. In this case, the back surface potential is considered as:

$$\psi_{sb} = \alpha_c \cdot \psi_{sf} + \varepsilon \quad (1.7)$$

With,

$$\alpha_c = \frac{C_{si}}{C_{si} + C_{box}} \quad (1.8)$$

$$\varepsilon = \frac{C_{box}}{C_{si} + C_{box}} \cdot V_b \quad (1.9]$$

Where $C_{si}=\varepsilon_{si}/T_{si}$.

Using the same formalism as in [1],

$$x = \frac{\psi_{sf}}{u_t} \quad (1.10)$$

$$x_{gf} = \frac{V_g - V_{FB}}{u_t} \quad (1.11)$$

$$x_{gb} = \frac{V_b - V_{FBb}}{u_t} \quad (1.12)$$

$$x_n = \frac{V_c}{u_t} \quad (1.13)$$

$$\varepsilon' = \frac{C_{box}}{C_{si} + C_{box}} \cdot x_{gb} \quad (1.14)$$

$$G = \frac{\gamma}{\sqrt{u_t}} \qquad (1.15)$$

The Equation (1.5) becomes:

$$\left(x_{gf} - x\right)^2 - \frac{C_{box}{}^2}{C_{ox}{}^2} \cdot \left(x_{gb} - \alpha_c \cdot x - \varepsilon'\right)^2 = G^2 \cdot \left(\exp\left(x - x_n\right) - \exp\left(\alpha_c \cdot x + \varepsilon' - x_n\right)\right) \qquad (1.16)$$

This surface potential equation is analytically resolved using the similar mathematical approximation as in [1].

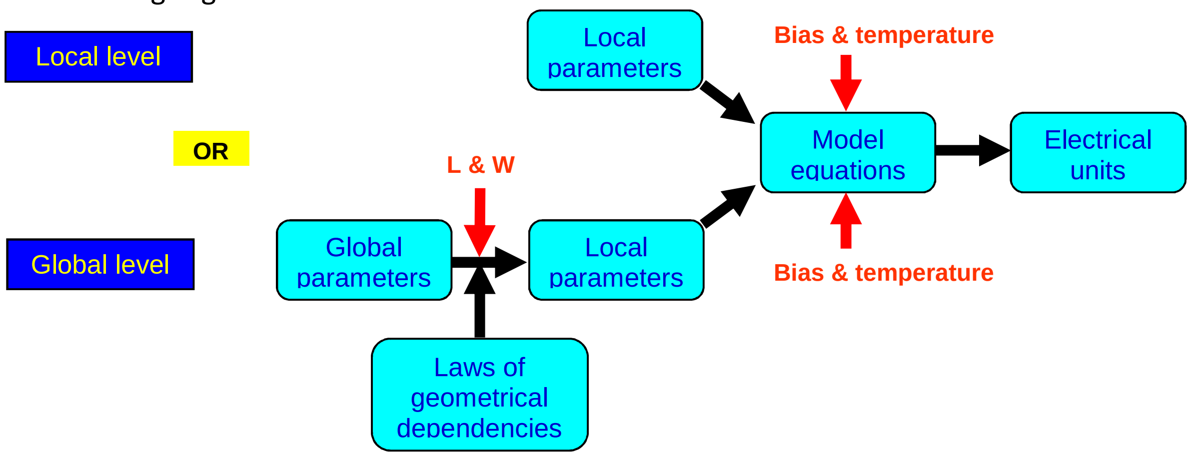
The drain current expression is obtained by a similar analytical resolution of the transport equation as in PSP model [2]:

$$i_d = -W \cdot C_{ox} \cdot \mu \cdot u_t \cdot \left(\int_{x_{n,s}}^{x_{n,d}} q_i \cdot dx_n - \int_{q_{is}}^{q_{id}} dq_i \right) \qquad (1.17)$$

Where, q_i is the inversion charge, μ is the carrier mobility, W is the channel width. $x_{n,d}$ and $x_{n,s}$ are the quasi Fermi level at the drain and source sides respectively. q_{id} and q_{is} are the inversion charges at the drain and source sides, respectively.

1.3. Local and global levels

As in PSP model, the UTSOI model offers 2 sets of parameters: local and global parameter sets. The model structure in regards to the management of the global parameters is given the following organization chart.



1.3.1. Local level

This level ensures, thanks to local parameters, the description of a single transistor with a defined geometry as the length L and the width W. Note that knowledge of these last values of these quantities is not necessary in this mode. The list of local parameters is provided in section 2.

1.3.2. Global level

This level allows describing the electrical behaviors of all transistor geometries with a single parameter set (global parameters) including in a unique model card. The list of global parameters is provided in section 2. The global parameters, combined with the laws of geometrical dependencies, provide local parameter sets, each set being on a given geometry. For this level, the knowledge of L and W is required.
In regards to the geometrical dependencies, the local parameters of the UTSOI model can be divided into four categories:

- Constant parameters (without geometrical dependencies). For example: the process parameters, oxide thickness, substrate doping, etc.
- Parameters with L dependencies only. For example: AX, the smoothing parameter between the linear and saturation regimes.
- Parameters with W dependencies only. For example: the access resistances.
- Parameters with L and W dependencies. For example: the gate to channel tunneling current.

The laws of geometrical variations can be grouped into:

- Laws having a physical significance: they are derived from the laws of physics.
- Hybrid laws: only a part of the law has a physical significance. For example, the CF local parameter associated with the DIBL effect varies with L and W:

$$\mathbf{CF} = \mathbf{CFL} \cdot \left(\frac{L_{EN}}{L_E} \right)^{\mathbf{CFLEXP}} \cdot \left(1 + \mathbf{CFW} \cdot \frac{W_{EN}}{W_E} \right) \qquad (1.18)$$

  With L_{EN}= W_{EN}=1 µm. CFL, CFLEXP and CFW are the global parameters. L_E and W_E are the electric length and width respectively. Classically, CF is function of $1/L^2$, as consequence the default values of CFLEXP is 2. But, the dependency with W is phenomenological.

- Empirical laws: without a real physical significance, they are generally of the form:

$$\mathbf{STVFB} = \mathbf{STVFBO} \cdot \left(1 + \mathbf{STVFBL} \cdot \frac{L_{EN}}{L_E} \right) \cdot \left(1 + \mathbf{STVFBW} \cdot \frac{W_{EN}}{W_E} \right) \cdot \left(1 + \mathbf{STVFBLW} \cdot \frac{L_{EN} \cdot W_{EN}}{L_E \cdot W_E} \right) \qquad (1.19)$$

All equations are given in section 3.1.

1.4. Law of temperature dependencies

In the UTSOI model, the temperature dependencies are taken into account:

- Naturally in the model’s core (as the subthreshold slope)
- Through an RC circuit used to model the self-heating effect
- By laws of temperature dependencies (for mobility, gate workfunction, etc.)

All equations are given in section 4.2.

2. Models Parameters

2.1. Global model flags and parameters

Name	Unit	Default	Min.	Max.	Description
TYPE	—	1	-1	1	Channel type parameter, +1=NMOS, -1=PMOS
TR	°C	21.0	-273.0	—	Reference temperature
SWSCALE	—	0	0	1	Flag for scaling rules, 0=local parameter set, 1=global parameter set
VERSION	—	1.11	—	—	Flag for model version, 1.11=old version, 1.13= new version
SWIGATE	—	0	0	1	Flag for gate current, 0=turn off
SWGIDL	—	0	0	1	Flag for GIDL current, 0=turn off
SWSHE	—	0	0	1	Flag for self heating effect, 0=turn off
SWRSMOD	—	0	0	1	Flag for access resistance calculation, 0=includes in mobility model, 1=using internal nodes
SWIGN	—	1	0	1	Flag for induced gate noise, 0=turn off

2.2. Parameters at local level (SWSCALE=0)

2.2.1. Instance parameters for local model

Name	Unit	Default	Min.	Max.	Description
ASOURCE	m^2	10^{-12}	0.0	—	Source region area
ADRAIN	m^2	10^{-12}	0.0	—	Drain region area
MULT	—	1	1	—	Number of device in parallel

2.2.2. Parameters for local model

Process parameters

Name	Unit	Default	Min.	Max.	Description
VFB	V	0.0	—	—	Flat-band voltage at TR
STVFB	V/K	5.10^{-4}	—	—	Temperature dependence of VFB
TOX	m	2.10^{-9}	10^{-10}	—	Gate oxide thickness
TSI	m	10^{-8}	10^{-9}	10^{-7}	Silicon film thickness
TBOX	m	10^{-7}	10^{-8}	10^{-6}	Buried oxide thickness
NSI	cm^{-3}	0.0	—	10^{18}	Lightly silicon film doping, 0=undoped

NSUB	cm^{-3}	3.10^{18}	10^{16}	10^{21}	Substrate doping, negative value=N-type, positive value=P-type
DVFBB	V	0.0	—	—	Offset of back-gate flat-band voltage
CT	—	0.0	0.0	—	Interface states factor
TOXOV	m	2.10^{-9}	10^{-10}	—	Overlap oxide thickness
NOV	cm^{-3}	0.0	10^{17}	10^{21}	Effective doping of overlap region, 0=no doping effect

Quantum effect parameter

Name	Unit	Default	Min.	Max.	Description
QMC	—	1	0	—	Quantum correction factor

Interface coupling parameter

Name	Unit	Default	Min.	Max.	Description
CIC	—	1.0	0.1	10.0	Substrate bias dependence factor of interface coupling

Short channel effect parameter

Name	Unit	Default	Min.	Max.	Description
PSCE	—	0.0	0.0	—	SCE-parameter above threshold

DIBL parameters

Name	Unit	Default	Min.	Max.	Description
CF	V^{-1}	0.0	0.0	—	DIBL-parameter
CFB	V^{-1}	0.0	0.0	—	Substrate bias dependence of CF
STCF	—	0.0	—	—	Temperature dependence of CF

Mobility parameters

Name	Unit	Default	Min.	Max.	Description
BETN	$m^2/V/s$	5.10^{-2}	0.0	—	Channel aspect ratio times zero-field mobility
STBET	—	1.0	—	—	Temperature dependence of BETN
MUE	m/V	0.5	0.0	—	Mobility reduction coefficient at TR
STMUE	—	0.0	—	—	Temperature dependence of MUE
THEMU	—	1.5	0.0	—	Mobility reduction exponent at TR
STTHEMU	—	1.5	—	—	Temperature dependence of THEMU
CS	—	0.0	0.0	—	Remote Coulomb scattering parameter at TR

CSB	—	0.0	—	—	Substrate bias dependence of CS
THECS	—	1.5	0.0	—	Remote Coulomb scattering exponent at TR
STTHECS	—	1.5	—	—	Temperature dependence of THECS
STCS	—	0.0	—	—	Temperature dependence of CS
XCOR	V^{-1}	0.0	0.0	—	Non-universality factor
STXCOR	—	0.0	—	—	Temperature dependence of XCOR
FETA	—	1.0	0.0	—	Effective field parameter

Series resistance parameters

Name	Unit	Default	Min.	Max.	Description
RS	Ω	30.0	0.0	—	Source/Drain series resistance at TR
RSG	—	0.0	0.0	—	Gate bias dependence of RS
THERSG	—	2.0	0.0	—	Gate bias dependence exponent of RS
STRS	—	1.0	—	—	Temperature dependence of RS

Velocity saturation parameters

Name	Unit	Default	Min.	Max.	Description
THESAT	V^{-1}	0.0	0.0	—	Velocity saturation parameter at TR
STTHESAT	—	1.0	—	—	Temperature dependence of THESAT
THESATB	—	0.0	-0.5	—	Substrate bias dependence of velocity saturation
THESATG	V^{-1}	0.0	0.0	—	Gate bias dependence of velocity saturation

Saturation voltage parameter

Name	Unit	Default	Min.	Max.	Description
AX	—	10.0	1.0	10.0	Linear/saturation transition factor

Channel length modulation parameters

Name	Unit	Default	Min.	Max.	Description
ALP	—	0.0	0.0	—	CLM pre-factor
ALP1	V	0.0	0.0	—	CLM enhancement factor above threshold
VP	V	0.05	10^{-10}	—	CLM logarithm dependence factor

Gate current parameters

Name	Unit	Default	Min.	Max.	Description

GCO		0.0	-10.0	10.0	Gate tunneling energy adjustment
IGINV	A	0.0	0.0	—	Gate to channel current pre-factor in inversion
IGOVINV	A	0.0	0.0	—	Gate to overlap current pre-factor in inversion
IGOVACC	A	0.0	0.0	—	Gate to overlap current pre-factor in accumulation
GC2CH	—	0.375	0.0	10.0	Gate current slope factor for gate to channel current
GC3CH	—	0.063	-2.0	2.0	Gate current curvature factor for gate to channel current
GC2OV	—	0.375	0.0	10.0	Gate current slope factor for overlap currents
GC3OV	—	0.063	-2.0	2.0	Gate current curvature factor for overlap currents
STIG	—	2.0	—	—	Temperature dependence of all gate currents
CHIB	V	3.1	1.0	—	Tunneling barrier height

Gate induced drain/source leakage current parameters

Name	Unit	Default	Min.	Max.	Description
AGIDL	A/V^3	0.0	0.0	—	GIDL pre-factor
BGIDL	V	41.0	0.0	—	GIDL probability factor at TR
STBGIDL	V/K	0.0	—	—	Temperature dependence of BGIDL
CGIDL	—	0.0	—	—	Substrate bias dependence of GIDL

Charge model parameters

Name	Unit	Default	Min.	Max.	Description
COX	F	10^{-14}	0.0	—	Oxide capacitance for intrinsic channel
CBOX	F/m^2	5.10^{-4}	0.0	—	Unit area buried oxide capacitance of drain/source region
CGBOV	F	0.0	0.0	—	Oxide capacitance for gate-substrate overlap
COV	F	0.0	0.0	—	Overlap capacitance
CFR	F	0.0	0.0	—	Outer fringe capacitance
CSDO	F	0.0	0.0	—	Outer drain-source capacitance

Self heating parameters

Name	Unit	Default	Min.	Max.	Description
RTH	°C/W	1500.0	0.0	—	Substrate thermal resistance
STRTH	—	0.0	0.0	—	Temperature dependence of RTH
CTH	W.s /°C	5.10^{-10}	0.0	—	Substrate thermal capacitance

Noise model parameters

Name	Unit	Default	Min.	Max.	Description
FNT	—	1.0	0.0	—	Thermal noise coefficient
NFA	V^{-1}/m^4	8.10^{22}	0.0	—	First coefficient of flicker noise
NFB	V^{-1}/m^2	3.10^7	0.0	—	Second coefficient of flicker noise
NFC	V^{-1}	0.0	0.0	—	Third coefficient of flicker noise
EF	—	1.0	0.1	—	Frequency coefficient of flicker noise

2.3. Parameters at global level (SWSCALE=1)

2.3.1. Instance parameters at global level

Name	Unit	Default	Min.	Max.	Description
L	m	10^{-6}	10^{-9}	—	Drawn channel length
W	m	10^{-6}	10^{-9}	—	Drawn channel width
SA	m	0.0	—	—	Distance between OD-edge and gate at source side
SB	m	0.0	—	—	Distance between OD-edge and gate at drain side
SD	m	0.0	—	—	Distance between neighboring fingers
ASOURCE	m^2	10^{-12}	0.0	—	Source region area
ADRAIN	m^2	10^{-12}	0.0	—	Drain region area
NF	—	1	1	—	Number of fingers
MULT	—	1	1	—	Number of device in parallel

2.3.2. Parameters at global level

Geometry scaling parameters

Name	Unit	Default	Min.	Max.	Description
LVAR0	m	0.0	—	—	Geometry-independent difference between physical and drawn gate lengths
LVARL	—	0.0	—	—	Length dependence of ΔLPS
LVARW	—	0.0	—	—	Width dependence of ΔLPS
LAP	m	0.0	—	—	Effective channel length reduction per side
WVARO	m	0.0	—	—	Geometry-independent difference between physical and drawn field-oxide opening
WVARL	—	0.0	—	—	Length dependence of ΔWOD
WVARW	—	0.0	—	—	Width dependence of ΔWOD
WOT	m	0.0	—	—	Effective reduction of channel width per side

DLQ	m	0.0	—	—	Effective channel length offset for CV
DWQ	m	0.0	—	—	Effective channel width offset for CV

Mechanical stress model parameters

Name	Unit	Default	Min.	Max.	Description
SAREF	m	10^{-6}	10^{-9}	—	Reference distance between OD edge to poly from one side
SBREF	m	10^{-6}	10^{-9}	—	Reference distance between OD edge to poly from other side
WLOD	m	0.0	—	—	Width parameter
KUO	m	0.0	—	—	Mobility degradation/enhancement coefficient
KVSAT	m	0.0	-1.0	1.0	Saturation velocity degradation/enhancement parameter
TKUO	—	0.0	—	—	Temperature coefficient of KUO
LKUO	—	0.0	—	—	Length dependence of KUO
WKUO	—	0.0	—	—	Width dependence of KUO
PKUO	—	0.0	—	—	Cross-term dependence of KUO
LLODKUO	—	0.0	0.0	—	Length parameter for mobility stress effect
WLODKUO	—	0.0	0.0	—	Width parameter for mobility stress effect
KVTHO	V.m	0.0	—	—	Threshold shift parameter
LKVTHO	—	0.0	—	—	Length dependence of KVTHO
WKVTHO	—	0.0	—	—	Width dependence of KVTHO
PKVTHO	—	0.0	—	—	Cross-term dependence of KVTHO
LLODVTH	—	0.0	0.0	—	Length parameter for threshold voltage stress effect
WLODVTH	—	0.0	0.0	—	Width parameter for threshold voltage stress effect
STETAO	m	0.0	—	—	ETAO shift factor related to threshold voltage change
LODETAO	—	1.0		—	ETAO shift modification factor

Process parameters

Name	Unit	Default	Min.	Max.	Description
VFBO	V	0.0	—	—	Geometry-independent flat-band voltage at TR
VFBL	—	0.0	—	—	Length dependence of VFB
VFBLEXP	—	1.0	—	—	Exponent describing length dependence of VFB
VFBW	—	0.0	—	—	Width dependence of VFB
VFBLW	—	0.0	—	—	Area dependence of VFB
STVFBO	V/K	5.10^{-4}	—	—	Geometry-independent temperature dependence of VFB
STVFBL	—	0.0	—	—	Length dependence of STVFB

STVFBW	—	0.0	—	—	Width dependence of STVFB
STVFBLW	—	0.0	—	—	Area dependence of STVFB
TOXO	m	2.10^{-9}	10^{-10}	—	Gate oxide thickness
TSIO	m	10^{-8}	10^{-9}	10^{-7}	Silicon film thickness
TBOXO	m	10^{-7}	10^{-8}	10^{-6}	Buried oxide thickness
NSIO	cm^{-3}	0.0	—	—	Lightly silicon film doping, 0=intrinsic doping
NSUBO	cm^{-3}	-3.10^{18}	10^{16}	10^{21}	Substrate doping, negative value=N-type, positive value=P-type
DVFBBO	V	0.0	—	—	Offset of back-gate flat-band voltage
CTO	—	0.0	0.0	—	Interface states factor
TOXOVO	m	2.10^{-9}	10^{-10}	—	Overlap oxide thickness
LOV	m	0.0	0.0	—	Length of gate/drain and date/source overlaps
NOVO	cm^{-3}	0.0	10^{17}	10^{21}	Effective doping of overlap region, 0=No doping effect

Quantum effect parameter

Name	Unit	Default	Min.	Max.	Description
QMC	—	1	0	—	Quantum correction factor

Interface coupling parameter

Name	Unit	Default	Min.	Max.	Description
CICO	—	1.0	0.1	10.0	Geometry-independent part of substrate bias dependence factor of interface coupling
CICL	—	0.0	—	—	Length dependence of CIC
CICLEXP	—	1.0	—	—	Exponent describing length dependence of CIC
CICW	—	0.0	—	—	Width dependence of CIC
CICLW	—	0.0	—	—	Area dependence of CIC

Short channel effect parameters

Name	Unit	Default	Min.	Max.	Description
PSCEL	—	0.0	0.0	—	Length dependence of short channel effect above threshold
PSCELEXP	—	1.0	—	—	Exponent describing length dependence of PSCE
PSCEW	—	0.0	0.0	—	Width dependence of PSCE

DIBL parameters

Name	Unit	Default	Min.	Max.	Description

CFL	V^{-1}	0.0	0.0	—	Length dependence of DIBL-parameter
CFLEXP	—	2.0	—	—	Exponent for length dependence of CF
CFW	—	0.0	—	—	Width dependence of CF
CFBO	—	0.0	0.0	—	Substrate bias dependence of CF
STCFO	—	0.0	—	—	Temperature dependence of CF

Mobility parameters

Name	Unit	Default	Min.	Max.	Description
UO	$m^2/V/s$	5.10^{-2}	—	—	Zero-field mobility at TR
BETNL	—	0.0	—	—	Second order length dependence of BETN
BETNLEXP	—	1.0	—	—	Exponent for second order length dependence of BETN
BETNW	—	0.0	—	—	Second order width dependence of BETN
STBETO	—	1.0	—	—	Geometry-independent part of temperature dependence of BETN
STBETL	—	0.0	—	—	Length dependence of STBET
STBETW	—	0.0	—	—	Width dependence of STBET
STBETLW	—	0.0	—	—	Area dependence of STBET
MUEO	m/V	0.5	0.0	—	Mobility reduction coefficient at TR
STMUEO	—	0.0	—	—	Temperature dependence of MUE
THEMUO	—	1.5	0.0	—	Mobility reduction exponent at TR
STTHEMUO	—	1.5	—	—	Temperature dependence of THEMU
CSO	—	0.0	0.0	—	Remote coulomb scattering parameter at TR
CSBO	—	0.0	0.0	—	Back bias dependence of CS
THECSO	—	1.5	0.0	—	Remote coulomb scattering exponent at TR3
STCSO	—	0.0	—	—	Temperature dependence of CS
STTHECSO	—	1.5	—	—	Temperature dependence of THECS
XCORO	V^{-1}	0.0	0.0	—	Non-universality factor
STXCORO	—	0.0	—	—	Temperature dependence of XCOR
FETAO	—	1.0	0.0	—	Effective field parameter

Series resistance parameters

Name	Unit	Default	Min.	Max.	Description
RSW1	Ω	30.0	—	—	Source/Drain series resistance for channel width WEN at TR
RSW2	—	0.0	—	—	Higher-order width scaling of source/drain series resistance
RSGO	—	0.0	-0.5	—	Gate-bias dependence of RS

THERSGO	—	2.0	—	—	Gate-bias dependence exponent of RS
STRSO	—	1.0	—	—	Temperature dependence of RS

Velocity saturation parameters

Name	Unit	Default	Min.	Max.	Description
THESATO	V^{-1}	0.0	0.0	—	Geometry-independent Velocity saturation parameter at TR
THESATL	—	0.0	—	—	Length dependence of THESAT
THESATLEXP	—	1.0	—	—	Exponent for length dependence of THESAT
THESATW	—	0.0	—	—	Width dependence of THESAT
THESATLW	—	0.0	—	—	Area dependence of THESAT
THESATGO	V^{-1}	0.0	0.0	—	Geometry-independent gate bias dependence of velocity saturation parameter at TR
STTHESATO	—	1.0	—	—	Geometry-independent of temperature dependence of THESAT
STTHESATL	—	0.0	—	—	Length dependence of STTHESAT
STTHESATW	—	0.0	—	—	Width dependence of STTHESAT
STTHESATLW	—	0.0	—	—	Area dependence of STTHESAT
THESATBO	V^{-1}	0.0	-0.5	1.0	Substrate bias dependence of velocity saturation

Saturation voltage parameter

Name	Unit	Default	Min.	Max.	Description
AXO	—	10.0	—	—	Geometry-independent of linear/saturation transition factor
AXL	—	0.0	0.0	—	Length dependence of AX
AXLEXP	—	1.0	0.0	—	Exponent for length dependence of AX

Channel length modulation parameters

Name	Unit	Default	Min.	Max.	Description
ALPL1	—	0.0	0.0	—	Length dependence of CLM pre-factor ALP
ALPLEXP	—	1.0	—	—	Exponent for length dependence of ALP
ALPL2	—	0.0	—	—	Second order length dependence of ALP
ALPW	—	0.0	—	—	Width dependence of ALP
ALP1L1	V	0.0	0.0	—	Length dependence of CLM enhancement factor
ALP1LEXP	—	1.0	—	—	Exponent for length dependence of ALP1
ALP1L2	—	0.0	—	—	Second order length dependence of ALP1
ALP1W	—	0.0	—	—	Width dependence of ALP1

VPO	V	0.05	10^{-10}	—	CLM logarithm dependence factor

Gate current parameters

Name	Unit	Default	Min.	Max.	Description
GCOO	—	0.0	-10.0	10.0	Gate tunneling energy adjustment
IGINVLW	A	0.0	0.0	—	Gate channel cu1.0rrent pre-factor for a channel area of WEN.LEN
IGOVINVW	A	0.0	0.0	—	Gate to overlap current pre-factor in inversion for an overlap of WEN.LOV
IGOVACC W	A	0.0	0.0	—	Gate to overlap current pre-factor in accumulation overlap of WEN.LOV
GC2CHO	—	0.375	0.0	10.0	Gate current slope factor for gate to channel current
GC3CHO	—	0.063	-2.0	2.0	Gate current curvature factor for gate to channel current
GC2OVO	—	0.375	0.0	10.0	Gate current slope factor for overlap currents
GC3OVO	—	0.063	-2.0	2.0	Gate current curvature factor for overlap currents
STIGO	—	2.0	—	—	Temperature dependence of all gate currents
CHIBO	V	3.1	1.0	—	Tunneling barrier height

Gate induced drain/source leakage current parameters

Name	Unit	Default	Min.	Max.	Description
AGIDLW	A/V^3	0.0	0.0	—	Width dependence of GIDL pre-factor
BGIDLO	V	41.0	0.0	—	GIDL probability factor at TR
STBGIDLO	V/K	0.0	—	—	Temperature dependence of BGIDL
CGIDLO	—	0.0	—	—	Substrate bias dependence of GIDL

Charge model parameters

Name	Unit	Default	Min.	Max.	Description
CGBOVL	F	0.0	0.0	—	Oxide capacitance for gate-substrate overlap
CFRW	F	0.0	0.0	—	Outer fringe capacitance

Self heating parameters

Name	Unit	Default	Min.	Max.	Description
RTHO	°C/W	1500.0	0.0	—	Geometry-independent part of substrate thermal resistance
RTHL	—	0.0	—	—	Length dependence of RTH
RTHW	—	0.0	—	—	Width dependence of RTH
RTHLW	—	0.0	—	—	Area dependence of RTH

CTHO	W.s /°C	5.10^{-10}	0.0	—	Geometry-independent part of substrate thermal capacitance
STRTHO	—	0.0	—	—	Temperature dependence of substrate thermal resistance

Noise model parameters

Name	Unit	Default	Min.	Max.	Description
FNTO	—	1.0	0.0	—	Thermal noise coefficient
NFALW	V^{-1}/m^4	8.10^{22}	0.0	—	First coefficient of flicker noise
NFBLW	V^{-1}/m^2	3.10^{7}	0.0	—	Second coefficient of flicker noise
NFCLW	V^{-1}	0.0	0.0	—	Third coefficient of flicker noise
EFO	—	1.0	0.1	—	Frequency coefficient of flicker noise

3. Parameter extraction

3.1. Introduction

In this section, a guideline of the extraction procedure is proposed. All routines are not detailed because the extraction procedure depends of the device specifications and the IC design applications. Note that for described routines, the extraction procedures are given as examples and can be modified by the users.
The main steps of the proposed procedures are listed in the following table. For some parameters, named RS, RSG, THERSG, RTH and CTH, an independent extraction methods are used (steps I and II) and that to reduce the risk of compensation. Indeed, the parameters of access resistances (RS, RSG and THERSG) and those of the thermal impedance (RTH and CTH, respectively), can be compensated by those of the carrier mobility and the short channel effects. Note that steps I and II are not described in this document.

Step	Description
I	Extraction of the access resistance parameter RS with its gate voltage dependency (RSG and THERSG) using an independent method
II	Extraction of the self heating effect parameters (thermal resistance RTH and thermal capacitance CTH) using an independent method
III	Extraction of local parameters
IV	Extraction of global parameters
V	Validation and fine tuning

Global parameters (step IV) are obtained from local parameters that are themselves extracted (step III) through the characteristics I(V) and C(V). For example: the extraction of the flat-band voltage VFB for devices of different lengths provides the VFB(L) curve. This curve is used to determine the values of the parameters involved in the law of dependence of VFB: VFBO, and VFBL VFBLEXP. This approach is made possible by the notion of local and global levels.

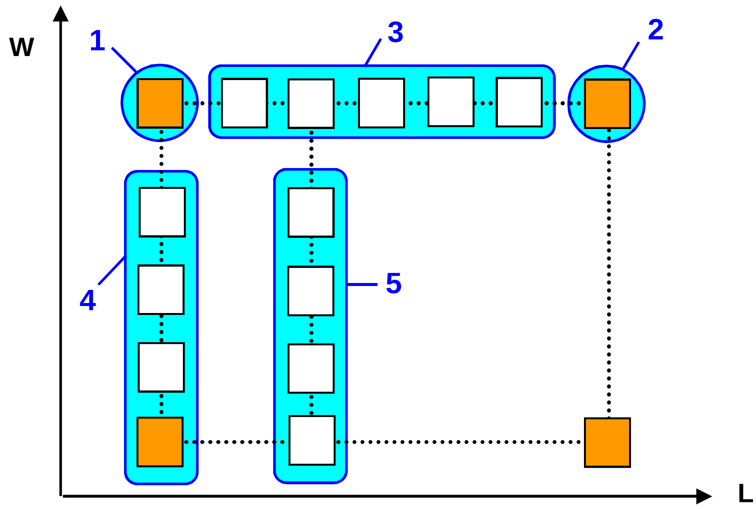
The validation (step V) consists to compare the results from the model and a global parameter set with the electrical the characteristics I(V) and C(V) for all devices. Finally, some global parameters can be fine tuned to improve accuracy.

3.2. Geometrical scaling

The geometric space (next figure) shows all the devices to be used during the extraction in step III. Their local settings are divided as follows:

- Those considered as constant. They are common to all sets of local parameters and can be grouped into three classes:
    - Known parameter values : mainly those related to the process, thicknesses such as TSI and TBOX, doping, etc. The extraction of these parameters is not necessary.

  - Extracted parameters on a long and wide transistor (device 1 on the next figure): for example, the parameters of the mobility degradation. Their extractions on other geometries are not pertinent because their electrical signatures are masked by other effects.
  - Extracted parameters on a short and wide transistor (device 2): For example, THESATG, the gate voltage dependency of the velocity saturation, ie, all parameters where the phenomena are exacerbated and so visible for this geometry.
- Those with geometrical dependencies and extracted for each transistor. All of the devices 3 and 4 are dedicated for the extraction of geometrical scaling parameters. All of the transistors 5 are optional and are used for checking.



3.3. Measurements

The extraction procedures require 5 electrical characteristics for each device. 3 optional DC-measurement can be used for checking or fine tuning. Measurement setups are details in the following table.

Characteristics	Biasing	Utility
$C_{GG}(V_{GS})$	V_{GS}= -V_{DD} to V_{DD} /step 10 mV V_{DS} = 0 V V_{BS} = 0 V f=1 MHz	Required
$I_G(V_{GS})$ and its derivative	V_{GS}= -V_{DD} to V_{DD} /step 10 mV V_{DS} = 0 V V_{BS} = [-2V_{DD} ; -V_{DD} ; 0 ; V_{DD} ; 2V_{DD}]	Required
$I_D(V_{GS})$ and $g_m(V_{GS})$ in linear regime	V_{GS} = -V_{DD} to V_{DD} /step 10 mV V_{DS} = 50 mV V_{BS} = [-2V_{DD} ; -V_{DD} ; 0 ; V_{DD} ; 2V_{DD}]	Required
$I_D(V_{GS})$ and $g_m(V_{GS})$ in saturation	V_{GS} = 0 to V_{DD} /step 10 mV V_{DS} = V_{DD} V_{BS} = [-2V_{DD} ; -V_{DD} ; 0 ; V_{DD} ; 2V_{DD}]	Required
$I_D(V_{DS})$ and $g_{DS}(V_{DS})$	V_{GS} = 0 to V_{DD} /step 200 mV V_{DS} = 0 to V_{DD} /step 10 mV V_{BS} = 0 V	Required

$I_D(V_{GS})$ and $g_m(V_{GS})$	V_{GS} = $-V_{DD}/2$ to V_{DD} /step 10 mV $V_{DS} = V_{DD}/2$ V_{BS} = [$-2V_{DD}$; $-V_{DD}$; 0 ; V_{DD} ; $2V_{DD}$]	Optional
$I_D(V_{DS})$ and $g_{DS}(V_{DS})$	V_{GS} = 0 to V_{DD} /step 200 mV V_{DS} = 0 to V_{DD} /step 10 mV $V_{BS} = -2V_{DD}$	Optional
$I_D(V_{DS})$ and $g_{DS}(V_{DS})$	V_{GS} = 0 to V_{DD} /step 200 mV V_{DS} = 0 to V_{DD} /step 10 mV $V_{BS} = 2V_{DD}$	Optional

3.4. Extraction of local parameters

This section is focused on the extraction of local parameters (step III). As previously mentioned the extraction flow requires a long and wide transistor, a short and wide and several intermediate geometries. Classically for each device, the flow in local level includes the extraction of:

1) C(V) parameters: gate oxide capacitance COX and the electrical gate oxide thickness TOX. These parameters are independent in local level. To ensure consistency between their values in global level, TOX is obtained from $\mathbf{TOX} = \varepsilon_{OX} \frac{W_{E,CV} \cdot L_{E,CV}}{\mathbf{COX}}$ where ε_{ox} is the dielectric permittivity of gate oxide and $W_{E,CV}$ and $L_{E,CV}$ are calculated from the geometric dimensions.
2) Parameters in linear regime: mobility and subthreshold slope parameters.
3) Parameters in saturation: mainly those of DIBL, velocity saturation and channel length modulation parameters.
4) Parameter for transition between linear and saturation regime: AX parameter obtained from $I_D(V_{DS})$ and $G_{DS}(V_{DS})$ characteristics. Note that these last electrical characteristics are also used to define the channel length modulation parameters.
5) Parameters of the gate current I_G: 7 parameters obtained thanks to $I_G(V_{GS})$ characteristics.

3.4.1. Parameter extraction of large transistor

The extraction routine of the large transistor is given by the following table:

Steps	Extracted parameters	Effect	Electrical data	Temperature (°C)
1	TSI, TBOX, NSUB, NSI, NOV	Process parameters	Not described	Ambient
2	RS, RSG, THERSG, RTH, CTH	From external extraction routine	Not described	
3	CFR	Parasitic capacitances	$C_{GG}(V_{GS})$	
4	COX, TOX, TOXOV	Equivalent gate oxide thickness		
5	BETN	Mobility at high field	$I_D(V_{GS})$ and $g_m(V_{GS})$ in linear regime	
6	VFB, CT, CIC	In subthreshold region		
7	BETN, CS, THECS, CSB	Mobility at low field		
8	BETN, MUE,	Mobility at high field		

	THEMU, XCOR			
9	IGOVINV, GC2OV, GC3OV	Gate tunneling currents	$I_G(V_{GS})$ and its derivative	
10	IGOVACC			
11	IGINV, GC2CH, GC3CH			
12	STVFB	Flatband voltage versus temperature	$I_D(V_{GS})$ and $g_m(V_{GS})$ in linear regime	-40 to 125
13	STBET, STMUE, STTHEMU	Mobility versus temperature		
14	STIG	Gate current versus temperature	$I_G(V_{GS})$ and its derivative	

3.4.2. Parameter extraction of short transistor

The extraction routine of the short transistor is given by the following table:

Steps	Extracted parameters	Effect	Electrical data	Temperature (°C)
1	TSI, TBOX, NSUB, NSI, NOV	Process parameters	Not described	Ambient
2	RS, RSG, THERSG, RTH, CTH	From external extraction routine	Not described	
3	CFR, COX, TOX, TOXOV, CT, MUE, THEMU, XCOR, CS, THECS, CSB, GC2OV, GC3OV, GC2CH, GC3CH, STMUE, STTHEMU, STIG BETN	Imported parameters	See parameter extraction of the large transistor	
4	VFB, CIC, PSCE	In subthreshold region	$I_D(V_{GS})$ and $g_m(V_{GS})$ in linear regime	
5	BETN, RS	Mobility at high field		
6	CF, CFB	DIBL	$I_D(V_{GS})$ and $g_m(V_{GS})$ in saturation	
7	THESAT, THESATG, THESATB	Velocity saturation		
8	AX	Transition between linear and saturation regimes	$I_D(V_{DS})$ and $g_{DS}(V_{DS})$	
9	THESAT, ALP, ALP1	Channel length modulation and velocity saturation		
10	IGOVINV	Gate tunneling currents	$I_G(V_{GS})$ and its derivative	
11	IGOVACC			
12	IGINV			
13	STVFB	Flatband voltage versus temperature	$I_D(V_{GS})$ and $g_m(V_{GS})$ in linear regime	-40 to 125
14	STBET, STRS	Mobility versus temperature		
15	STCF	DIBL versus temperature	$I_D(V_{GS})$ and $g_m(V_{GS})$ in saturation	

16	STTHESAT	Velocity saturation versus temperature		

3.4.3. Parameter extraction of intermediate geometries

The extraction routine of the intermediate transistor geometries is given by the next table:

Steps	Extracted parameters	Effect	Electrical data	Temperature (°C)
1	TSI, TBOX, NSUB, NSI, NOV	Process parameters	Not described	Ambient
2	RSG, THERSG, RTH, CTH	From external extraction routine	Not described	
3	CFR, COX, TOX, TOXOV, CT, MUE, THEMU, XCOR, CS, THECS, CSB, GC2OV, GC3OV, GC2CH, GC3CH, STMUE, STTHEMU, STIG BETN	Imported parameters from the large transistor parameter extraction	See parameter extraction of the large transistor	
4	RS, CFB, THESATG, THESATB, STRS, STCF,	Imported parameters from the short transistor parameter extraction	See parameter extraction of the short transistor	
5	VFB, CIC, PSCE	In subthreshold region	$I_D(V_{GS})$ and $g_m(V_{GS})$ in linear regime	
6	BETN	Mobility at high field		
7	CF	DIBL	$I_D(V_{GS})$ and $g_m(V_{GS})$ in saturation	
8	THESAT	Velocity saturation		
9	AX	Transition between linear and saturation regimes	$I_D(V_{DS})$ and $g_{DS}(V_{DS})$	
10	THESAT, ALP, ALP1	Channel length modulation and velocity saturation		
11	IGOVINV	Gate tunneling currents	$I_G(V_{GS})$ and its derivative	
12	IGOVACC			
13	IGINV			
14	STVFB	Flatband voltage versus temperature	$I_D(V_{GS})$ and $g_m(V_{GS})$ in linear regime	-40 to 125
15	STBET	Mobility versus temperature		
16	STTHESAT	Velocity saturation versus temperature	$I_D(V_{GS})$ and $g_m(V_{GS})$ in saturation	

3.5. Extraction of global parameters

Several global parameters are independents to the geometry. In this case, the global parameters are named as “local parameter name” + O. For example, the gate oxide thickness in local level is noted TOXO in global level.

For others parameters (25 local parameters), The transition in global level is directly obtained the use of the local parameter values, themselves obtained from the characteristics C (V) and I (V). All equations of local versus global parameters are given in section 3.1.

4. Operating output variables

4.1. Total DC currents

Name	Unit	Equation	Description
Ide	A	$I_{ds} + I_{gidl} + I_{gisl} - I_{gd}$	Total DC drain current
Ige	A	$I_{gs} + I_{gd}$	Total DC gate current
Ise	A	$-I_{ds} - I_{gidl} - I_{gisl} - I_{gs}$	Total DC source current
Ibe	A	0	Total DC bulk current

4.1. Internal DC currents

Name	Unit	Equation	Description
Ids	A	I_{ds}	DC Drain current, excluding avalanche, tunnel, GISL, GIDL, and junction currents
Idb	A	0	DC drain-bulk current
Isb	A	0	DC source-bulk current

4.1. Applied Voltages

Name	Unit	Equation	Description
Vds	V	V_{ds}	Drain-Source DC voltage
Vsb	V	V_{sb}	Source-Bulk DC voltage
Vgs	V	V_{gs}	Gate-Source DC voltage

4.1. Transconductances and conductance

Name	Unit	Equation	Description
Gm	S	$\frac{\partial I_{ds}}{\partial V_{gs}} + \frac{\partial I_{gidl}}{\partial V_{gs}} + \frac{\partial I_{gisl}}{\partial V_{gs}} + \frac{\partial I_{gd}}{\partial V_{gs}}$	DC transconductance
Gmb	S	$\frac{\partial I_{ds}}{\partial V_{bs}} + \frac{\partial I_{gidl}}{\partial V_{bs}} + \frac{\partial I_{gisl}}{\partial V_{bs}} + \frac{\partial I_{gd}}{\partial V_{bs}}$	DC bulk transconductance
Gds	S	$\frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{gidl}}{\partial V_{ds}} + \frac{\partial I_{gisl}}{\partial V_{ds}} + \frac{\partial I_{gd}}{\partial V_{ds}}$	DC output conductance

4.1. Transcapacitances and capacitances

Capacitances include parasitic elements (overlaps, drain-source diffusion area,…)

Name	Unit	Equation	Description
Cdd	F	$\frac{\partial Q_{di}}{\partial V_{ds}} + \frac{\partial Q_{ds,ext}}{\partial V_{ds}} + \frac{\partial Q_{gd,ext}}{\partial V_{ds}} - \frac{\partial Q_{d,sub}}{\partial V_{ds}}$	AC drain capacitance
Cdg	F	$-\frac{\partial Q_{di}}{\partial V_{gs}} + \frac{\partial Q_{gd,ext}}{\partial V_{gs}}$	AC drain to gate capacitance
Cdb	F	$-\frac{\partial Q_{di}}{\partial V_{bs}} + \frac{\partial Q_{d,sub}}{\partial V_{bs}}$	AC drain to bulk capacitance
Cds	F	$C_{dd} + C_{dg} + C_{db}$	AC drain to source capacitance
Cgd	F	$-\frac{\partial Q_{gi}}{\partial V_{ds}} + \frac{\partial Q_{gd,ext}}{\partial V_{ds}}$	AC gate to drain capacitance
Cgg	F	$\frac{\partial Q_{gi}}{\partial V_{gs}} + \frac{\partial Q_{gs,ext}}{\partial V_{gs}} + \frac{\partial Q_{gd,ext}}{\partial V_{gs}} + \frac{\partial Q_{gb,ext}}{\partial V_{gs}}$	AC gate capacitance
Cgb	F	$-\frac{\partial Q_{gi}}{\partial V_{bs}} - \frac{\partial Q_{gb,ext}}{\partial V_{bs}}$	AC gate to bulk capacitance
Cgs	F	$C_{gg} + C_{gd} + C_{gb}$	AC gate to source capacitance
Cbd	F	$-\frac{\partial Q_{bi}}{\partial V_{ds}} - \frac{\partial Q_{d,sub}}{\partial V_{ds}}$	AC bulk to drain capacitance
Cbg	F	$-\frac{\partial Q_{bi}}{\partial V_{gs}} + \frac{\partial Q_{gb,ext}}{\partial V_{gs}}$	AC bulk to gate capacitance
Cbb	F	$\frac{\partial Q_{bi}}{\partial V_{bs}} - \frac{\partial Q_{gb,ext}}{\partial V_{bs}} + \frac{\partial Q_{s,sub}}{\partial V_{bs}} + \frac{\partial Q_{d,sub}}{v V_{bs}}$	AC bulk capacitance
Cbs	F	$C_{bb} + C_{bd} + C_{bg}$	AC bulk to source capacitance
Csd	F	$C_{dd} + C_{gd} + C_{bd}$	AC source to drain capacitance
Csg	F	$C_{dg} + C_{gg} + C_{bg}$	AC source to gate capacitance
Csb	F	$C_{db} + C_{gb} + C_{bb}$	AC source to bulk capacitance
Css	F	$C_{sg} + C_{sd} + C_{sb}$	AC source capacitance

4.1. Derived parameters

Name	Unit	Equation	Description
Vth	V	vth	Threshold voltage including back bias and drain bias effects (see §4.3.2)
Vgt	V	$V_{gs} - vth$	Effective gate drive voltage including back bias and drain bias effects
Vdss	V	V_{dsat}	Drain saturation voltage at actual bias
Vsat_marg	V	$V_{ds} - V_{dsat}$	V_{ds} margin
Self_gain		Gm/Gds	Transistor self gain
Rout	Ω	$1/Gds$	AC output resistor
Beff	A/V^2	$2 \cdot \frac{\lvert ide \rvert}{Vgt^2}$	Gain factor

Fug	Hz	$\frac{Gm}{2 \cdot \pi \cdot Cgg}$	Unity gain frequency at actual bias
Rgate	Ω	0	MOS gate resistance (not includes in this version)
Gmoverid	1/V	$\frac{Gm}{I_{ds}}$	Gm over Id
Vearly	V	$\frac{\lvert ide \rvert}{Gds}$	Equivalent early voltage

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