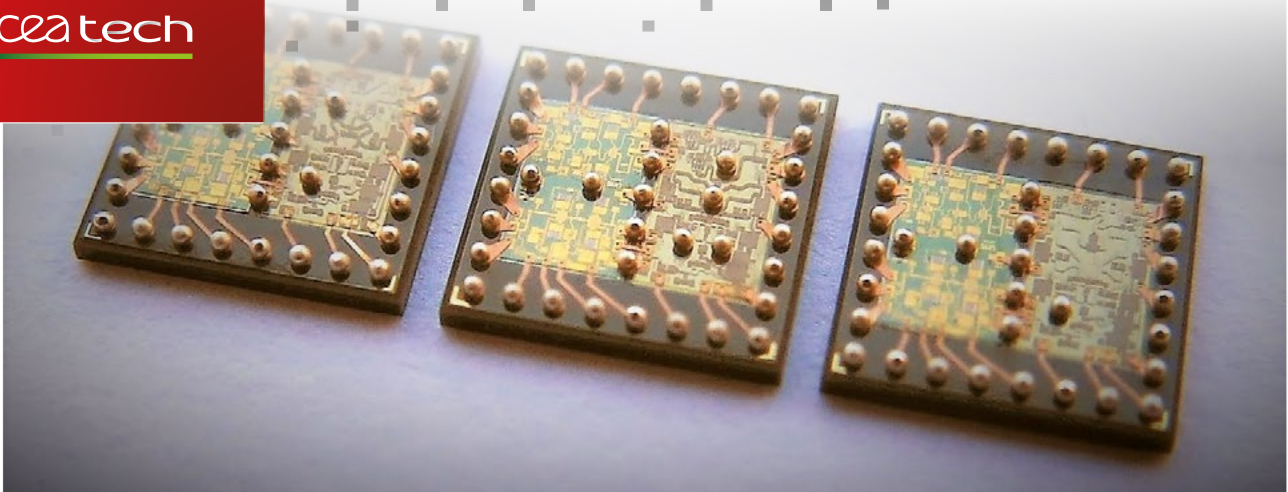
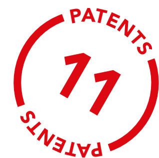


Fan-out wafer-level packaging



Advanced packaging technology for heterogeneous system-in-package (SiP)

What is fan-out wafer-level packaging technology?

CEA-Leti offers a competitive fan-out wafer-level packaging technology using 8" wafers. Based on the reconstruction of substrates around individual chips, this technology has become an iconic part of any "More than Moore" strategy, fueling high-potential multi-chip system-in-package (SiP) since the mid-2000s.

Eliminating the need for intermediate laminated substrates has enabled the integration of high performance systems at a reduced cost and footprint. It has also paved the way for applications that would have been difficult to address with conventional packaging.

Applications

RF front-end modules for wireless communications and radar

- Hybrid modules combining III-V, SiC and CMOS
- Integration of passive components
- Antenna in package

High-speed optical interconnect

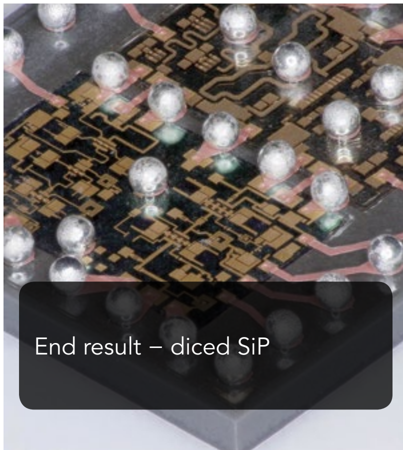
- VCSEL, PIN Diode and silicon photonics system-in-package

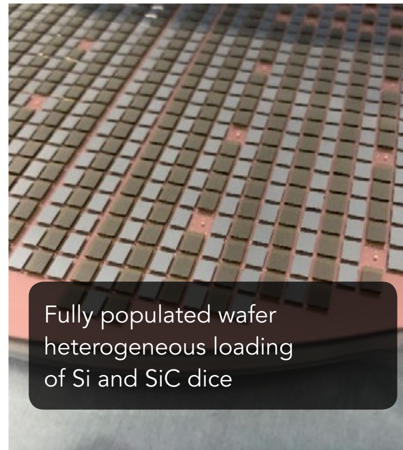
Sensing systems

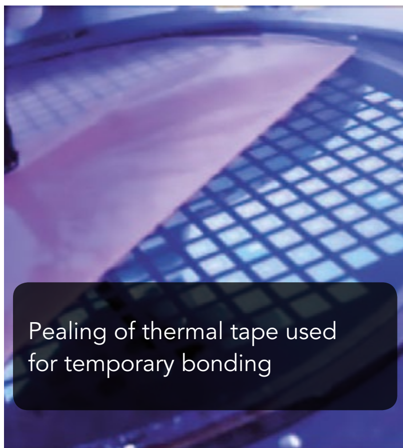
- Integration of various sensors such as MEMS with drivers IC

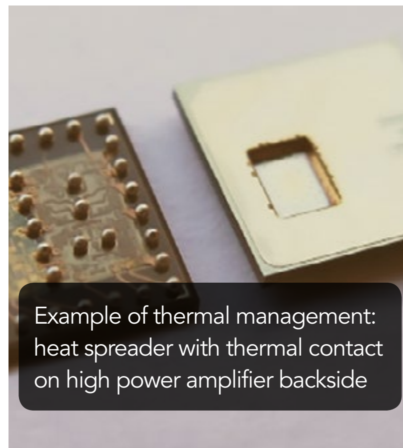
Expertise

From design fabrication down to UBM level, CEA-Leti offers extensive expertise in fan-out wafer-level packaging to industrial partners on the lookout for competitive heterogeneous system-in-package (SiP) solutions.


End result – diced SiP


Fully populated wafer heterogeneous loading of Si and SiC dice


Pealing of thermal tape used for temporary bonding


Example of thermal management: heat spreader with thermal contact on high power amplifier backside

Publications

- System in package embedding III-V chips by fan-out wafer-level packaging for RF applications, ECTC, 2021, pp. 2016-2023
- 3D embedded wafer-level packaging technology development for smart card SIP application, EPTC, 2012, pp. 304-310,
- Wafer level processing of 3D system in package for RF and data application; Proceedings Electronic Components and Technology, ECTC 2005, pp. 356-361 Vol. 1

Interested in this technology?

Sylvie Joly
sylvie-j.joly@cea.fr
+33 645 150 298

CEA-Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
Minatec Campus | 17 avenue des Martyrs | 38054 Grenoble Cedex 9 | France
www.cea-leti.com

@CEA_Leti CEALeti CEA-Leti

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