WHAT IS LETI’S Si PIC PLATFORM?

CEA-Leti’s fabrication platform for silicon Photonic Integrated Circuits (PIC) enables large-scale integration of active and passive devices in a flexible CMOS-compatible process.

Beyond silicon, the platform also offers integration of SiN and III-V bonded epi layers on the same wafer, providing the advantages of each material. The convergence of various photonic platforms combined with CEA-Leti’s multi-material process helps address numerous applications with the same technology.

APPLICATIONS

Several applications come with this photonics-technologies convergence on a Si CMOS platform, including:

- **Communication:** Telecom, Datacom, 5G infrastructures, quantum cryptography for cybersecurity
- **Computing:** Computer communication for High Performance Computing (HPC), quantum computing and neuromorphic computing for AI
- **Sensing:** optical gas sensing, structural health monitoring and 3D sensing such as LiDAR
Benefits of this convergence offer CEA-Leti’s partners a greater number of functions on photonic integrated circuits (PIC), fabricated on an advanced CMOS-compatible platform.

CEA-Leti’s key achievements:

- Mature device library for O-band and C-band in a Process - Design Kit (PDK), compatible with conventional CAD tools.
- III-V integration on CMOS-compatible process through collective die bonding
- Multilayer Si/Si or SiN/Si for 3D photonics
- 2D beam steering based on SiN OPA
- Tunable DBR, DFB, racetrack lasers

CEA-Leti’s Optics and Photonics Division will:

- Leverage its brand new immersion lithography to deliver smaller feature-size devices and low sidewall roughness
- Focus on ultra low insertion loss and high efficiency Si & SiN devices
- Develop high efficiency NbN Superconducting Single Photon Detector (SSPD)

WHAT’S NEXT?

CEA-Leti’s Optics and Photonics Division will:

- Leverage its brand new immersion lithography to deliver smaller feature-size devices and low sidewall roughness
- Focus on ultra low insertion loss and high efficiency Si & SiN devices
- Develop high efficiency NbN Superconducting Single Photon Detector (SSPD)

INTERESTED IN THIS TECHNOLOGY?

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KEY FEATURES:

- 300 mm SOI substrate with 310 nm Si, other thicknesses available
- Multilevel silicon patterning for silicon heights of 0, 65, 165 and 310 nm
- Selective Ge epitaxy
- SiN layer (optional)
- TiTiN heater
- 6 implant levels for p-type and n-type for electro-optic modulators and silicon doped heaters
- Silicide tungsten contact
- III-V collective die bonding