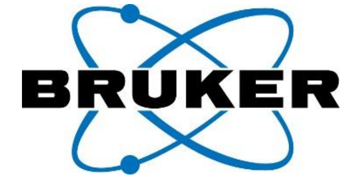
High-Resolution X-ray Diffraction Characterization and Metrology for Advanced Logic

Dr. Juliette van der Meer



Innovation with Integrity

Bruker Semiconductor Division

Acknowledgements

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- Colleagues
  - Paul Ryan & John Wall (BSEMI UK)
  - Matthew Wormington, Peter Gin & Kevin Matney (BSEMI US)
  - Nikolai Kasper & Sven Krannich (BSEMI Germany)

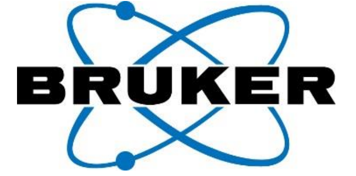
- Collaborators
  - Andreas Schulze formerly of IMEC (now at AMAT)

- The study on sGe nanowires and III-V materials in confined volumes was undertaken as part of the ongoing 3DAM Project (https://cordis.europa.eu/project/rcn/202643_en.html).
  - This project has received funding from the Electronic Component Systems for European Leadership Joint Undertaking under grant agreement No 692527. This Joint Undertaking receives support from the European Union's Horizon 2020 research and innovation programme and Netherlands, Belgium, France, Hungary, Ireland, Denmark, Israel.

Outline

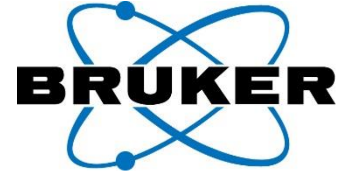
- HRXRD in the semiconductor industry
  - History
  - In-line tools / use in the silicon industry
- Principles of HRXRD
- Examples of advanced logic applications
  - SiGe fins etched from a blanket film
  - Selectively grown Ge/SiGe fins
  - SiGe/Si for nanowire / nanosheet FETs
- Conclusions

What can HRXRD give us, who uses it and for what?



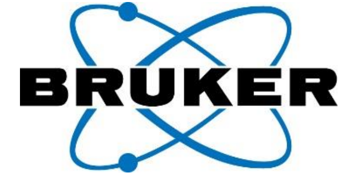
- High-resolution X-ray diffraction (HRXRD) provides a wealth of information about epitaxial materials
  - Crystal lattice misfit/strain, tilt and defectivity/quality…
  - Composition and thickness
  - Arrangement, shape and lattice distortion in arrays of patterned structures
- It is first-principles (no calibration) and non-destructive characterization and metrology technique
  - Does not require material/process dependent optical constants
  - Accurate and precise with very few assumptions
- Has been used for 30+ years in the compound semiconductor industry for a wide range of materials (III-V, III-nitride, II-VI…) and devices (LEDs, lasers, CPV, detectors…)
- Introduced into the Si industry with strain engineering for sub-100 nm logic devices
- Used for R&D, chamber qual., process diagnostics / ramp and in-line metrology

Challenges for HRXRD metrology for advanced logic applications



- Blanket wafer measurements are frequently used for epi chamber quals and materials / process development in logic fabs
  - Limited value for in-line monitoring
- Measurements on product wafers involve
  - Small pads
    - Scribe-line test structures (50 x 50 μm^2 or smaller)
  - Arrays of very small structures
    - Coverage is low (e.g. < 25% for 10 nm CD and 40 nm pitch line structures)
  - Heterogeneous structures with complex strain distributions
- Consequently, diffracted X-ray intensity is rather low and distributed in reciprocal space
- Challenges are drivers for innovation in HRXRD solutions
  - High-brightness X-ray beamlines (source + optics)
  - Advanced detectors
  - Flexible, innovative analytical software toolboxes

HRXRD tools for semiconductor production, history and future



Si developments

CS developments

QC1 / QC2
First PC diffractometers

QC200
First 200 mm system with automated analysis

Fab200
First fully automated 200mm system

BedeMetrix-F
First fully automated 300mm system

JV QC3
Production tool for GaN LEDS

JVX7300LSI
Fully automated fast RSMs

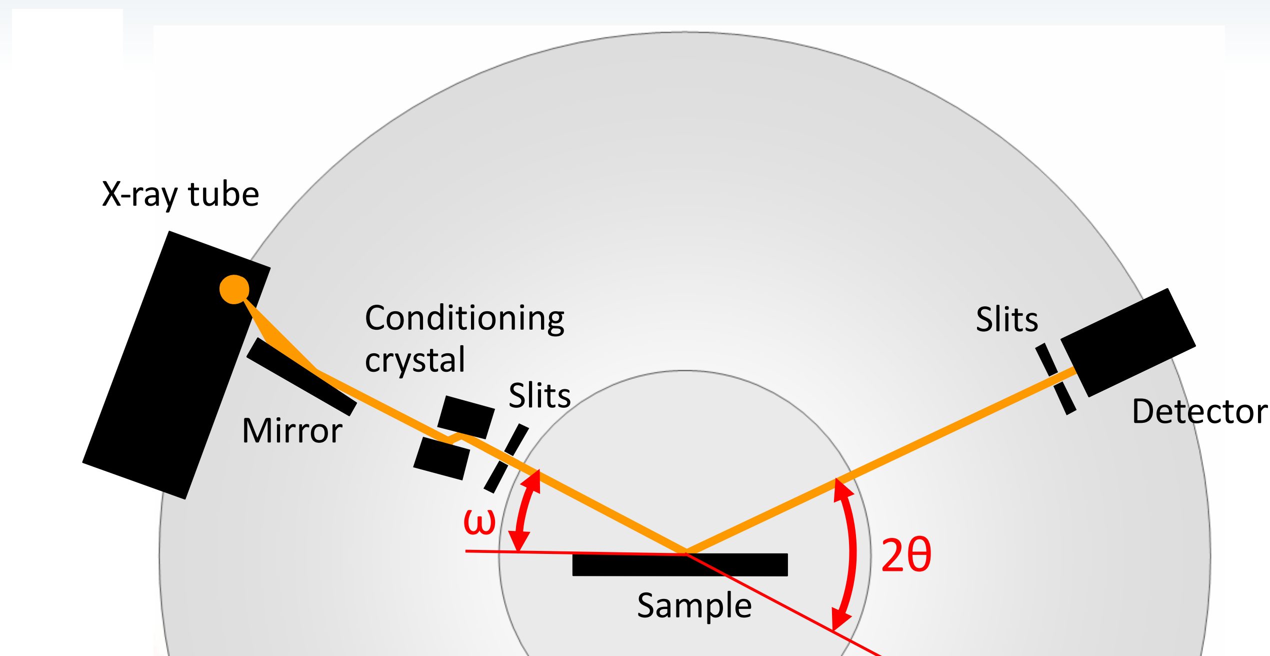
JVX8300S
Small spot fast RSMs

QCVelox
Enhanced production tool GaN, LED

- Brighter X-ray sources
- Optics
- Detectors
- Analysis SW

1986 | 2000 | 2002 | 2004 | 2008 | 2015 | **2018-19**

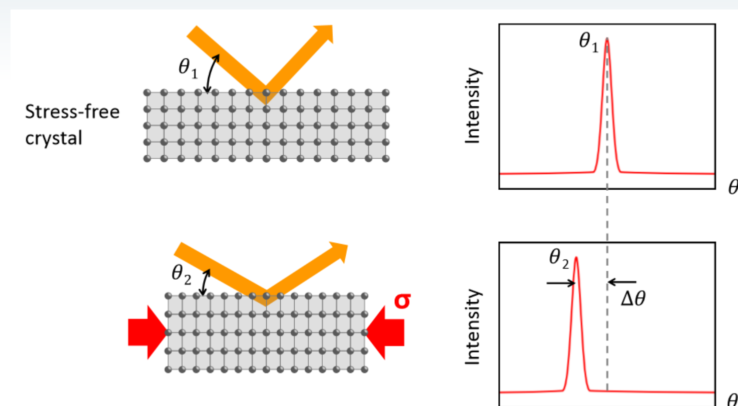
High resolution XRD setups

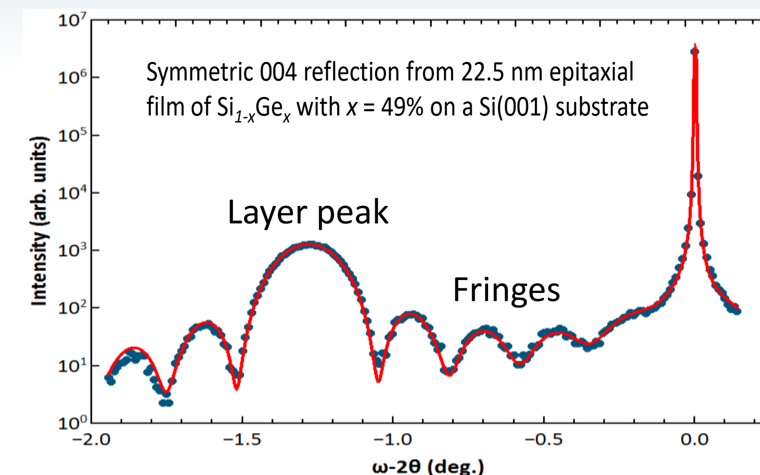


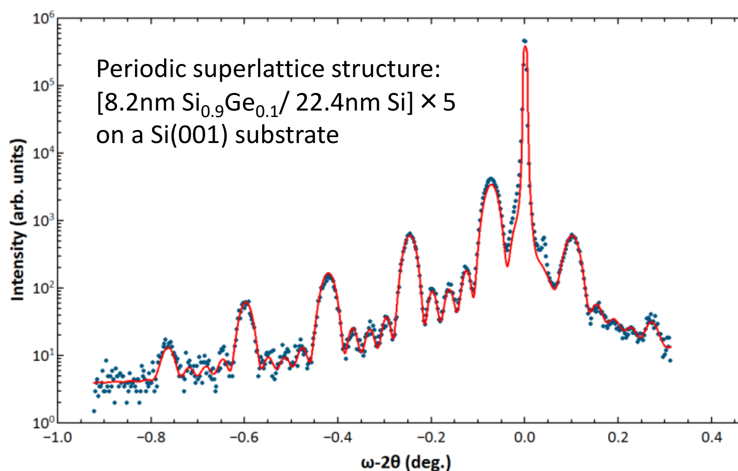
- Most common setup uses a parallel beam and point (0D) detector
  - Source and detector angles scanned using a motorized goniometer
  - Large (mm) and small (50 um) spot configurations are available

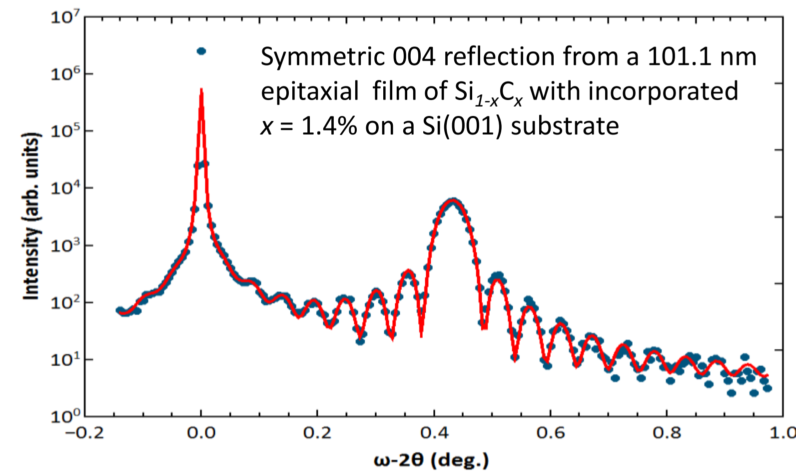
Examples of fully strained epilayers

- X-ray diffraction uses the crystal lattice as a "strain gauge"
- The relation between the lattice parameter and diffraction angle is defined by Bragg's law, $2d \sin\theta_B = n\lambda$
- Layer peak position relates directly to composition for fully strained layer
- Interference fringes give layer thickness information

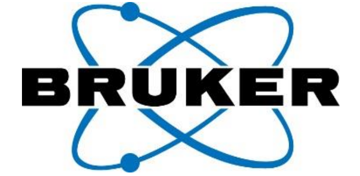




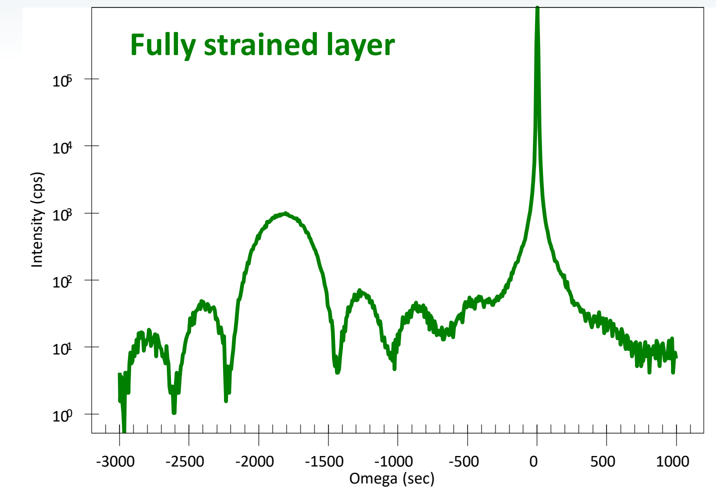


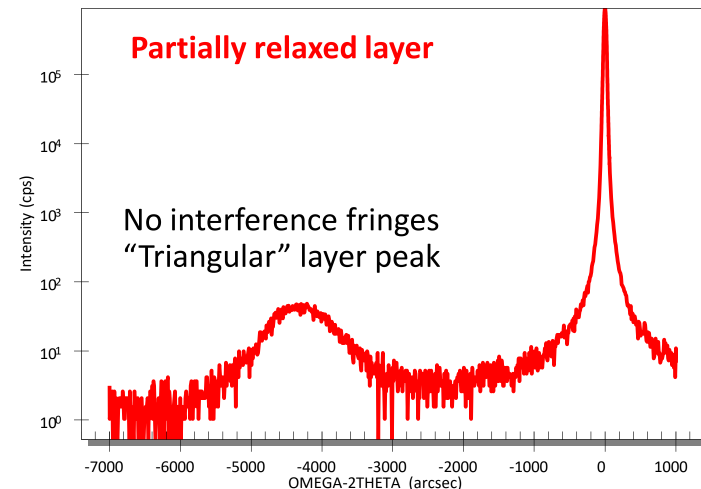


Comparison of HRXRD data from strained and relaxed SiGe epilayers

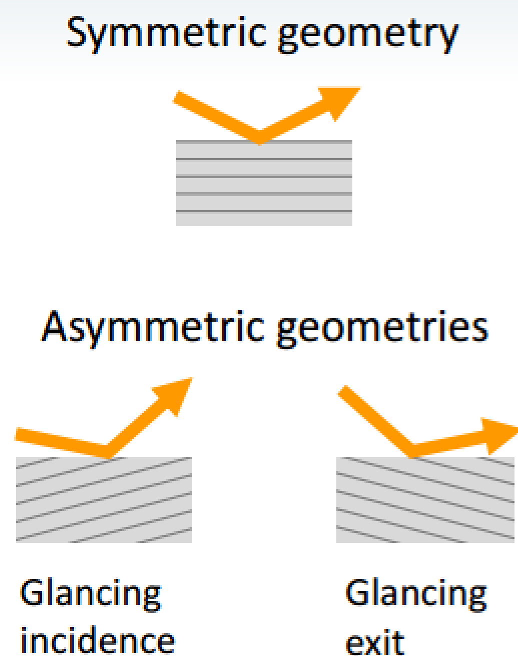


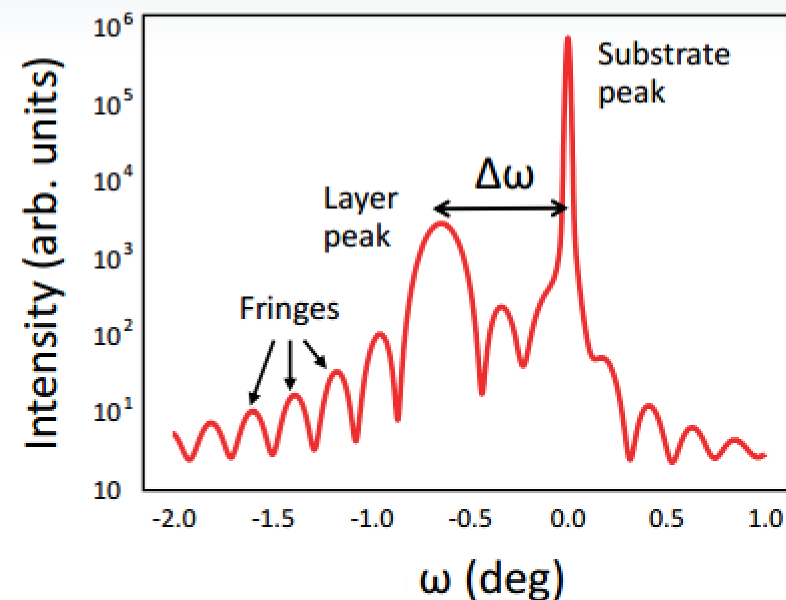
- Degradation of device performance and yield loss
  - Relaxed material has about 50% less strain than a pseudomorphic layer
  - Relaxed material will contain dislocations at the interface and in the layer - increased leakage?
- HRXRD provides a unique, automated solution for strain metrology and assessment of lattice defectivity





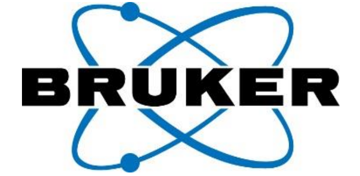
Symmetric and asymmetric geometry





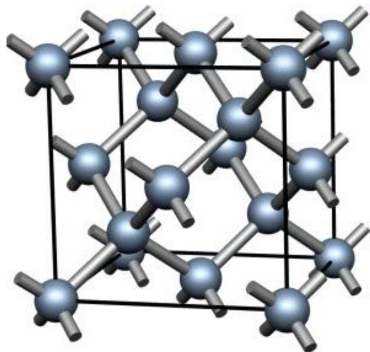
- Symmetric Bragg geometry is sensitive to lattice parameter perpendicular to the surface
- Asymmetric geometries are also sensitive to the lattice parameters both parallel and perpendicular to the surface

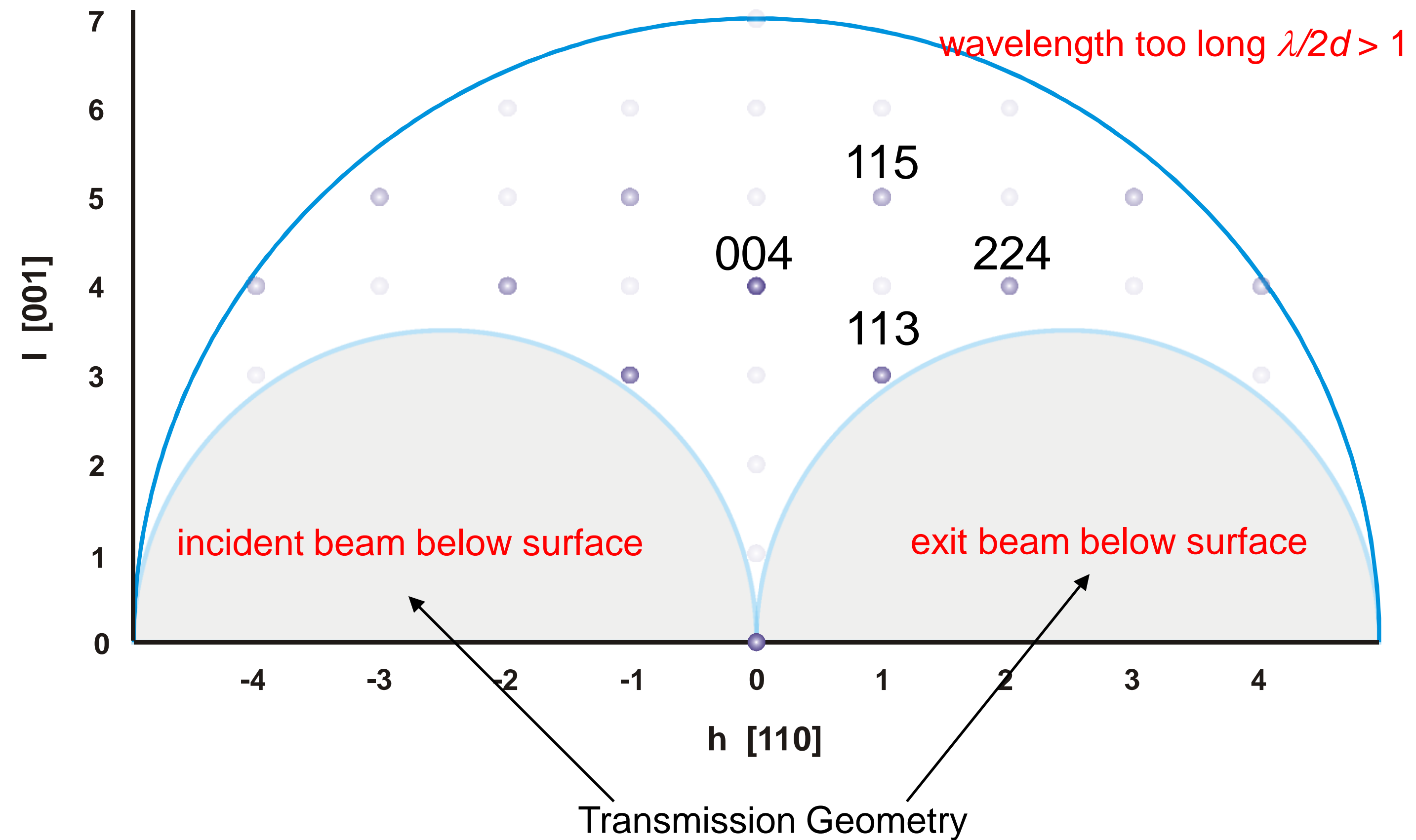
A silicon cystal in reciprocal space



- Diffraction planes projected as points in reciprocal space, intensity depends on incident beam scattering

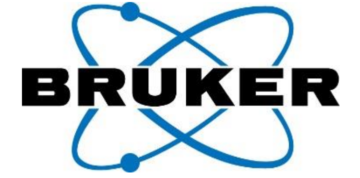
FCC-lattice with
Si atoms at
(0, 0, 0) and
(¼, ¼, ¼)



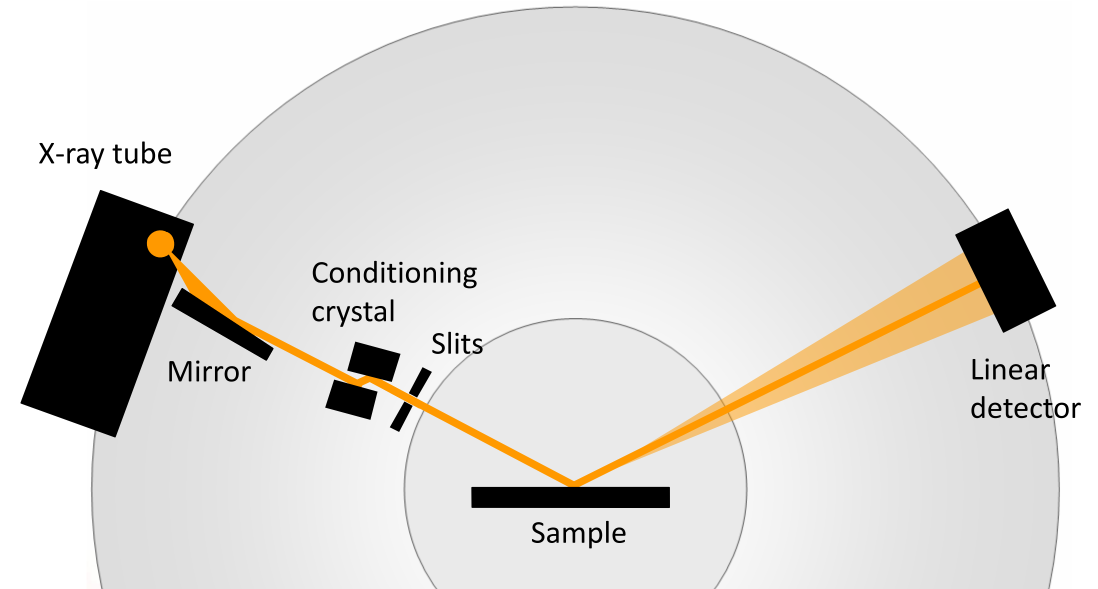


Transmission Geometry

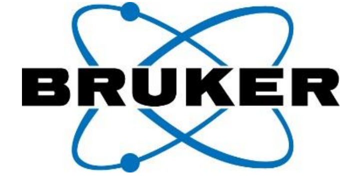
Fast reciprocal space mapping



- Linear (1D) or area (2D) detector replaces analyzer crystal / slits and point (0D) detector and allows routine RSMs to be measured in the fab
  - Simultaneously intensity acquisition over a large range of 2θ angles
  - x10-100 faster than conventional approach (minutes not hours)
- Provides more information than available by single HRXRD curves
- Automated RSM analysis for epi. process development and control of thin-films and patterned nanostructures

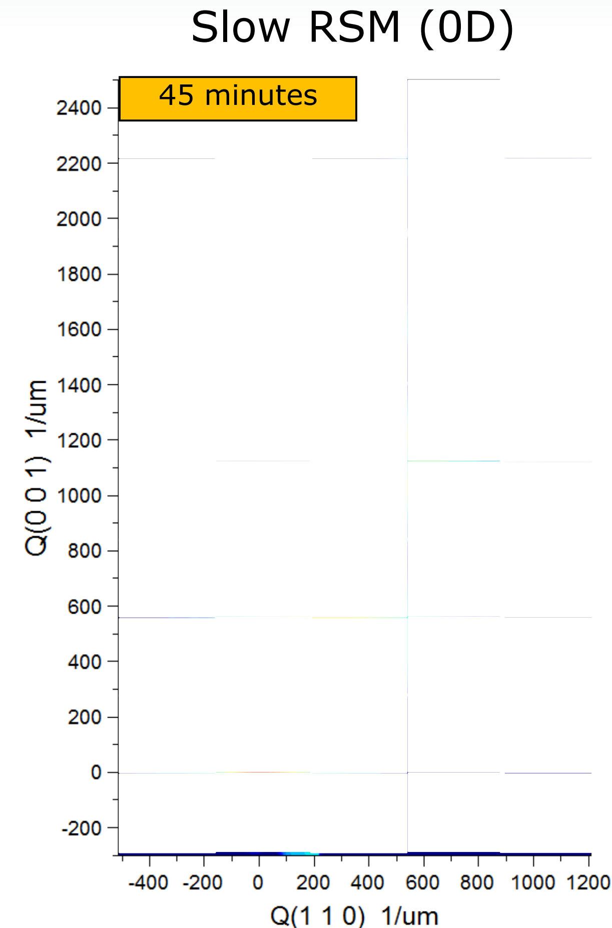


Fast RSMs using a 1D Detector

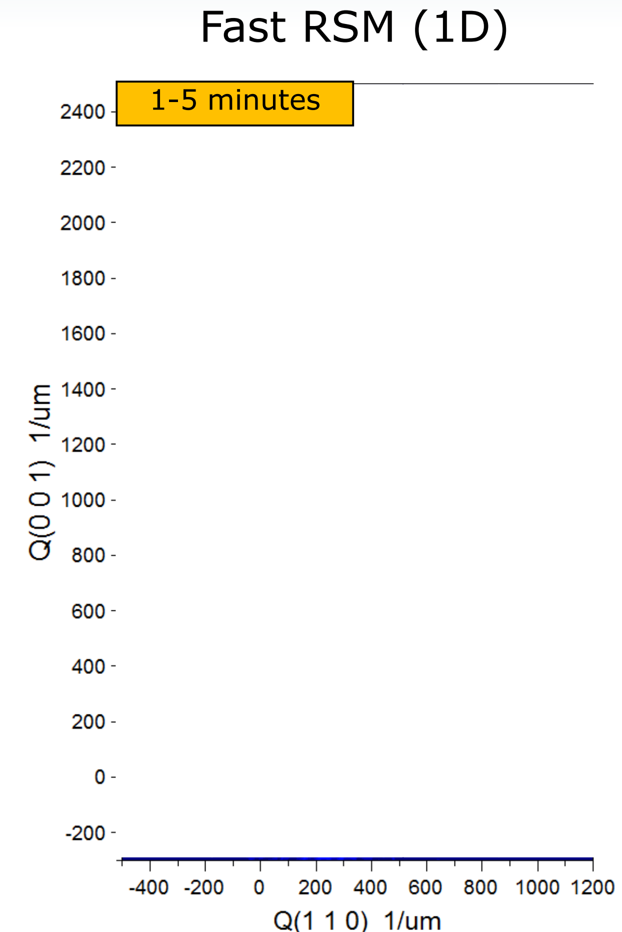


- Bruker has implemented a 1D detector which can measure RSMs in a few minutes
- 1D mode effectively captures a whole 0D line scan at once making RSMs much faster and better quality
  - Many pixels gives finer data
  - Lower noise floor at same throughput

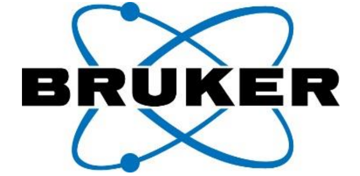
Slow RSM (0D)



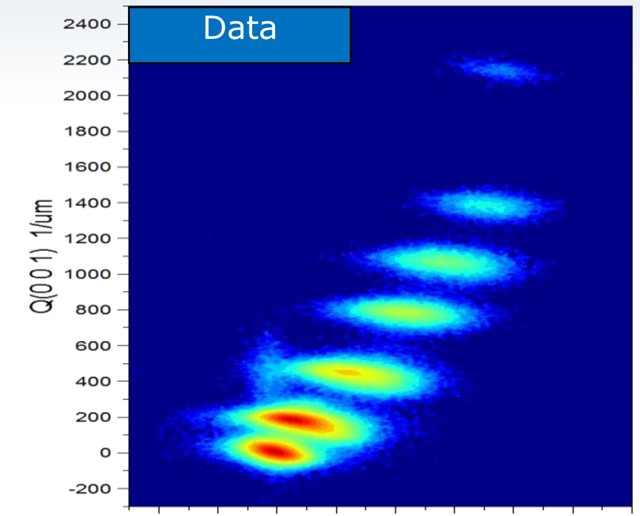
Fast RSM (1D)

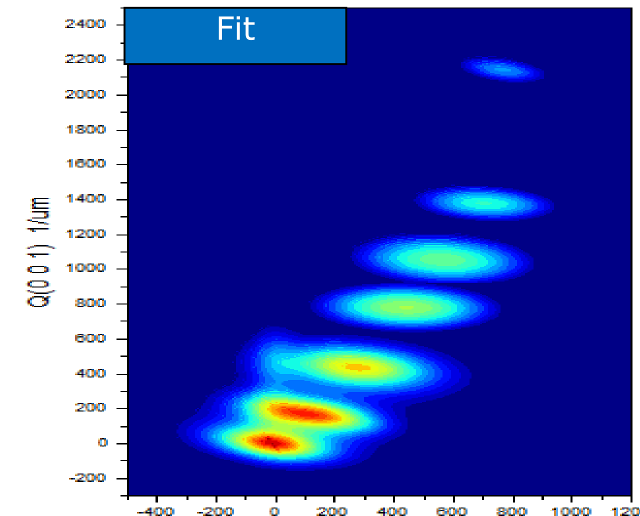


Automated RSM Analysis



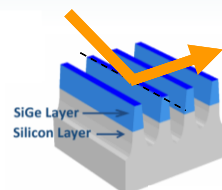
- Automatic fitting of RSMs is possible on Bruker tools
- Define a model in recipe
- Fitting and reporting of results fully automated

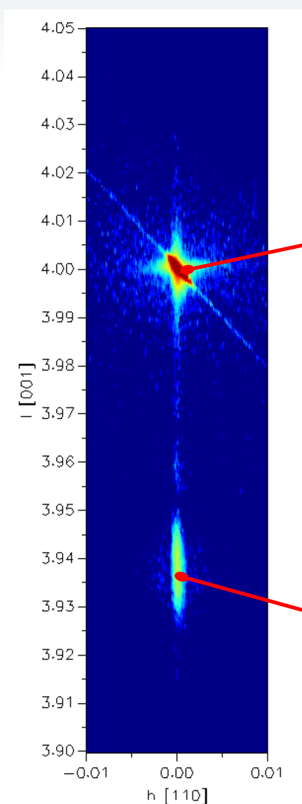


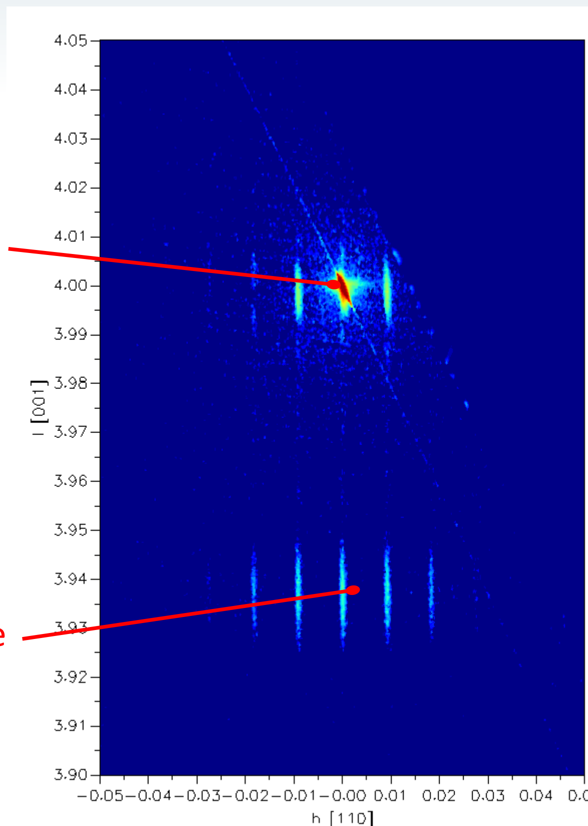


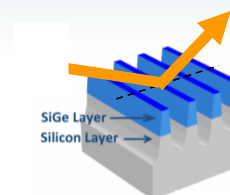
SiGe fins etched a from blanket layer

RSMs from epitaxial SiGe fins
Symmetric 004 reflection



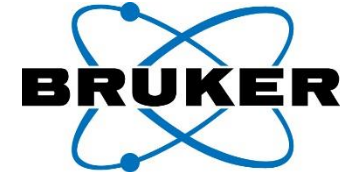






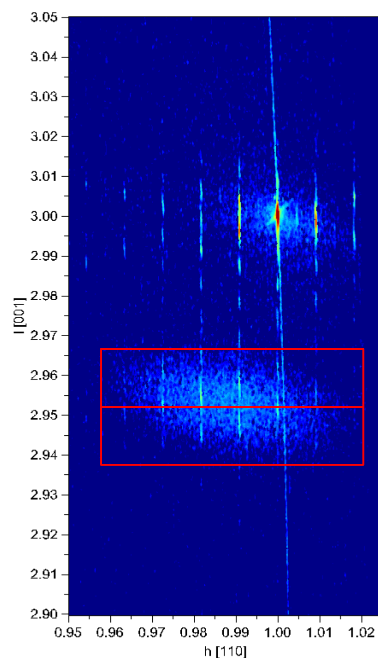
- H-spacing gives the pitch, $P = 42$ nm
- Components of the strain tensor can be determined from intensity envelopes by measuring asymmetric reflection at different azimuths

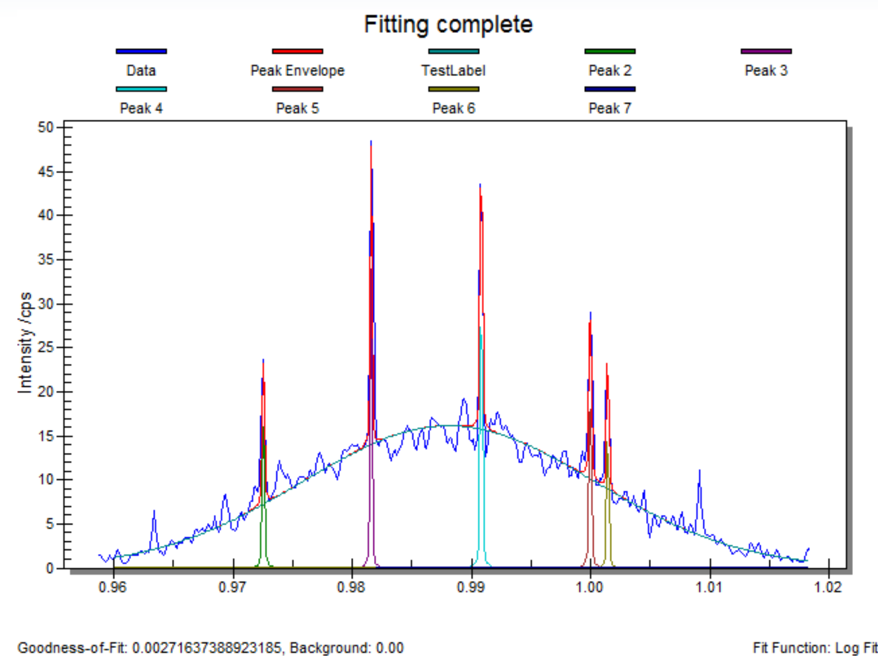
RSMs from epitaxial SiGe fins
Asymmetric 113ge reflection



- SiGe in a uniaxial stress state, cf. biaxial stress state for thin-films
  - Elastic relaxation perpendicular to the line direction
- Composition and thickness determined from fitting, x = 25%, t = 39.4 nm

Crystalline defectivity from RSMs

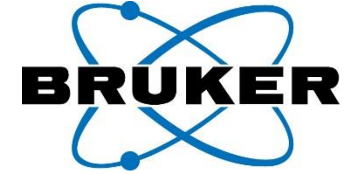




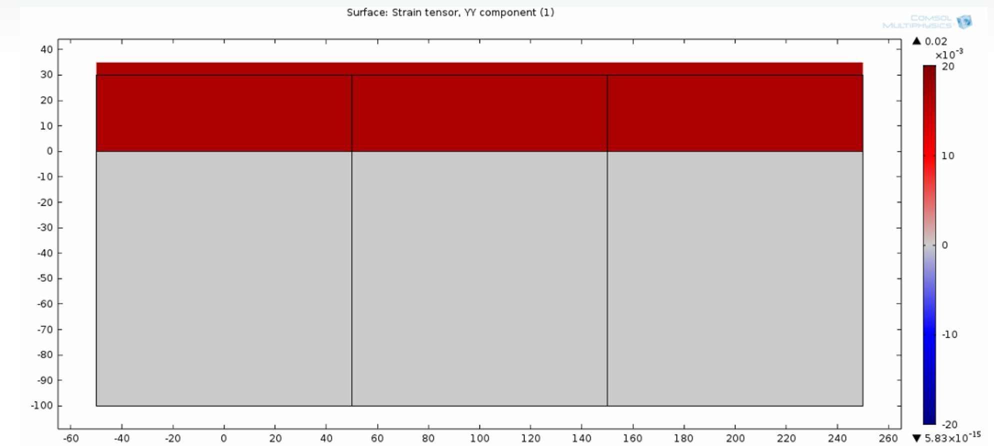
- Sharp peaks (coherent scatter) are from high crystalline quality material
- Broad peaks (diffuse scatter) is due to crystalline defectivity
- Ratio of the peak areas can be used to monitor defectivity in patterned structures

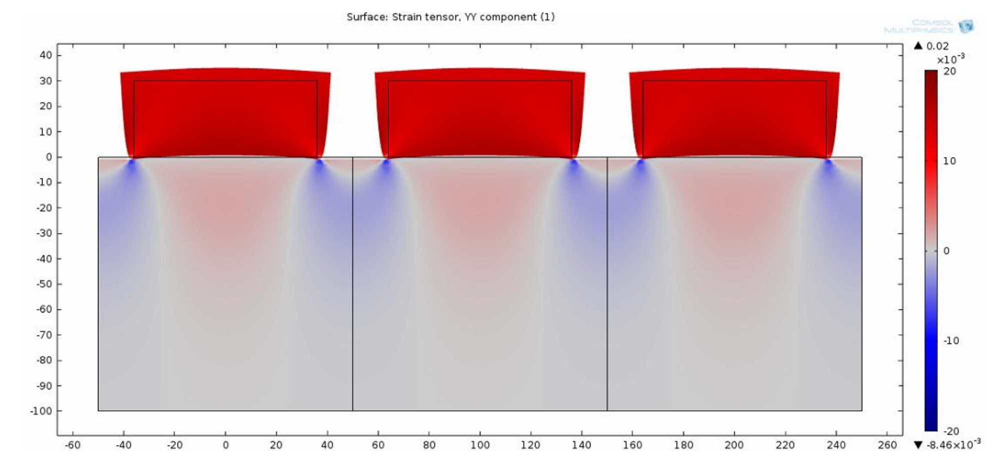
Selectively grown Ge/SiGe fins

Patterned epitaxial nanostructures



- In blanket epitaxy you have simple biaxial stress
  - Blanket pads are less relevant and / or no longer available
- In epitaxial nanostructures you have
  - Micro-loading effects in selective growth
  - Stress-state is far more complex, i.e. elastic relaxation of the epi and distortion of the substrate lattice





Ge/SiGe fins

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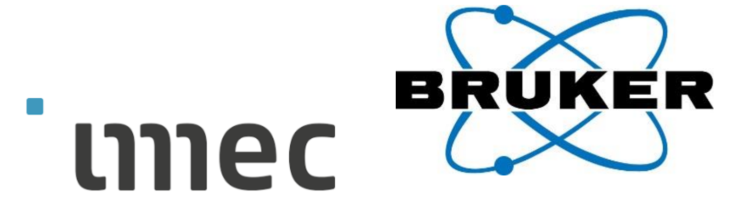
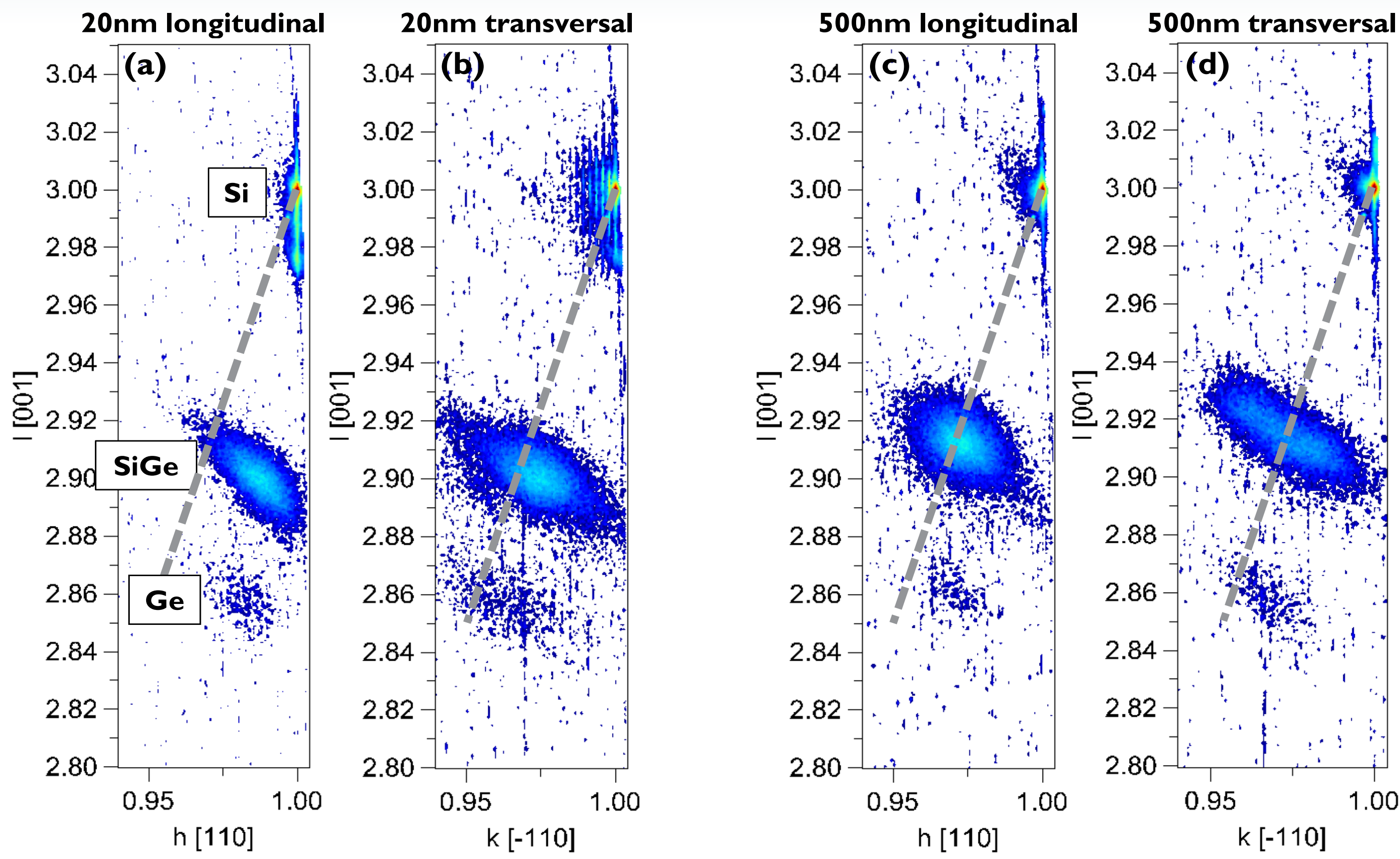
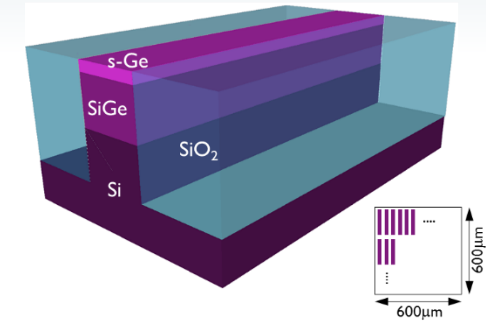
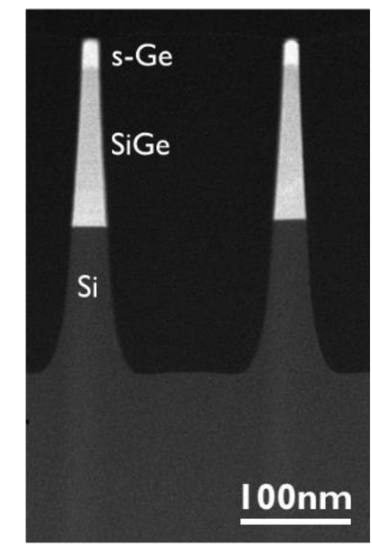
- Compressive sGe can provide higher mobility than bulk Si for pFETs
- Two integration schemes for creating sGe have been studied
  - Etching of thin, blanket Ge layer grown atop a thick blanket SiGe strain relaxed buffer (SRB) a few microns thickness to reduce the misfit dislocation density at the top of the SRB
  - Selective growth of thin Ge on a relaxed SiGe buffer in narrow trenches patterned in STI. Extended defects are trapped by Aspect Ratio trapping (ART) mechanism and terminate at the STI sidewalls
- Selective growth scheme is favored for CMOS
  - Allows co-integration with Si or III-V nFETs required for CMOS

Asymmetric RSMs (113ge reflection) of selectively grown Ge/SiGe fins





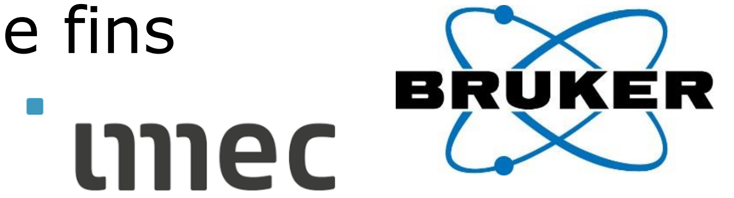


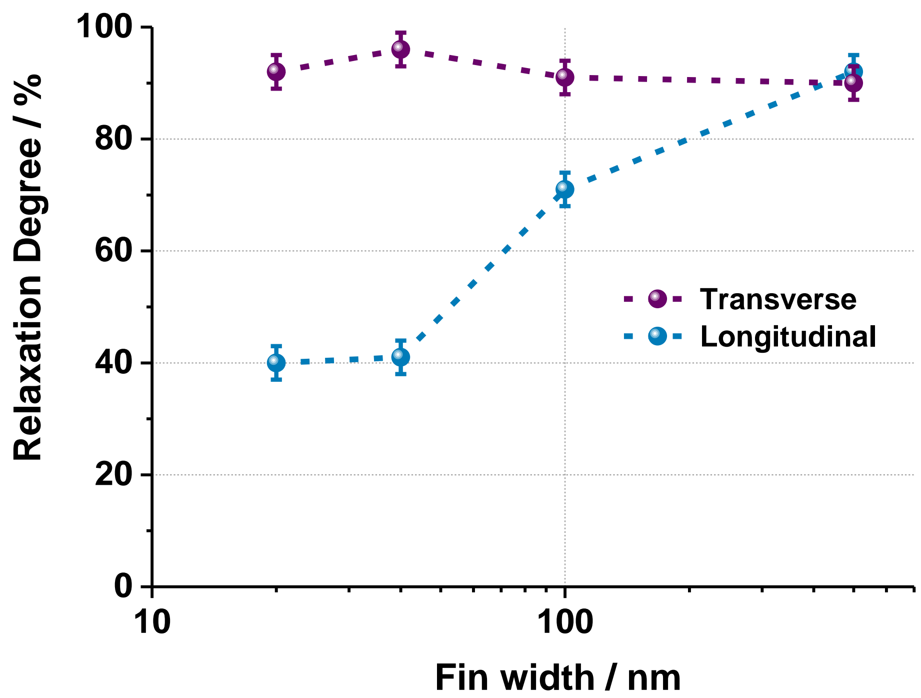


Schematic and STEM image of selectively grown Ge/SiGe fins

A. Schulze et al, Nanotechnology 28 (2017), 145703
doi.org/10.1088/1361-6528/aa5fbb

Asymmetric relaxation in selectively grown Ge/SiGe fins





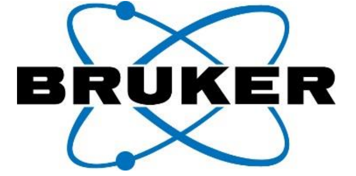
$$\text{Relaxation}_{\text{SiGe}} = \frac{a_{SiGe} - a_{Si}}{a_0 - a_{Si}}$$

A. Schulze et al, Nanotechnology 28 (2017), 145703
doi.org/10.1088/1361-6528/aa5fbb

- Fin width limits the plastic relaxation in the Longitudinal direction
  - For example, SiGe only 40% relaxed in the longitudinal direction for 20 nm wide fins
- Reduced probability for gliding of dislocation half-loops due to spatial confinement in narrow fins
  - Fewer misfits running perpendicular to the STI trench

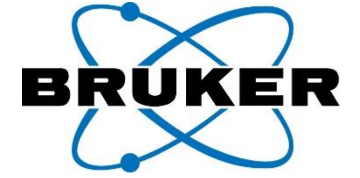
SiGe/Si for nanowire / nanosheet FETs

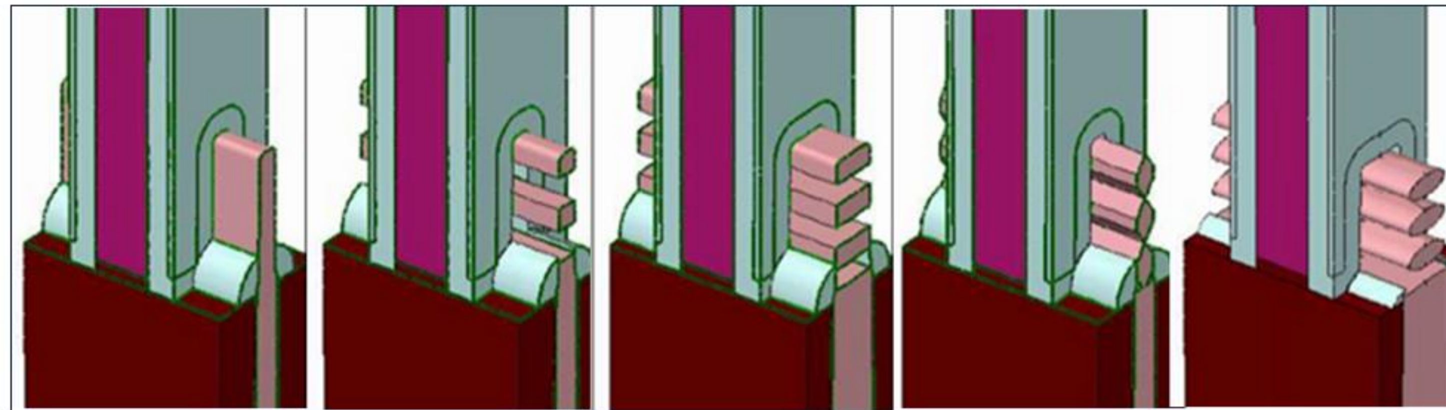
What device architecture comes after finFETs?



- New architecture after finFETs will likely be needed below 7 nm node
- Gate-all-around (GAA) architectures seem to be the most likely at this time
  - Further improves electrostatic control and reduces short channel effects by wrapping the gate completely around the channel
  - Shares many of the same process steps, materials and tools as finFETs
- Scaled finFETs incorporating sGe and III-V high-mobility channel materials are also being investigated
- Regardless, process complexity and costs will continue to escalate
- HRXRD is used for both R&D and production control of advanced logic technology
  - Composition and strain metrology

Types of horizontal gate-all-around architectures





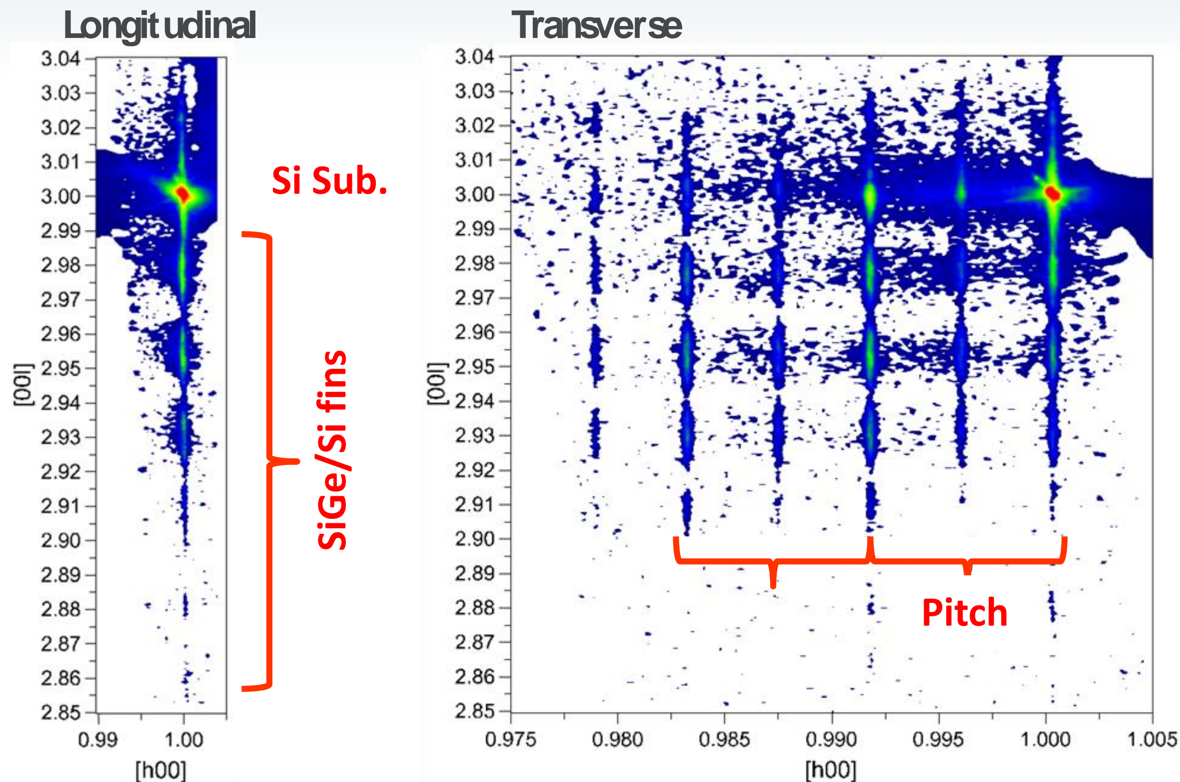
Ref: S.C. Song, Qualcomm; V. Moroz, Synopsys

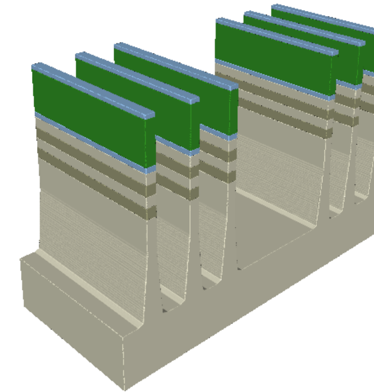
Traditional FinFET	Round/Square Wire	Horizontal Nanoslab/sheet/ multi-bridge channel	Hexagonal Nanowire	Nano-Ring
Three control surfaces	Four/All Around Control Surfaces Per Channel			

- Gate-All-Around (GAA) architecture provides better electrostatic control than FinFETs for sub 7 nm nodes
- Device performance is a function of the width of the wires/sheets
- Stacked GAA devices are needed to recover the loss in active width in moving to GAA

M. Lapedus, «What’s after FinFETs», (2017)
https://semiengineering.com/whats-after-finfets/

Strain in Si/SiGe fins after patterning

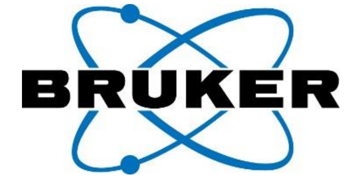




A. Schulze el al, Physica Status Solidi c, 14 (2017) 1700156.
doi:10.1002/pssc.201700156

- Asymmetric RSMs clearly show uniaxial stress in fins after patterning
  - Fully strained along the fins (longitudinal direction)
  - Elastically relaxed across the fins (transverse direction)

Monitoring strain after STI Process



After Fin Etch | After NEW STI | After OLD STI

[00l] vs [h00] reciprocal space maps (L from 2.85 to 3.04; H 0.99–1.00)

Imec-AMAT JDP

- Shallow trench isolation (STI) process involves SiO_2 deposition and densification
- Compressive strain induced by STI
  - Peak shift towards smaller L values → increased out-of-plane lattice parameter
  - Pronounced peak next to substrate peak
- Fin oxidation due to STI process
  - Material loss (strong oxidation of SiGe, clearly visible in TEM)
  - Volume expansion (SiO_2:Si) → Compressive stress on fin

Stress-induced peak shift reduced by new STI process

A. Schulze el al, Physica Status Solidi c, 14 (2017) 1700156.
doi:10.1002/pssc.201700156

Conclusions

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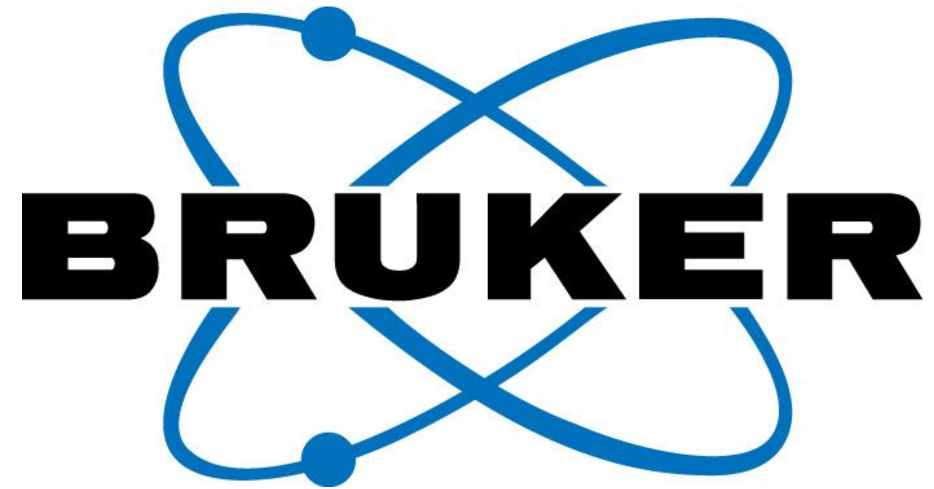
- High-resolution XRD delivers valuable information on epitaxial thin-films and arrays of nanostructures
  - Materials include: SiGe, Si:C(P), Ge and III-Vs for current and future technology nodes
  - Parameters (depending on sample) include: strain / stress components, composition, thickness, pitch, pitch-walk, crystalline quality…
- Complements traditional techniques such as SE / scatterometry and SEM / TEM
- The latest generation of lab / fab tools can yield good quality data in minutes not several hours
  - From patterned wafers with a 50 µm spot-size
  - Including reciprocal space mapping using linear detectors
- In-line X-ray metrology tools, enable materials and process development and production monitoring for advanced logic and other applications



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