ADVANCED MICROELECTRONICS ROADMAP AND SUBSEQUENT METROLOGY CHALLENGES

M. Vinet, F. Andrieu, E. Nowak, C. Reita and N. Gambacorti

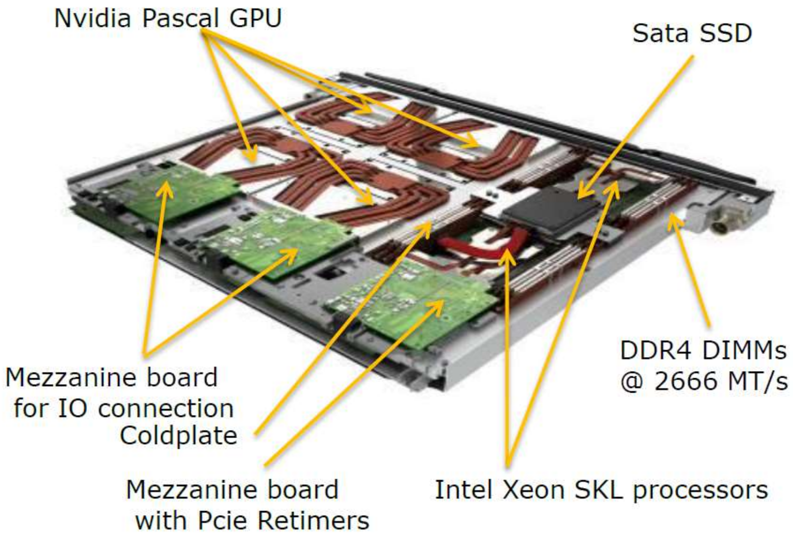
Context

Era of data deluge, 2010 the Economist

Functions and Constraints

Fundamental functions

- Compute
- Store
- Transmit



Bull sequana X1125 GPU blade

Constraint

- Power
- Cost
- Performance
- Time to Market

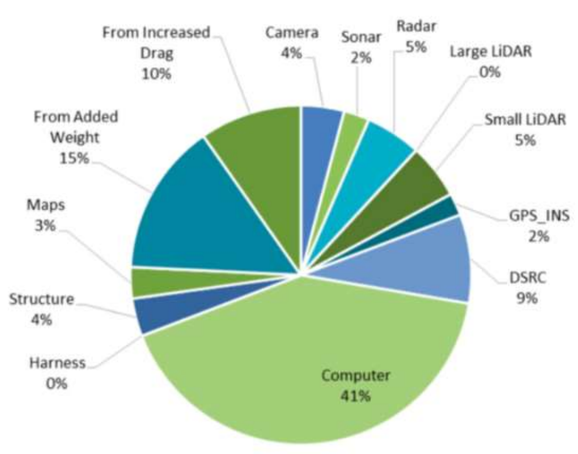
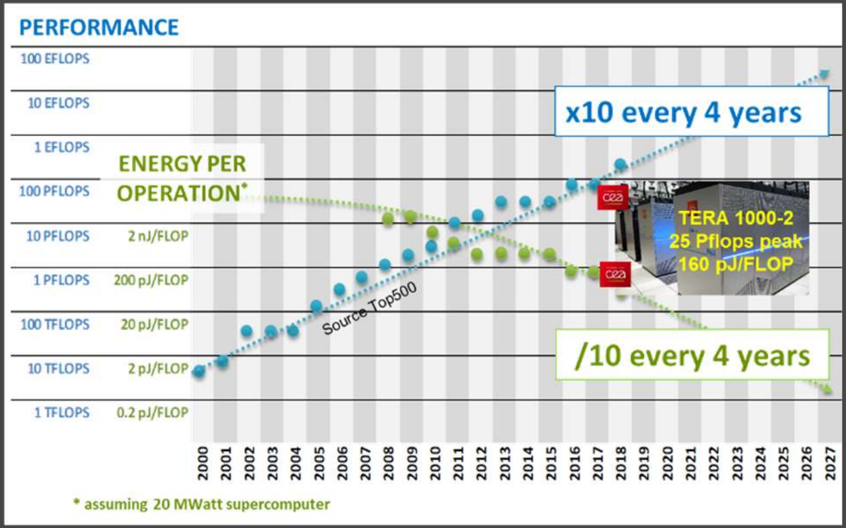


Image: University of Michigan

Sources of added energy consumption from Ford Fusion's autonomy system.



* assuming 20 MWatt supercomputer

Opportunities for alternative computing

Computing

Von Neumann

Heterogeneous computing

In memory computing

Quantum computing

Architecture

Multicore

3D heterogeneous integration

Photonic interconnects

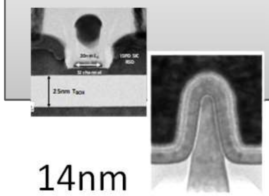
In memory computing

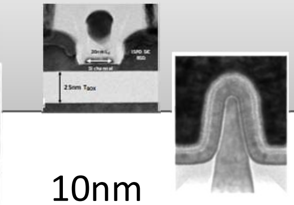
Circuit

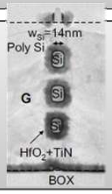
Power management

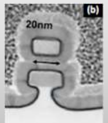
Standard cells height scaling

CMOS









14nm 10nm 7nm 5nm 3nm

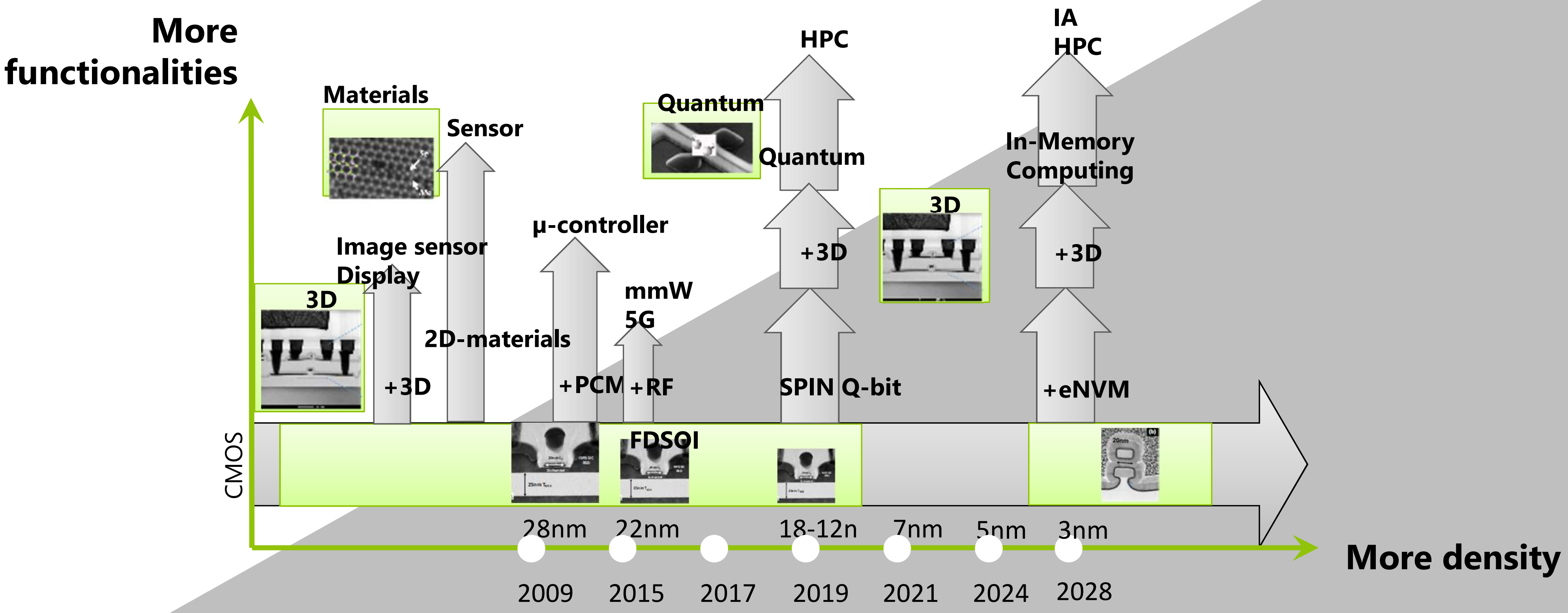
2014 2016 2018 2020 2022 Year of 1st introduction

Artificial intelligence

Low Power

HPC

Advanced CMOS roadmap



More functionalities

Materials
Sensor
Image sensor
Display
3D
+3D
2D-materials
µ-controller
+PCM
mmW
5G
+RF
Quantum
HPC
Quantum
+3D
SPIN Q-bit
3D
IA
HPC
In-Memory Computing
+3D
+eNVM

CMOS
FDSOI

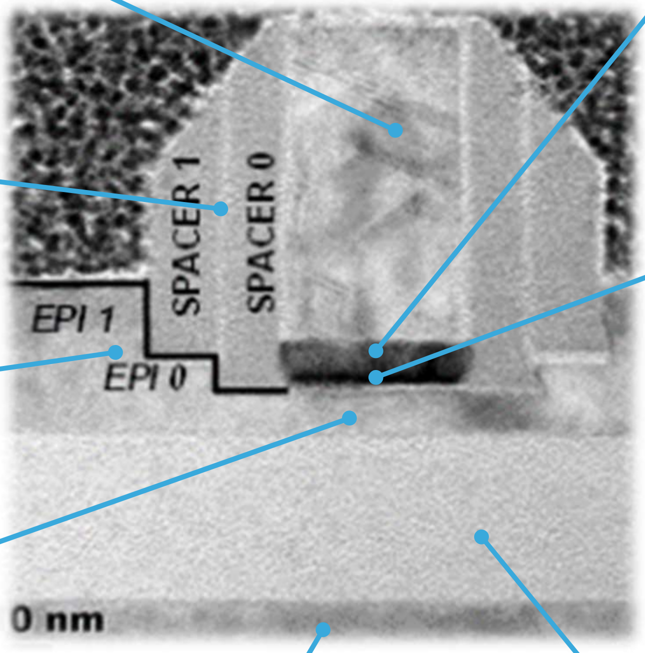
28nm
22nm
18-12n
7nm
5nm
3nm

2009
2015
2017
2019
2021
2024
2028

More density

Diversification of the roadmaps to fulfil many applications with high potential benefits

28FDSOI at a glance



Silicided Polysilicon (50nm)

Metal Gate (6.5nm TiN)

Double Spacers (20nm)

HK dielectric (1.8nm)

Double raised SD (22nm)

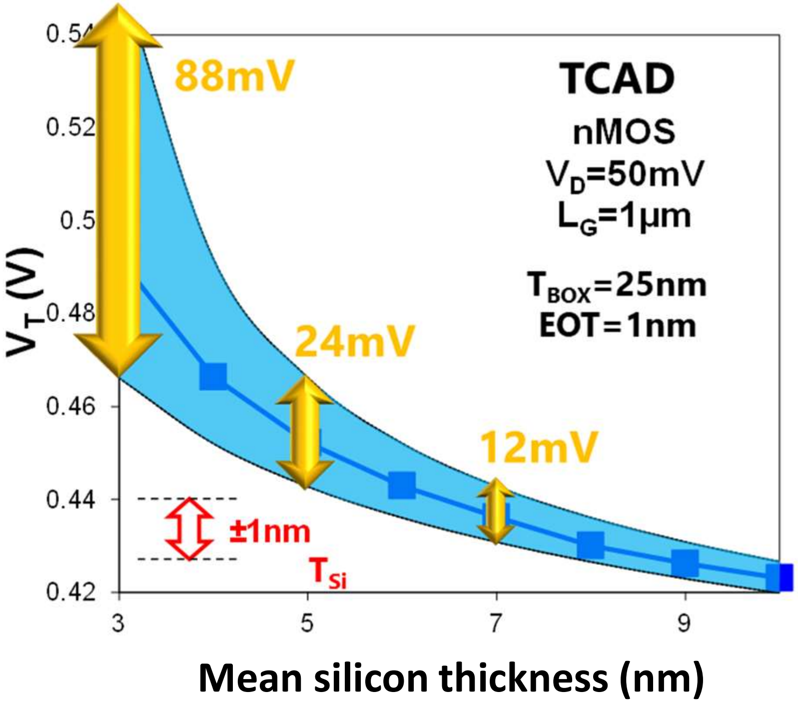
Thin Si film (7nm)

Handle substrate <100>

Thin buried oxide (25nm)

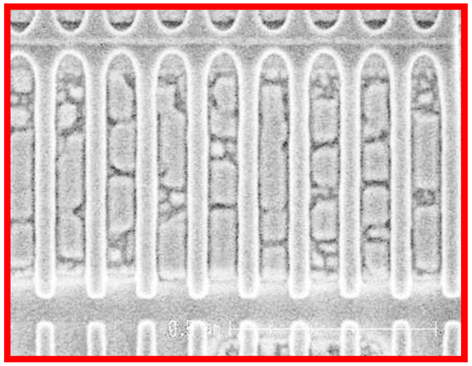
Need for accurate thickness measurements

- For performance motivation
  - Vt does depend on Tsi
  - To control variability

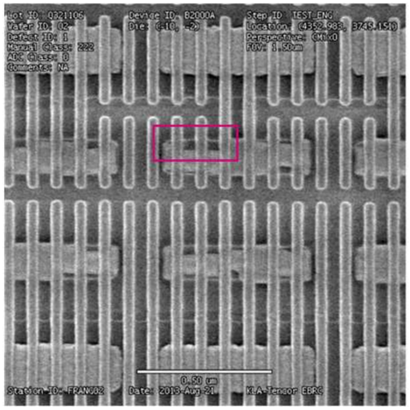


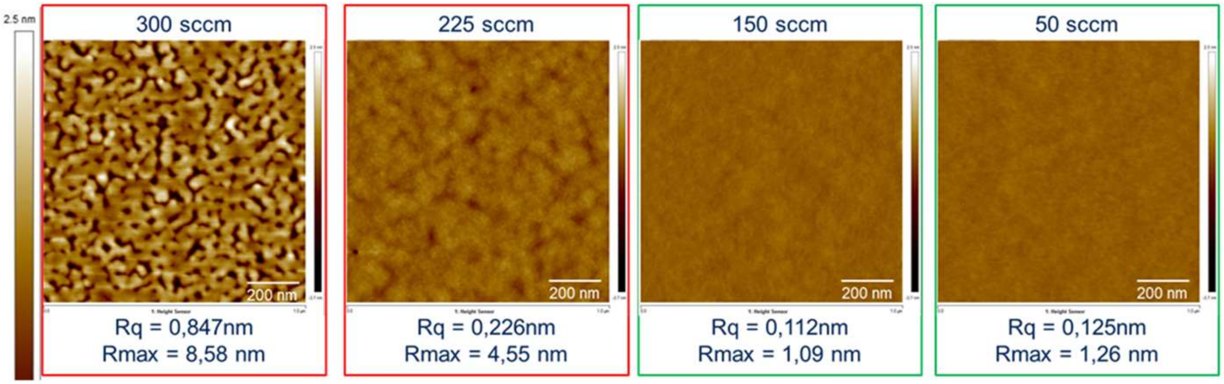
Need for accurate thickness measurements

- For integration motivation
  - To enlarge epitaxy process window

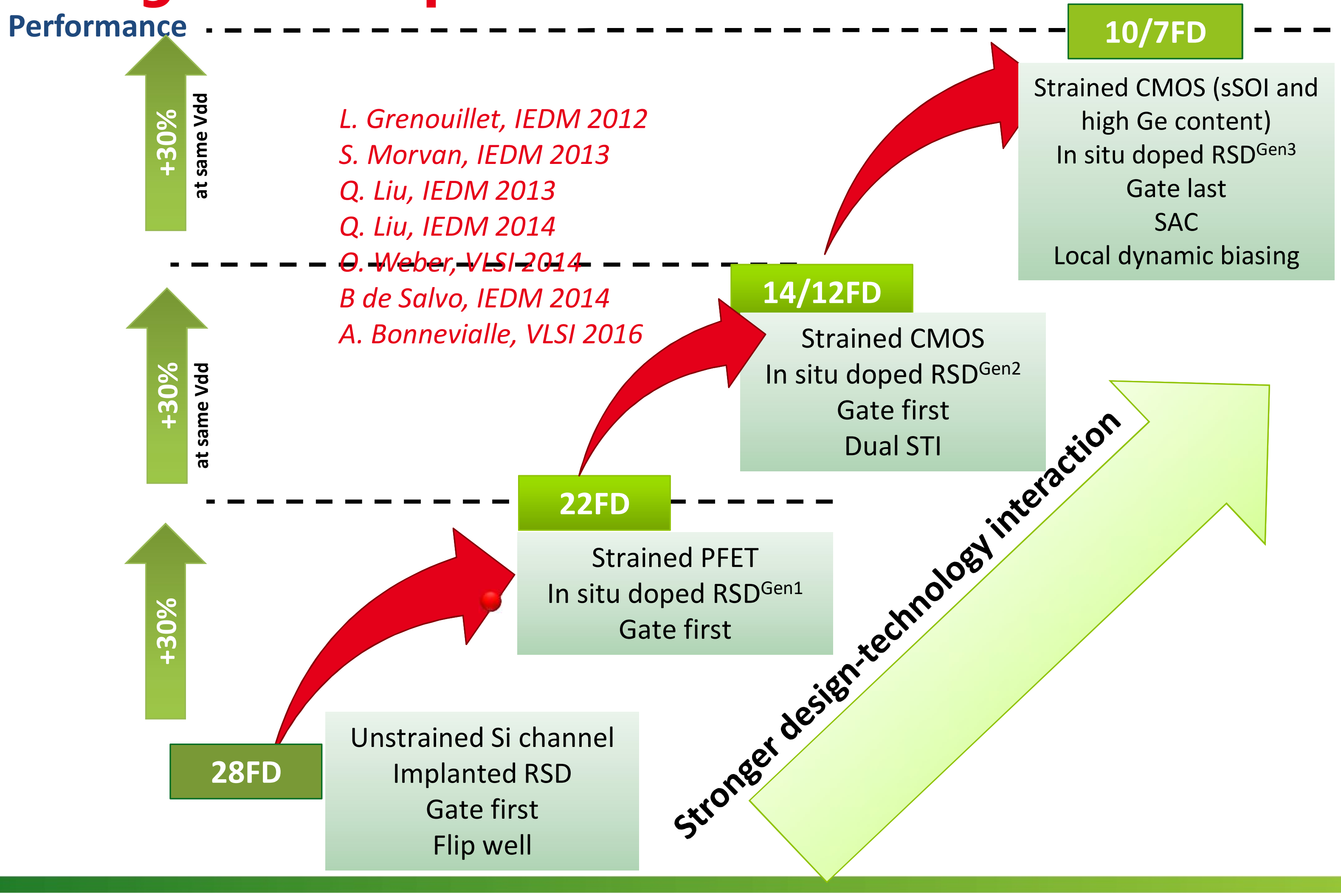


And surface quality/composition





Scaling Roadmap



L. Grenouillet, IEDM 2012
S. Morvan, IEDM 2013
Q. Liu, IEDM 2013
Q. Liu, IEDM 2014
O. Weber, VLSI 2014
B de Salvo, IEDM 2014
A. Bonnevialle, VLSI 2016

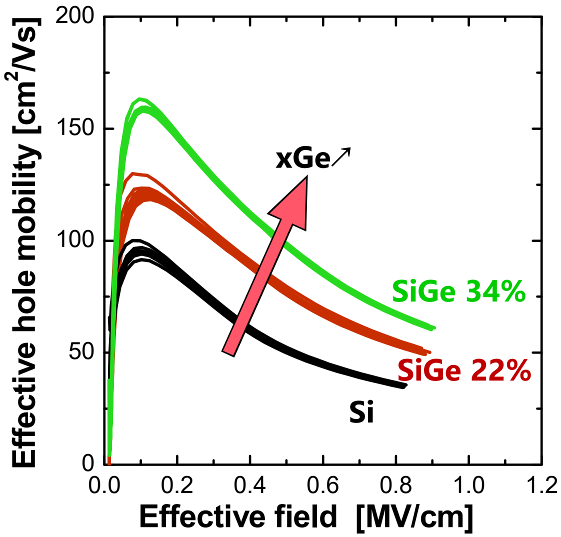
28FD
Unstrained Si channel
Implanted RSD
Gate first
Flip well

22FD
Strained PFET
In situ doped RSD^{Gen1}
Gate first

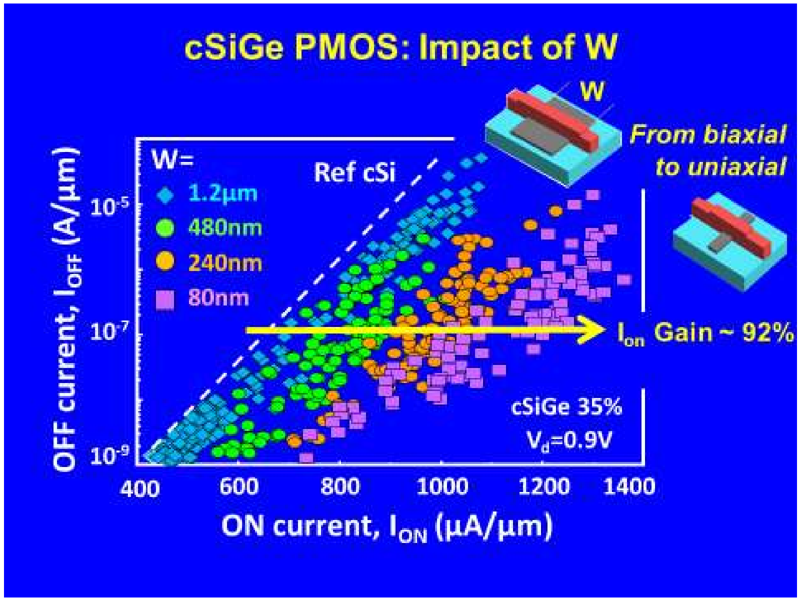
14/12FD
Strained CMOS
In situ doped RSD^{Gen2}
Gate first
Dual STI

10/7FD
Strained CMOS (sSOI and high Ge content)
In situ doped RSD^{Gen3}
Gate last
SAC
Local dynamic biasing

SiGe channel improves performance



K.Cheng et al., IEDM'12

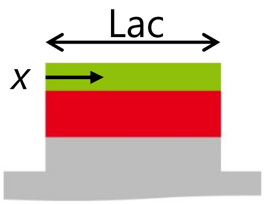


B De Salvo et al., IEDM'14

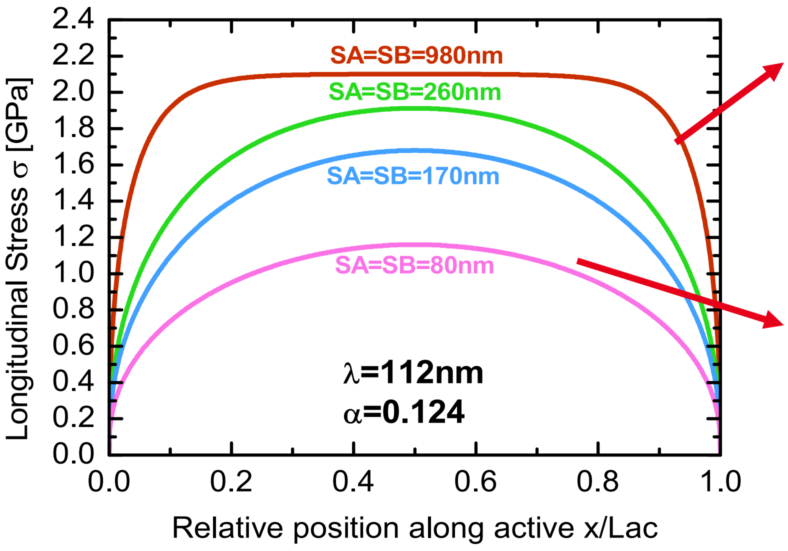
- Compressive stress from SiGe channel brings mobility gain
- Performance boost strongly depends on strain configuration

Stress Relaxation and Layout effects

Model of stress according to position along active area



$$\sigma(x, Lac) = \sigma_0 \left[\frac{1}{2}\left(\left(1 - \exp\left(-\frac{x}{\lambda}\right)\right)^{\alpha} + \left(1 - \exp\left(\frac{Lac - x}{\lambda}\right)\right)^{\alpha}\right)\right]^{1/\alpha}$$

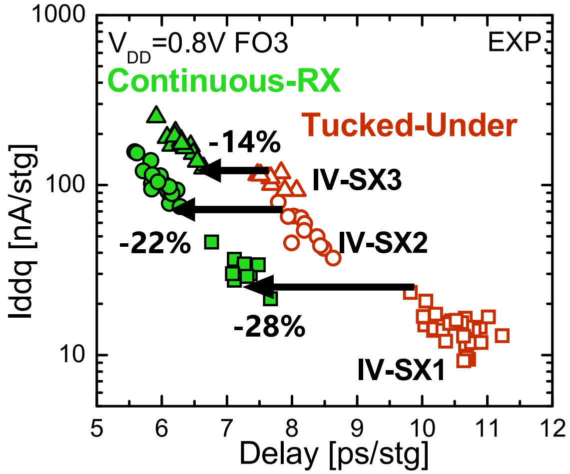


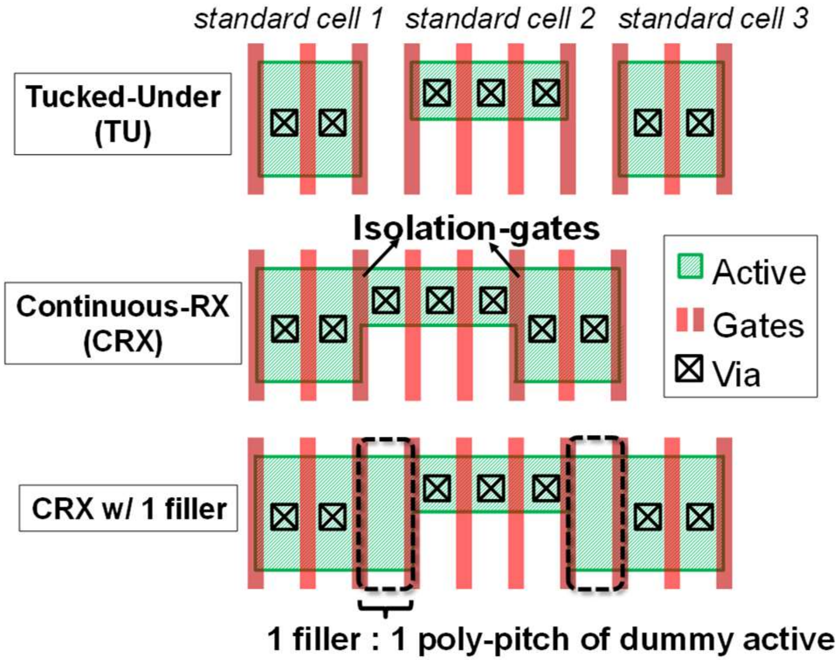
Stress relaxation on active area edges

Edge effects impact the whole active area when dimensions are reduced

R. Berthelon, F. Andrieu et al., EUROSOI'16

Design technology co-optimization



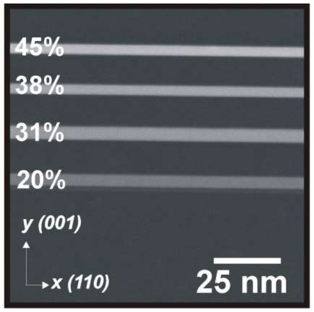


Continuous-RX designs is an optimimum for the W and SA/SB effects

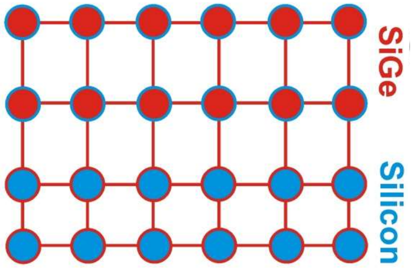
R. Berthelon, F. Andrieu et al., VLSI'16

Need for accurate strain measurements

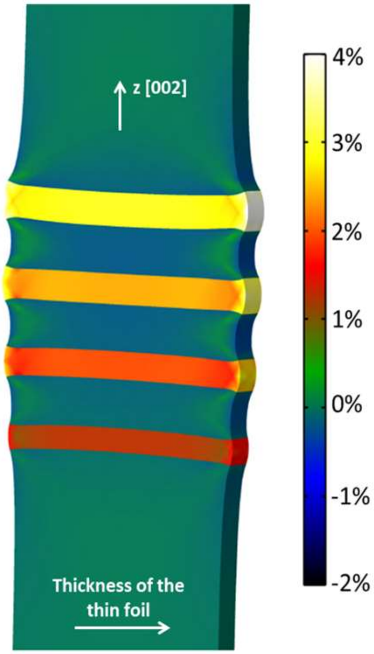
Use of PED for precise strain characterization

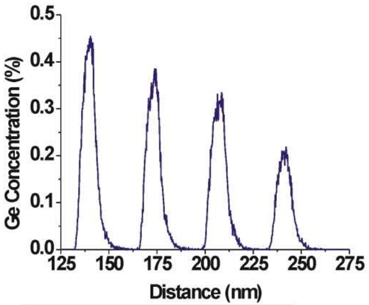


TEM Overview

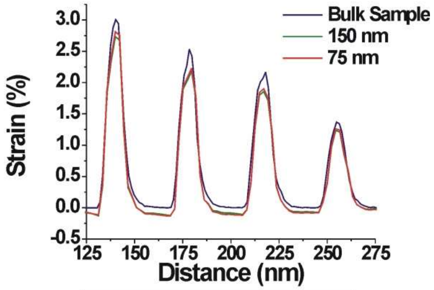


Schematic





SIMS Profiles

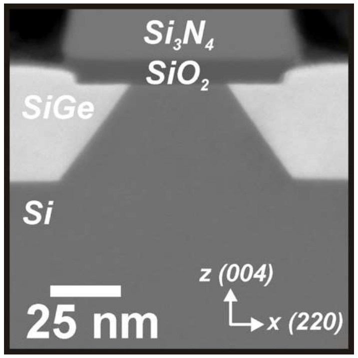


Simulations

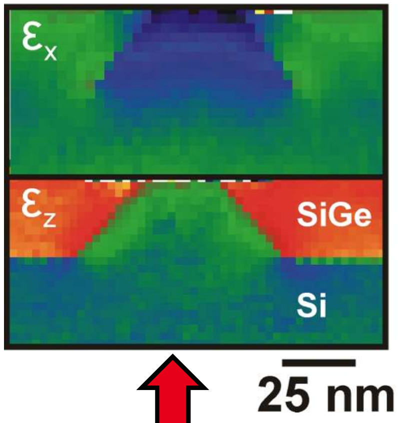
D Cooper, V Delaye *et al*

Apply precession to SiGe test device

HAADF STEM

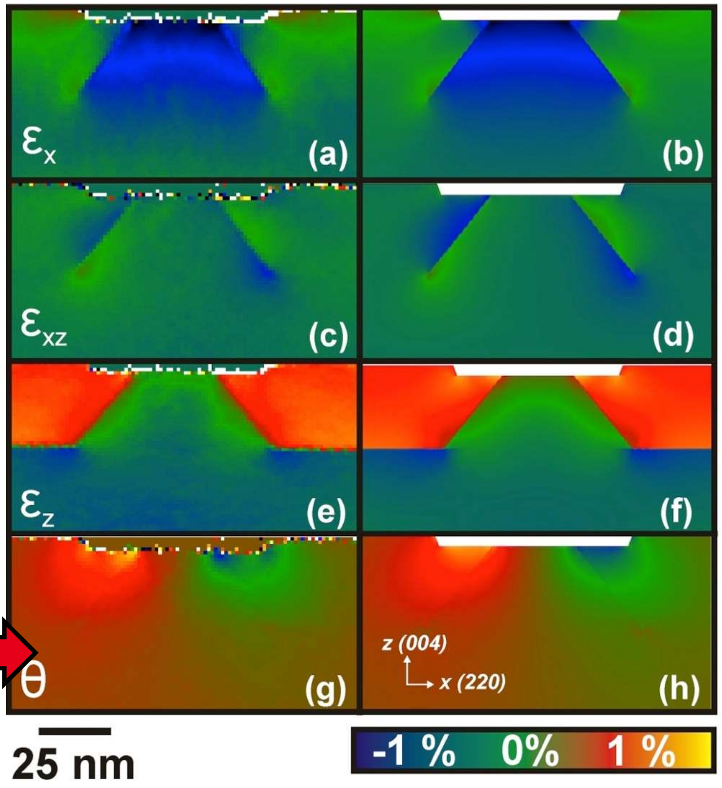


Fast Precession



Detailed Precession

Simulations



Maps formed using 800 diffraction patterns acquired quickly at using low CCD resolution. Less than 10 minutes acquisition and 30 seconds data processing.

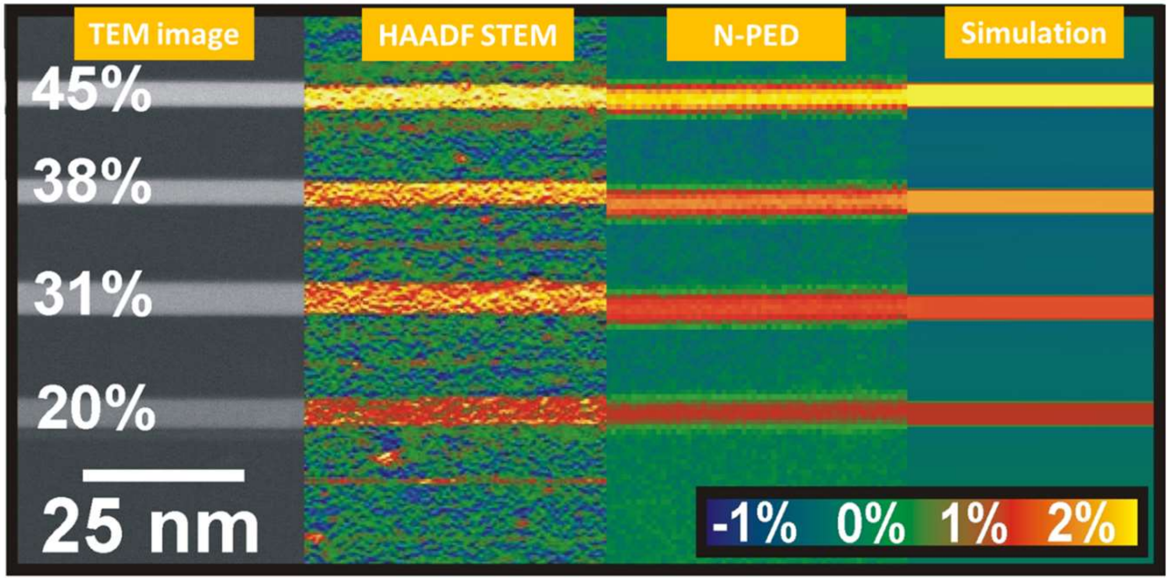
Maps formed using 5000 diffraction patterns, requires one hour acquisition and then one hour data processing.

Developments of acquisition in 2016 have sped up the acquisition to 10 patterns per second.

Cooper et al. Nano Letters. *15*, 5289–5294 (2015)

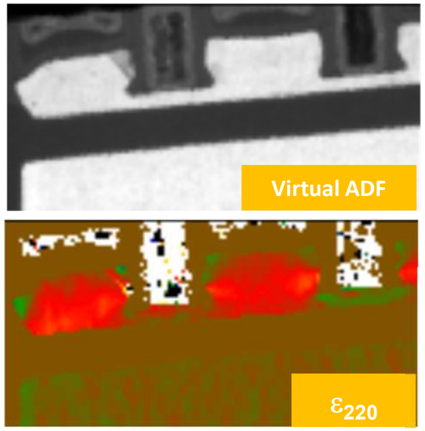
Need for accurate strain measurements

- ☐ Both STEM-HAADF and N-PED results are in good agreement with simulations
- ☐ Much more noise in the strain profile measured by STEM-HAADF

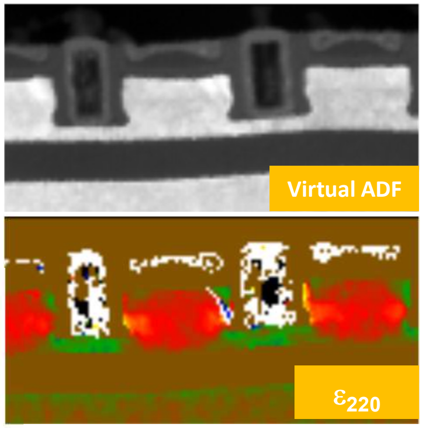


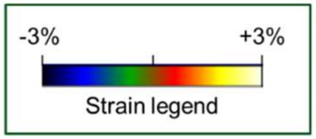
Strain mapping vs STI distance

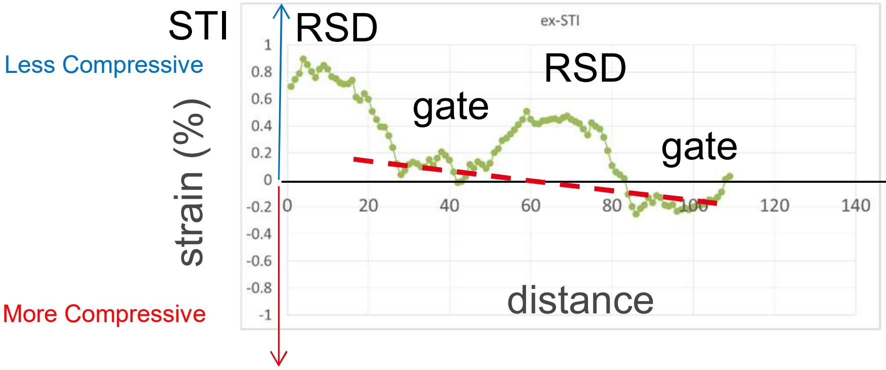
Strain relaxation on active edge

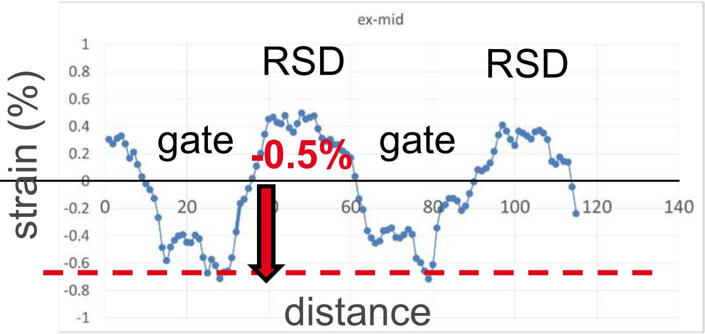


Continuous RX

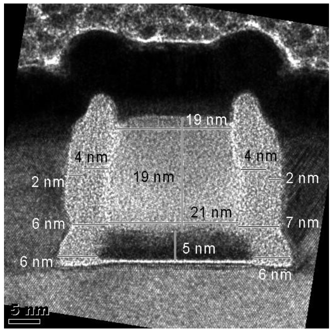




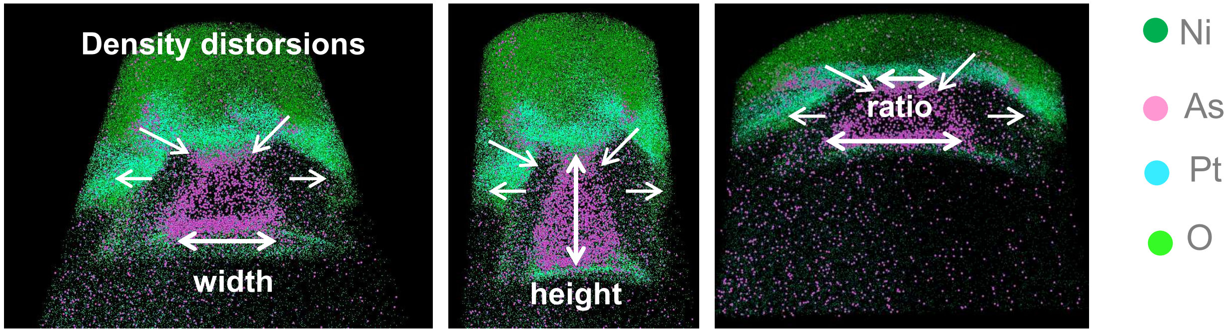




3D dopant mapping of PMOS device for 14 nm FDSOI technology

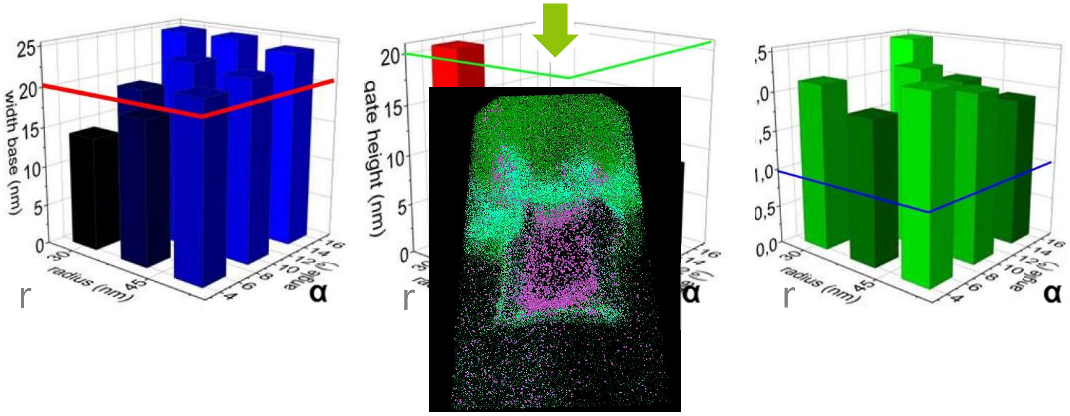


TEM image of the 14 nm PMOS device (NO-SOI)



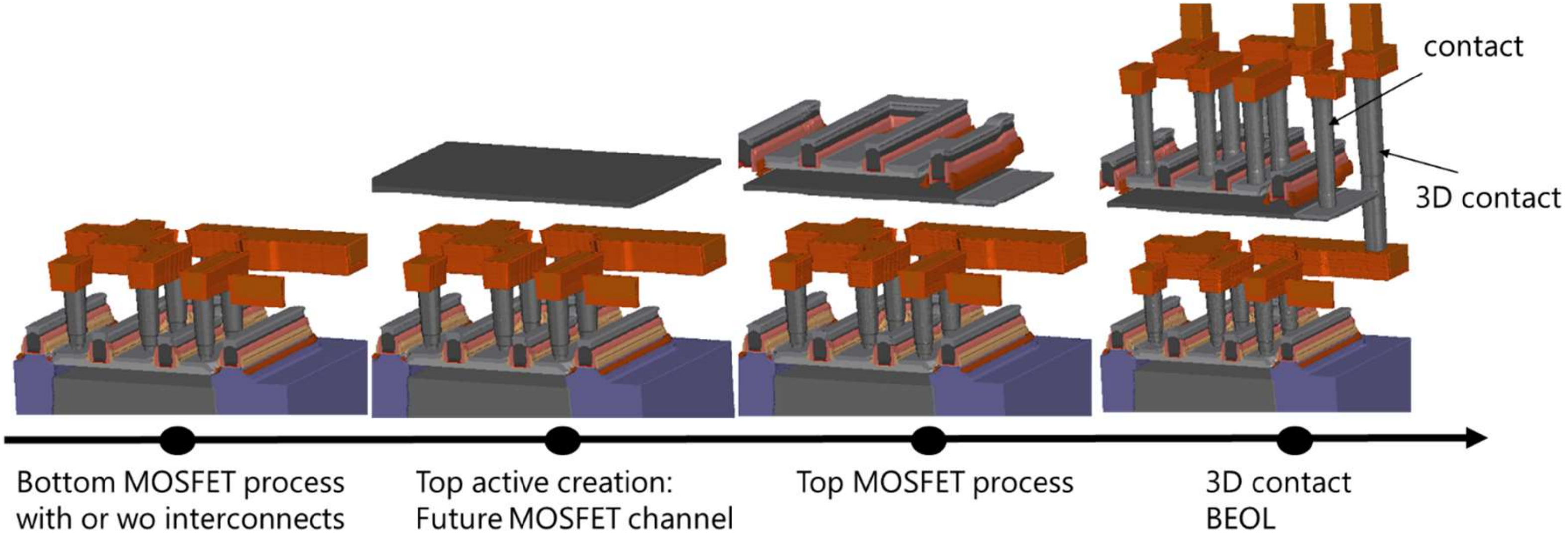
r: 30 nm α: 15° **r: 30 nm α: 5°** **r: 50 nm α: 5°**

1. Start with SEM/TEM dimensions.
2. Explore reconstruction space.
3. Density correction (real space relaxation).



r: 30 nm α: 5°

CoolCube^{TM} integration



ID card:

- Lithography alignment between layers (3σ<5nm)
- 3D contact = W plug scales with the device technology (@ 28nm diameter= 40nm)
- Thin active layer (10 to 100nm) (low C coupling)

Positioning of CoolCube™

More than Moore

System integration
More functionality
Power gain
Cost savings

Leti strategy

- Performance demonstration & technological modules development
  - FDSOI chosen as baseline for top layer
    - Low cost
    - IP portability (unlike junctionless)
    - Compatibility with analog and digital performance
- Wide range of applications scanning
- Ecosystem construction

Cost savings

More Moore

CoolCube^{TM} as a common platform

1 **Computing applications**

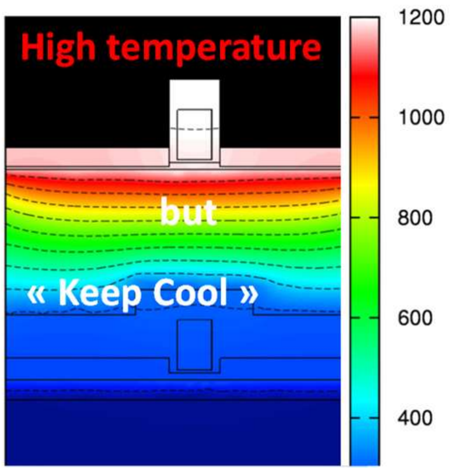
2 **Alternative computing architecture**

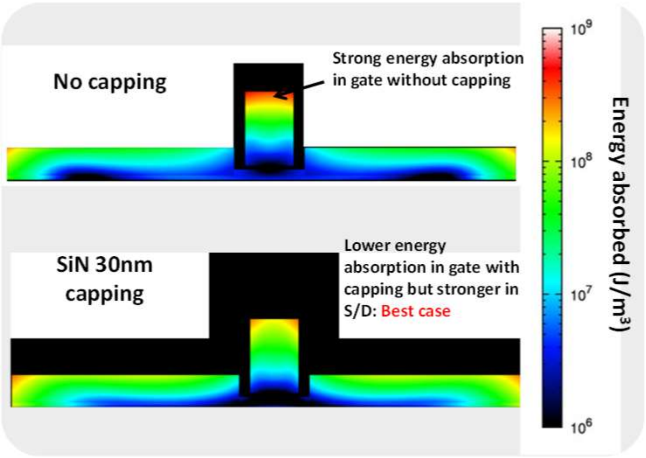
3 **Added functionality**

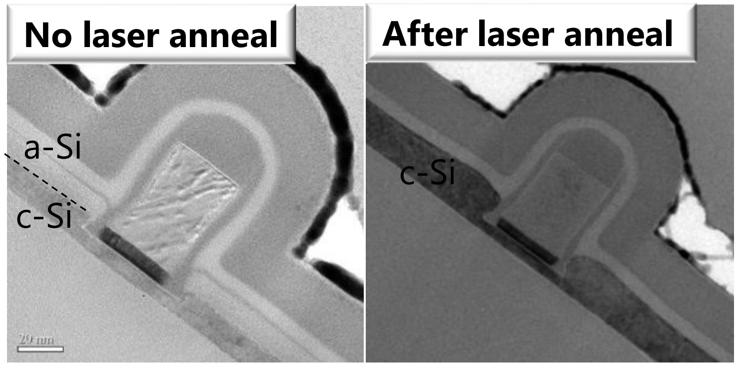
4 **Sensor interface (More than Moore)**

2014 IEDM: Laser for heat confinement

- 3D electro-thermal simulator development (Home made simulator, B Matthieu, SISPAD2015)
  - Nanosec laser annealing experimental demonstration
- Lower dopant diffusion and lower dopant segregation as compared to RTA

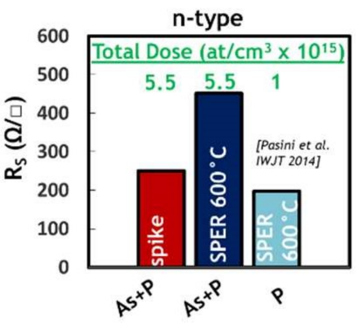


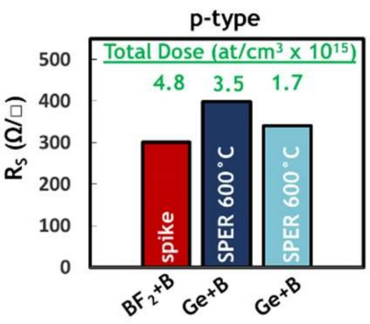


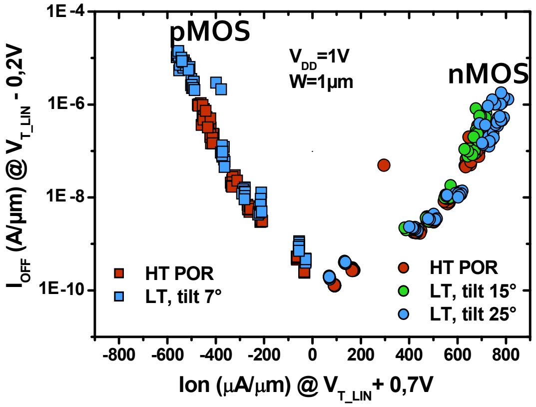


2015 and 2016: Low-temp 28 and 14FDSOI HP Demo

- Best integration scheme for 28 and 14 technology (mix between extension first and last ad in-situ doped)
- Solid-Phase Epitaxy Regrowth activation mechanisms
- Strain preservation

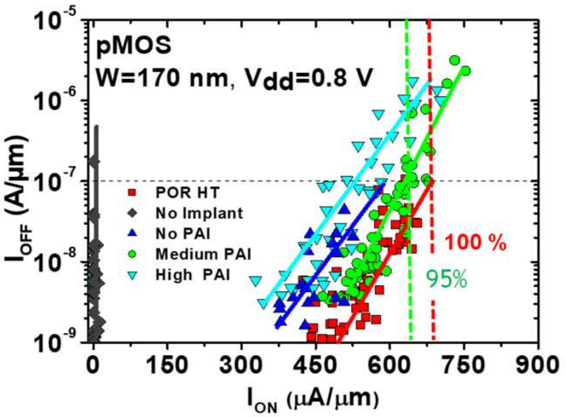






28FDSOI LT junction electrical characteristics

Same I_{ON}-I_{OFF} trade off as HT POR

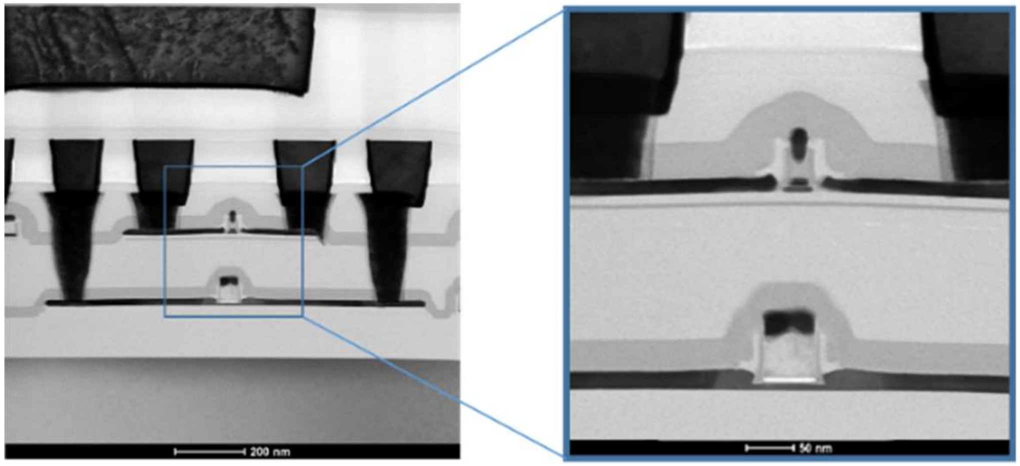


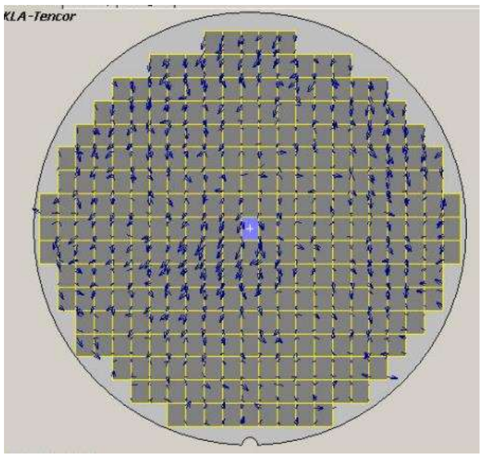
14FDSOI LT junction electrical characteristics

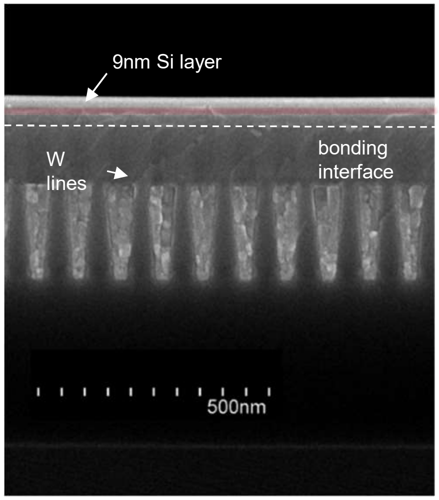
95% I_{ON}-I_{OFF} trade off as HT POR

2016: World’s first 300mm CoolCube™

- 300mm FDSOI on FDSOI transistors
- No deformation of lithographic maps during thin-film transfer
- N over P, and P over N 3D inverters
- Layer transfer above metal lines

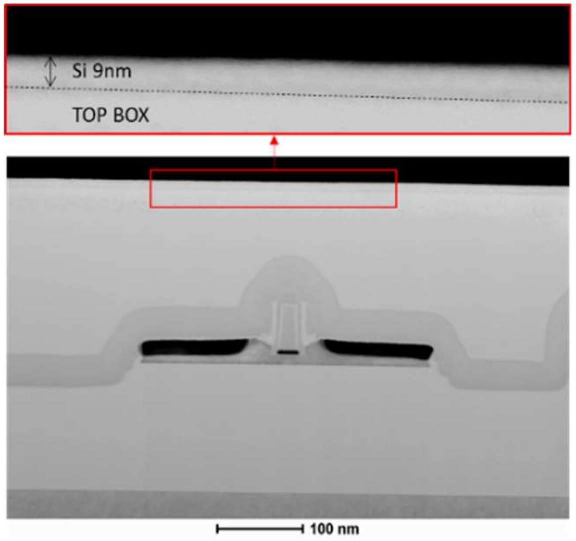


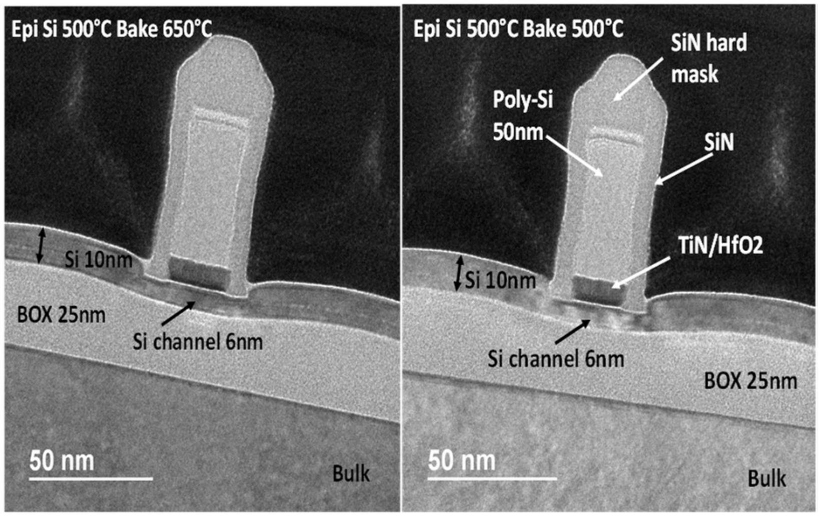




2018 IEDM: towards manufacturing

- Gate resistance optimization
- World first bevel contamination containment
- World first Smartcut© Si transfer on patterned wafers demonstration
- 500°C full epitaxy process (bake and growth)



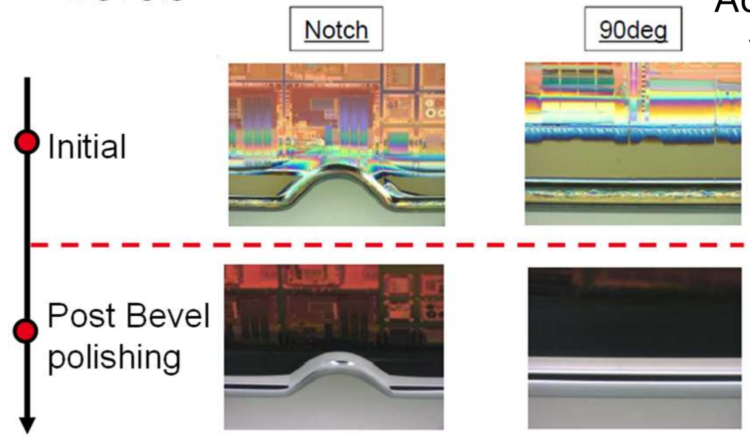


Metrology challenges

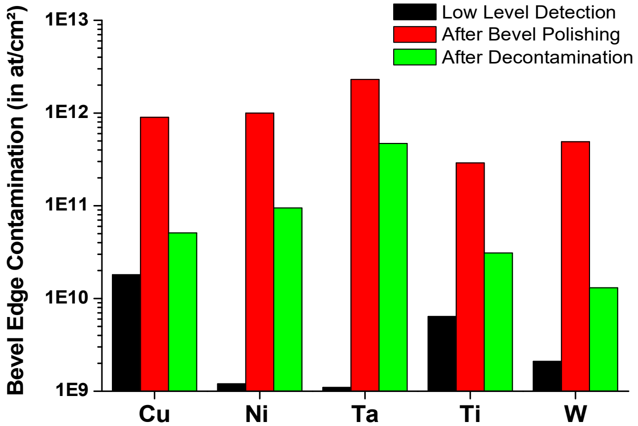
All of the original technologies

➕

- **Surface characterization for bonding**
  - Wafer scale and microscopic roughness
  - Chemical activation
- **Contamination measurements**
  - Backside
  - Bevels



Aqua Regia + nitric acid spiked with controlled HF solution

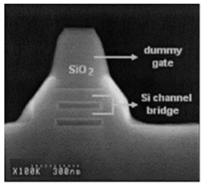


Bevel VDP-DC-ICPMS analysis

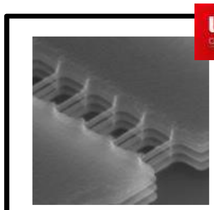
Nanowire integration: 15 years of innovation

MultiBridge Channel MOSFET

S.Y. Lee et al SAMSUNG
IEEE Trans Nano 2003

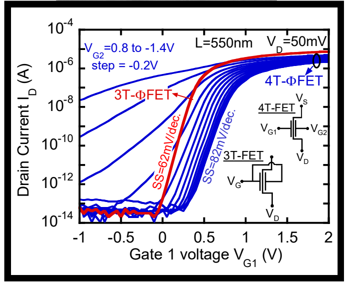


First Stacked NW CMOS

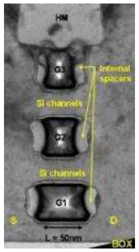


T. Ernst et al. ,
IEDM06

Nanowires with independent gates

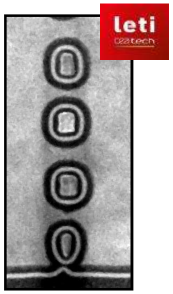


Internal spacers introduction

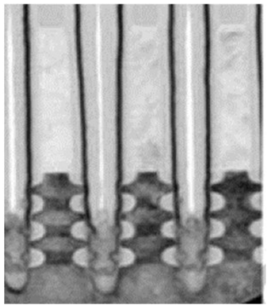


E. Bernard et al.
VLSI 08
LETI - STM

ONO crystalline 3D Flash

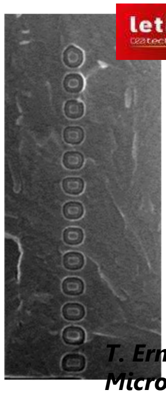


High density



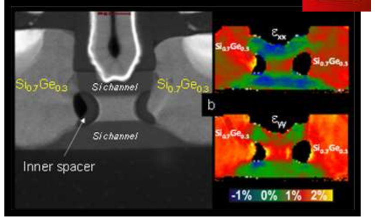
N. Loubet et al. VLSI 2017

13 crystalline levels !



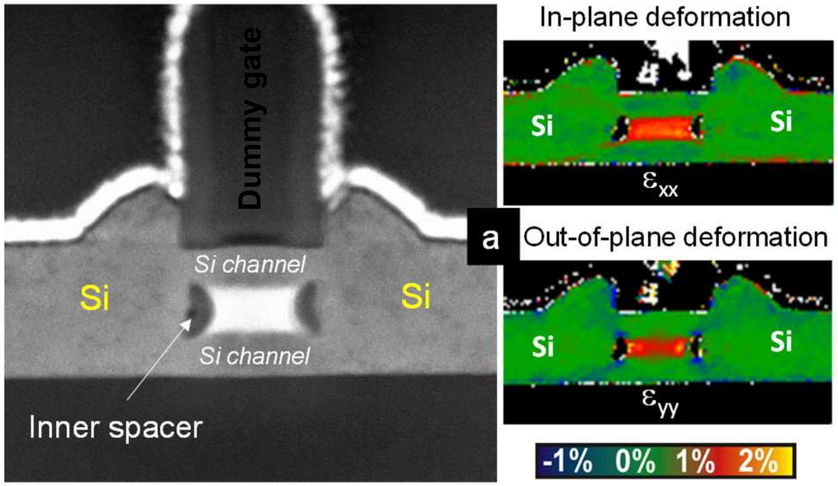
T. Ernst et al.
Micro. Eng. 2011

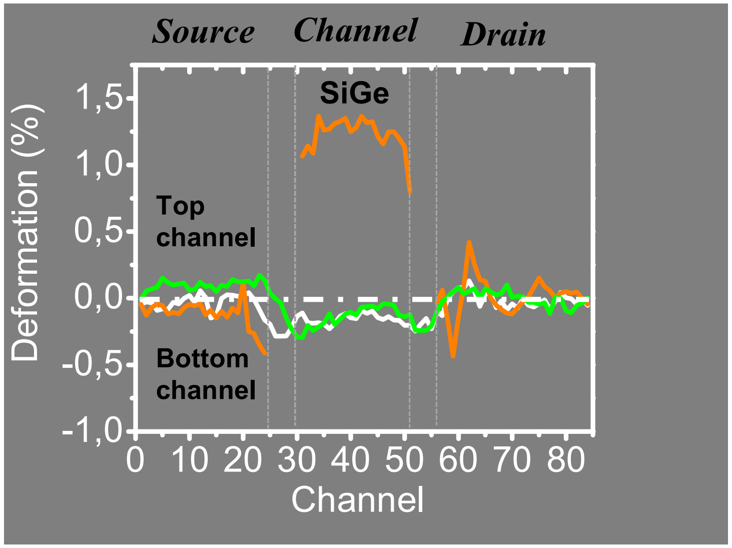
Strain booster



S. Barraud et al.
IEDM 2016, IEDM 2017

Strain characterization techniques





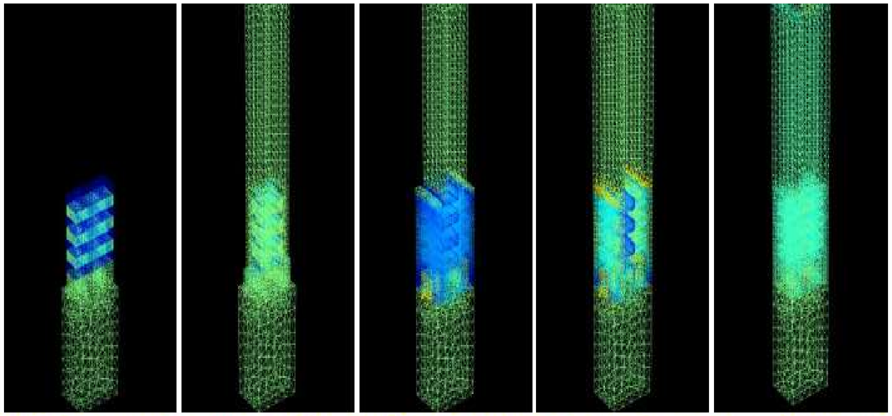
Full strain relaxation of sacrificial $Si_{0.7}Ge_{0.3}$ layer after the Fin recess

An initial strain (substrate-induced strain) is useless

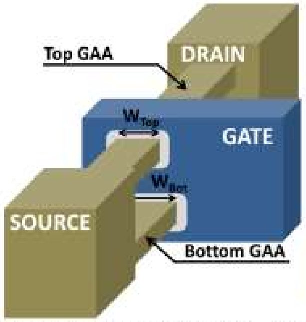
Strain measurement and mechanical simulation

- **Mechanical simulation and unique strain characterization**
- **Predictivice compact modelling – unique versatile solution**

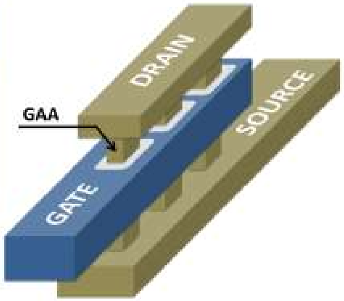
O Rozeau, IEDM 2016



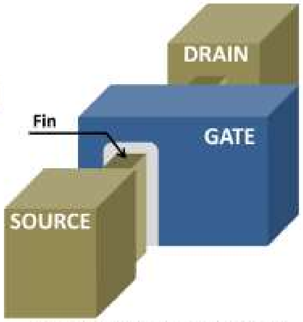
☐ Vertically stacked GAA MOSFET (nanosheet and/or nanowire)
☐ Vertical GAA MOSFET (nanosheet and/or nanowire)
☐ FinFET / Trigate MOSFET



Vertically stacked GAA MOSFET



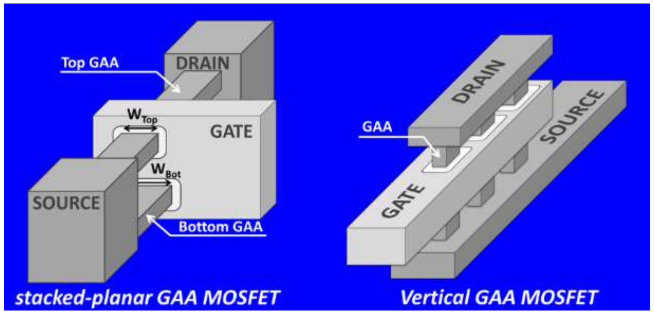
Vertical GAA MOSFET

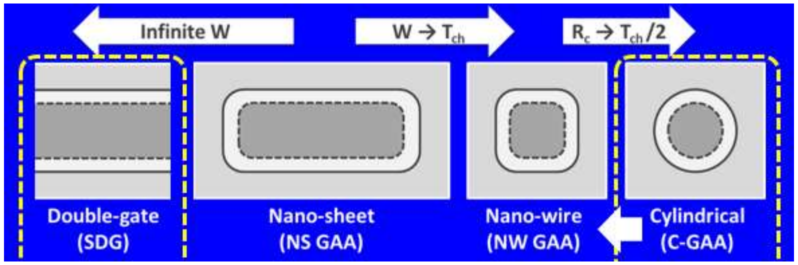


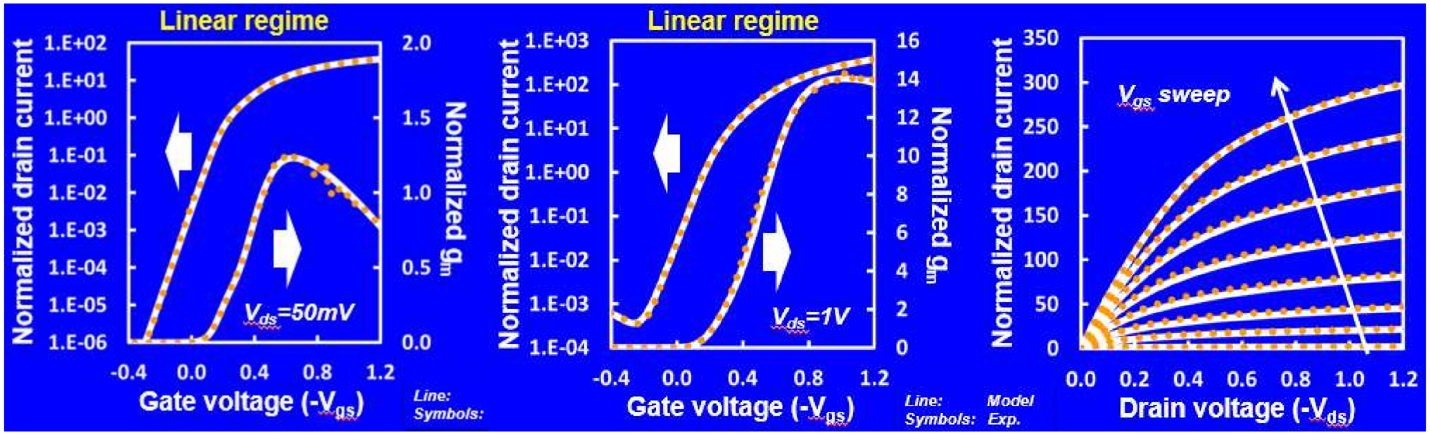
FinFET/Trigate MOSFET

Compact model for Nanowires

- Leti-NSP is a unique surface potential based model able to describe nanowire transistors whatever the shape of the wires







O. Rozeau et al. IEDM 2016

- **Model accuracy and predictability successfully checked against hardware date**

Quantum computing in numbers

Solving useful problems requires a tremendous scaling

Quantum supremacy
(theory demonstration)
50 qubits

Quantum chemistry
200 perfect qubits
Number of operations ~N^4

Factorization, AI, data mining
2000 perfect qubits
Number of operations ~N^3

Billions of errorless quantum operations

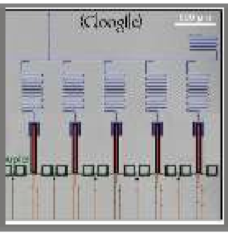
Well beyond reach for actual physical systems (due to decoherence)

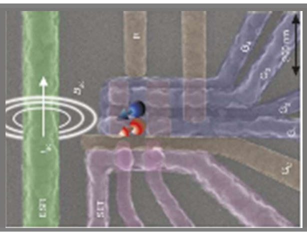
2 paths

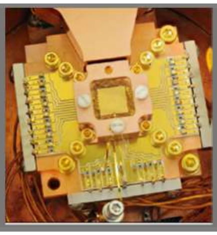
Fault tolerant quantum computing
Overhead in terms of qubits
Qubits > millions

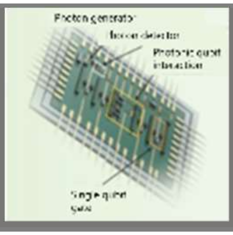
More robust qubits

State of the art



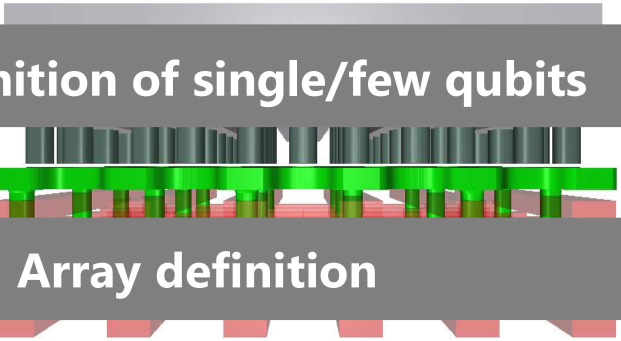






	Superconductor	**Si spin**		**Trapped ions**	**Photons**
Size*	(100µm)²	(100nm)²	~	(1mm)²	~(100µm)²
Fidelity	~99.3%	>98%	↗↗	99.9%	50% (mesure) 98% (portes)
Speed	250 ns	~5 µs	↘	100 µs	1 ms
Manufacturing	🟧	🟩	~	🟧	🟩
Variability	3%	0.1%-0.5%	↘	0.01%	0.5%
Operation T°	50mK	1K	~	300K	4K
Entangled qubits	20	2	↗↗	20	18

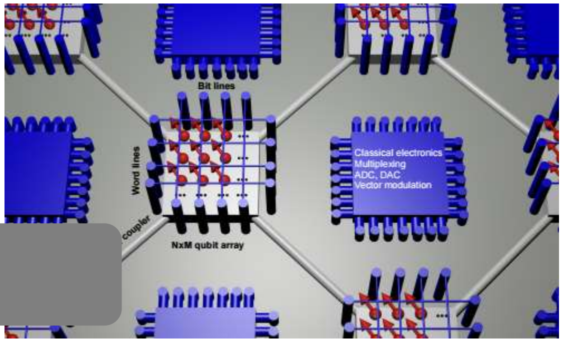
Quantum computing architectures



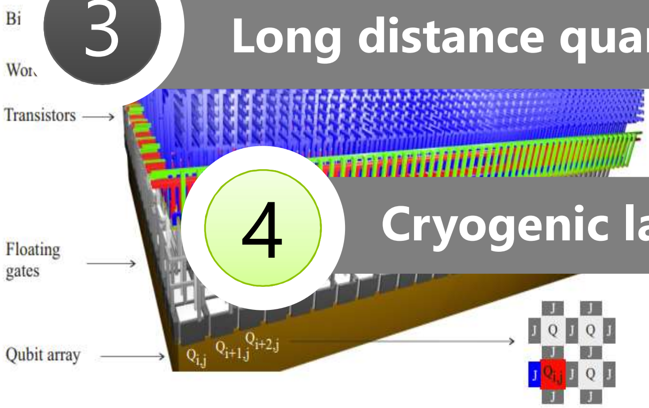
1 **Definition of single/few qubits**

2 **Array definition**

Our Architecture in Grenoble



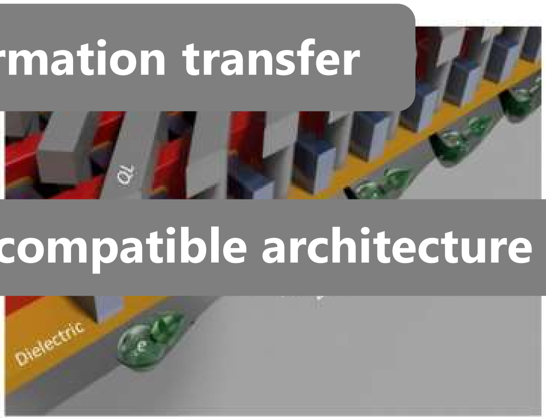
L.M.K. Vandersypen et al., npj Quant. Inf. (2017)



3 **Long distance quantum information transfer**

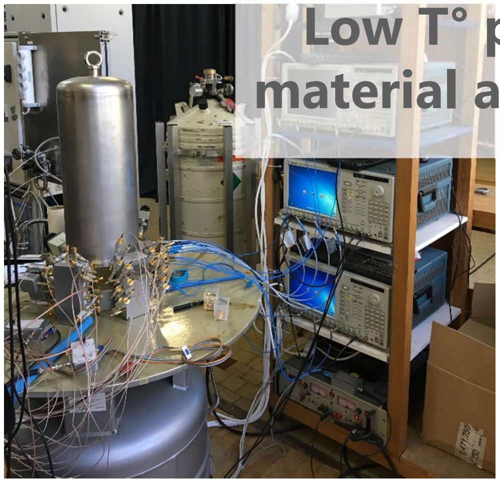
4 **Cryogenic large scale compatible architecture**

M. Veldhorst et al. (UNSW), Nature Comm. (2017)

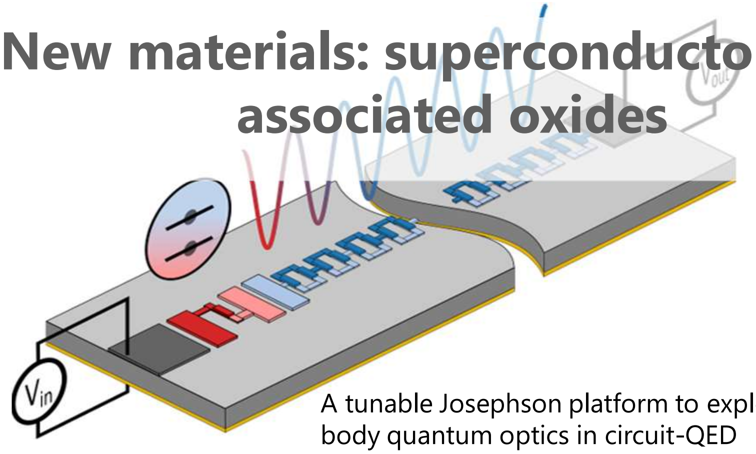


Quantum computing key features

Low T° properties: material and electrical

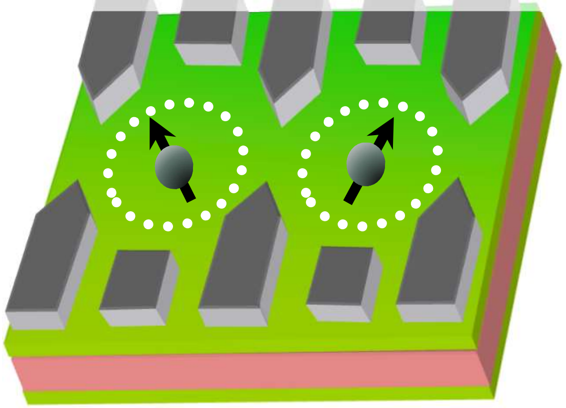


New materials: superconductors and associated oxides

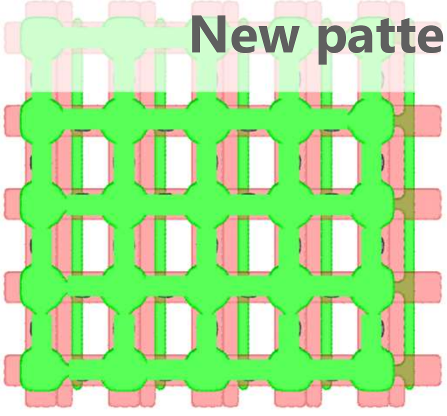


A tunable Josephson platform to explore many-body quantum optics in circuit-QED
Roch et al, ArXiv1802.00633

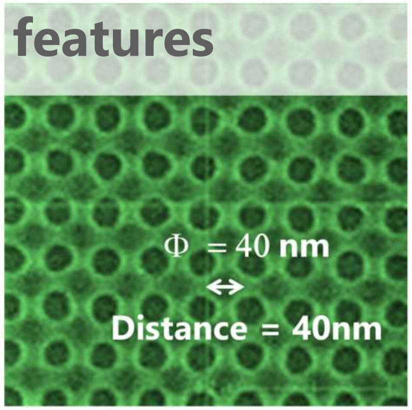
Few charges regime



New patterning features



Need for a2D array of dots connected by tunnel barriers



Conclusions

FDSOI, memories, CoolCube, nanowires, qubits (NCFET, FeFET, 2D materials…):

CMOS scaling has turned into **devices adding**

- Still a lot of opportunities and needs for technological developments
- In addition to the already existing needs for metrology, we are longing for accurate methods for:
  - Material characterization
  - Surface composition and roughness
  - Strain characterization
  - Within a wide range of temperature, charge density regime and geometries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Acknowledgments:
L. Grenouillet, L. Brunet, C. Fenouillet-Beranger, P. Batude, S. Beaurepaire, F. Ponthenier, N. Rambal, V. Mazzocchi, J-B. Pin, P. Acosta-Alba, S. Kerdiles, P. Besson, H. Fontaine, T. Lardin, F. Fournel, V. Larrey, F. Mazen, V. Balan, C. Morales, C. Guerin, V. Jousseaume, X. Federspiel, D. Ney, X. Garros, A. Roman, D. Scevola, P. Perreau, F. Kouemeni-Tchouake, L. Arnaud, C. Scibetta, S. Chevalliez, F. Aussenac, J. Aubin, S. Reboh, F. Andrieu, S. Maitrejean, L. Hutin, B. Bertrand, Y. Thonnart, G. Pillonnet, G. Billiot, H. Jacquinot, M. Cassé, S. Barraud, J.-M. Hartmann, Y.-J. Kim, V. Mazzocchi, S. De Franceschi and T. Meunier, V. Delaye

Thank you

The programs were/are partly funded by:
- theFrench Public Authorities through the NANO2017 & WAYTOGOFAST programsn through the ANR CMOSQuSpin
- H2020 EU fundings through SuperAid, 3DAM, 3DMuse, MOSQUITO ICT projects
- ERC project QuCube
- Industrial support of STMicroelectronics, Applied Materials, Screen,