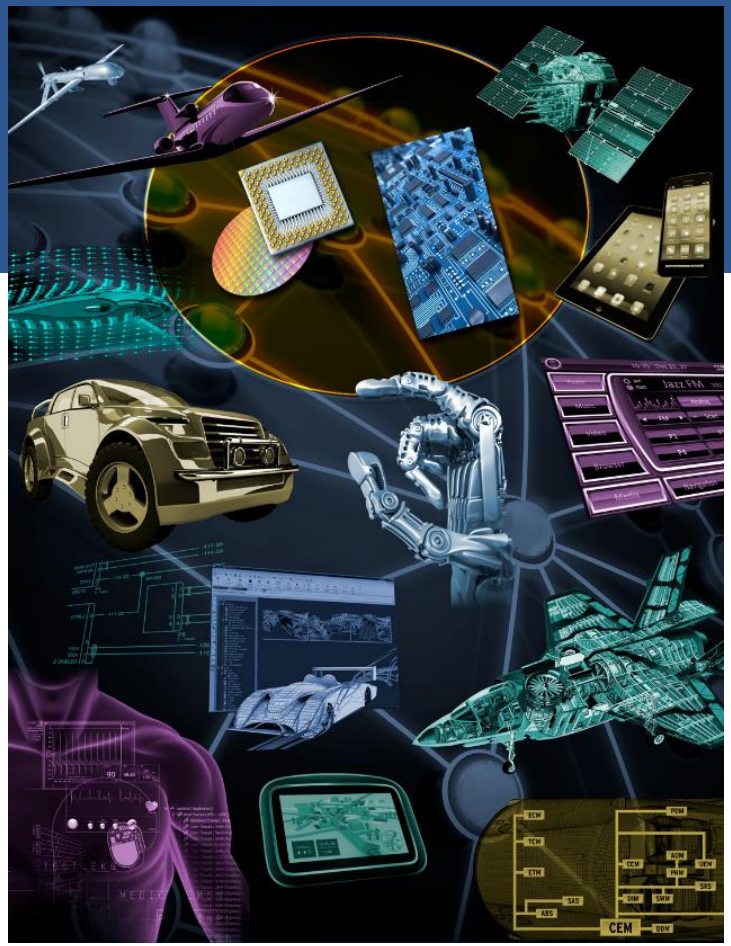

Evolution of EDA from Electronics to Photonics

Tony Liao

IC Design Solutions Design Kit Development Manager

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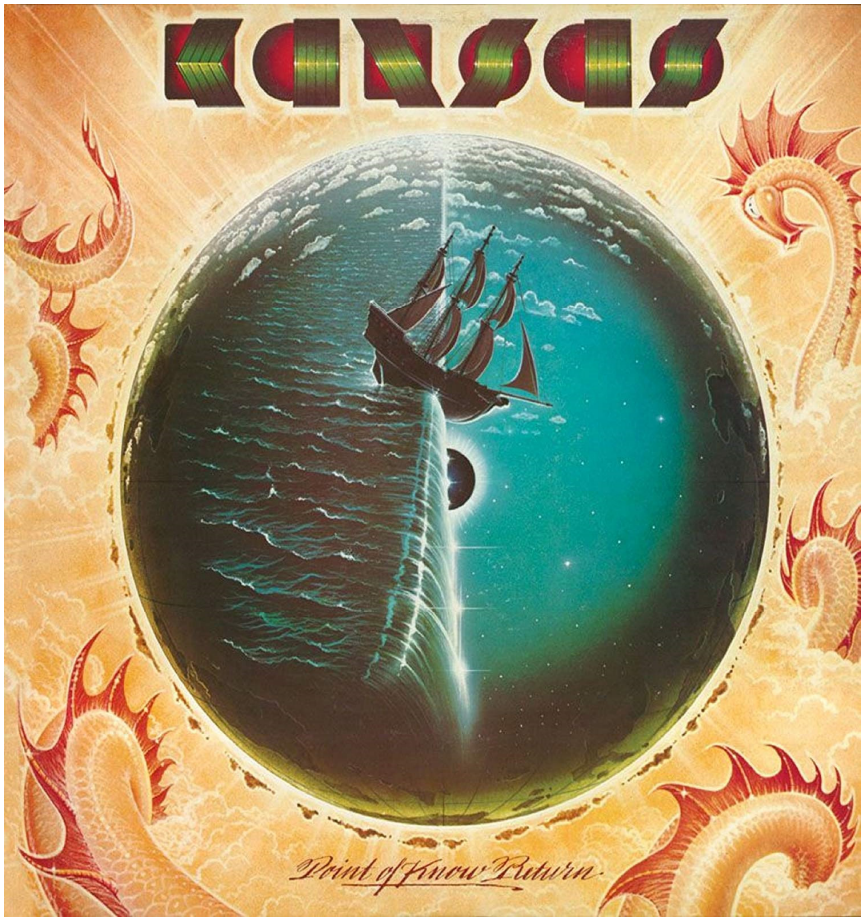
cea leti

Mentor®

A Siemens Business

Traditional IC Design

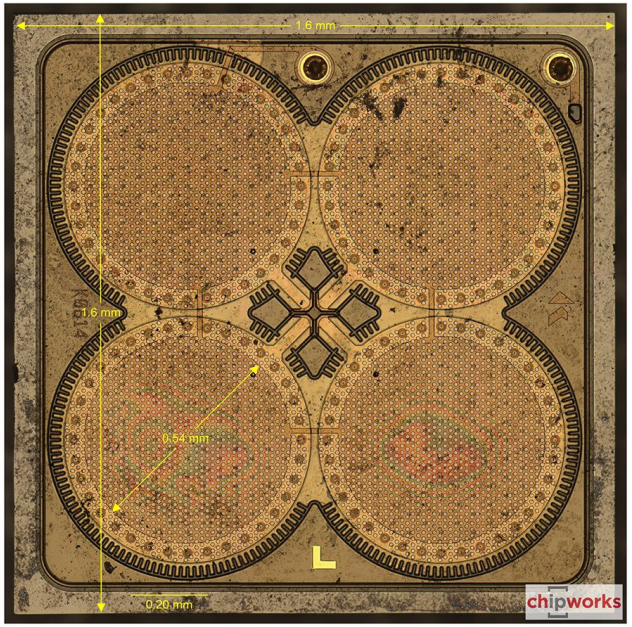
- Designers & tool developers have lived in a orthogonal world for 50+ years
- Electronic Design Automation tools
  - Tens of thousands of man/years developing software
  - Representing 100's of millions lines of code
- IC designers have been told not to use curved structures
- Lithography (steppers) are based on rectangles



Curved Structures – No Longer Outliers

MEMS & Photonics

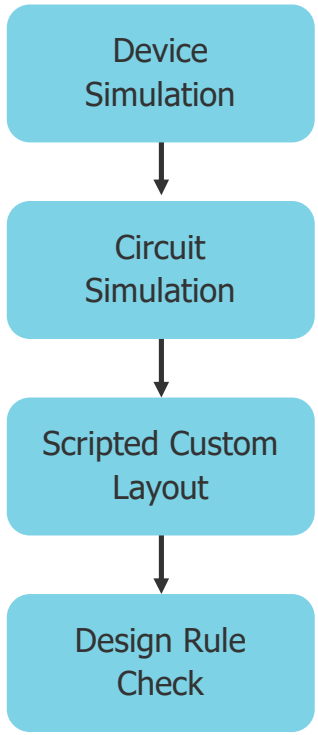
- MEMS has become a driver of curved structures
- We indirectly MEMS every day in our car and on our cell phone



Accelerometer
Antenna switch
Compass
Gyroscope
Oscillators
Pressure sensor
. . .

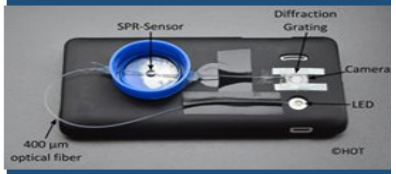
Photonics Today - Is like CMOS in the early 80's

- Must be an expert
- Manual design flow
- No standards to help
- No abstractions
- First time design success were rare



Integrated Photonics Applications

Sensors



Research & Design

Designer Needs
- Number of components < 50
- Devices optimization
- Easily retargetable to other foundries

EDA Needs
- Manual layout editing
- Optical simulation
- Physical verification
- Automate migration to other foundries
- Test chip creation

Networking (outside the box)

Production

Designer Needs
- Number of components < 100
- Photonics/Electronics co-simulation
- Foundry PDK

EDA Needs
- Manual layout editing
- Optical/electrical simulation
- Physical verification
- Routing capabilities

Self driving cars - LIDAR

Research

Designer Needs
- Number of components < 50
- Devices optimization
- Easily retargetable to other foundries

EDA Needs
- Manual layout editing
- Optical simulation
- Physical verification
- Automate migration to other foundries
- Test chip creation

Networking (in the box) & High Performance Computing

Research

Designer Needs
- Number of components > 10,000
- Photonics/Electronics co-simulation
- Foundry PDK

EDA Needs
- Optical/electrical co-simulation
- Physical verification
- Automation

Recent Customer Question

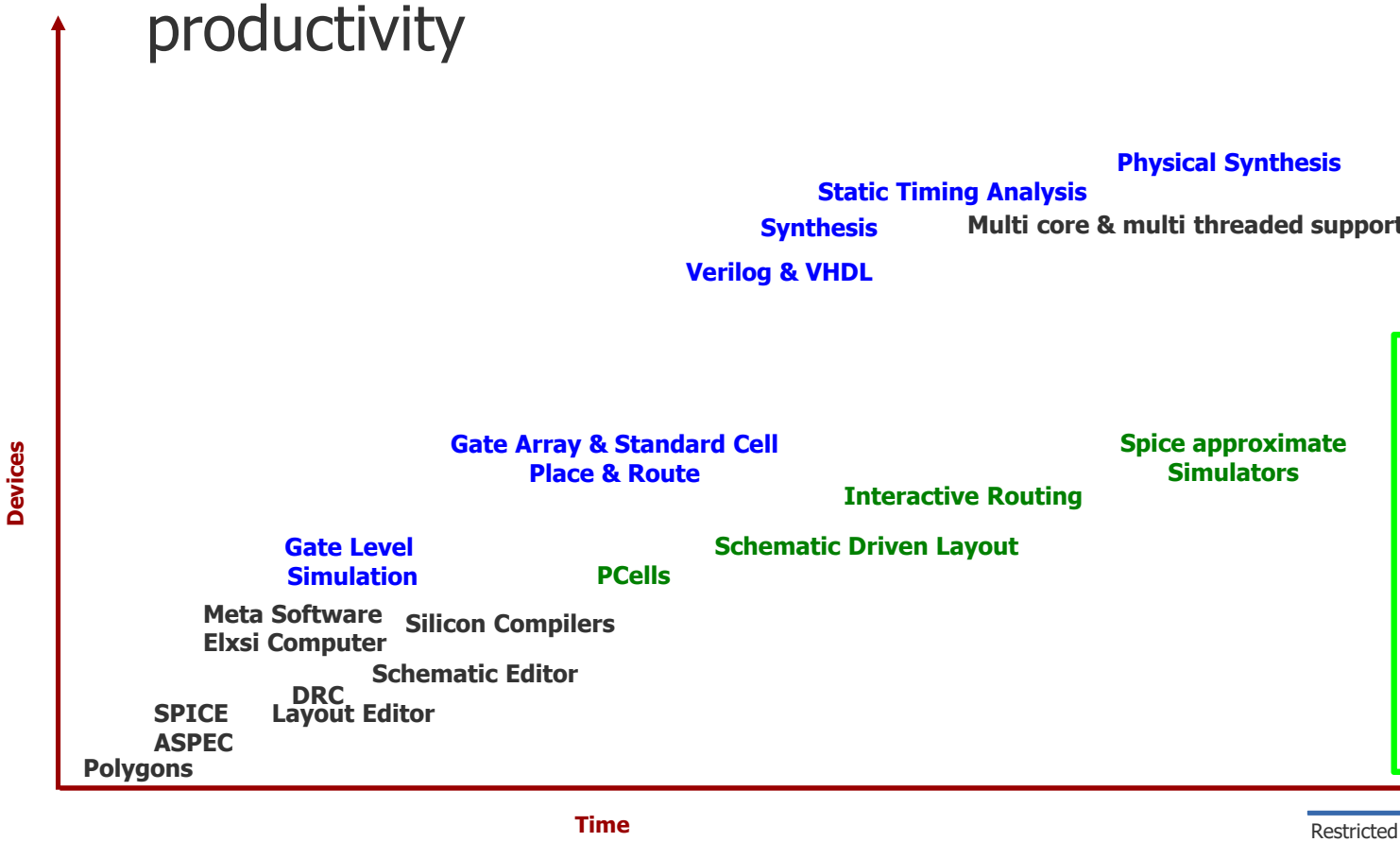
How long does it take to automatically layout a photonics design with 100,000 components?

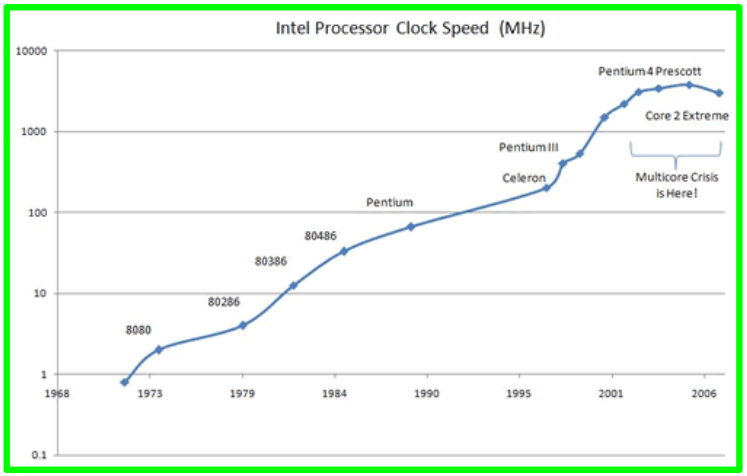
How do we get to 100,000 Component Designs?

- Designers need more productivity
- Need to expand the designer base
- Standards

Productivity Improvements

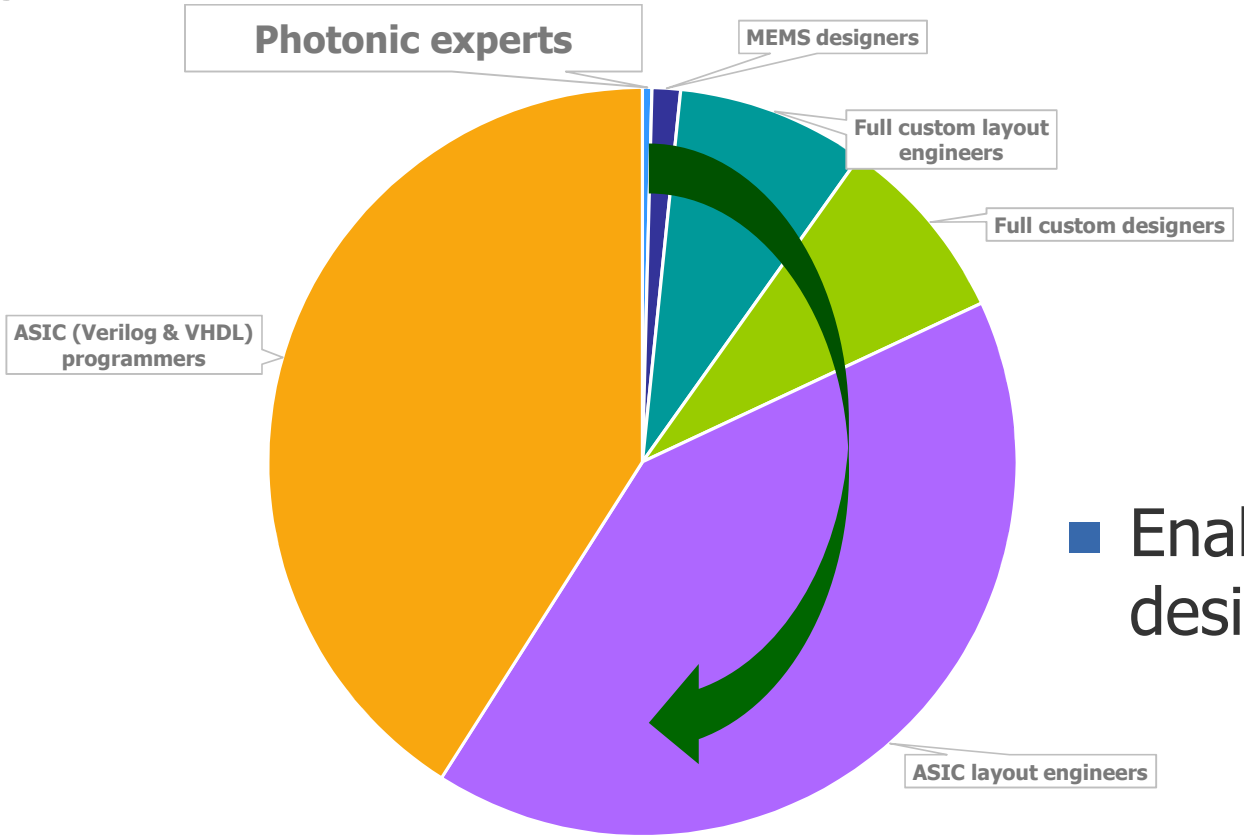
- Automation & new methodologies vastly improved IC design productivity





Expand Designer Base

- Not enough photonics experts



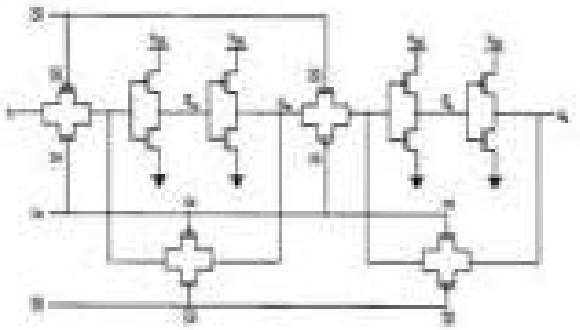
- Enable other designers

How Did We Grow From
1,000's Custom Engineers -> 10,000's ASIC Engineers

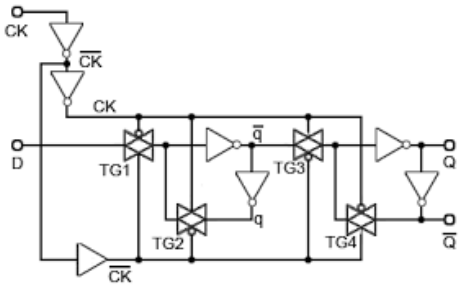
- Simplified what they needed to know
- Standards
- Abstractions enabled
  - — Faster simulation
  - — Synthesis
  - — Automatic placement and routing

Simplified What the Designer Needs to Know

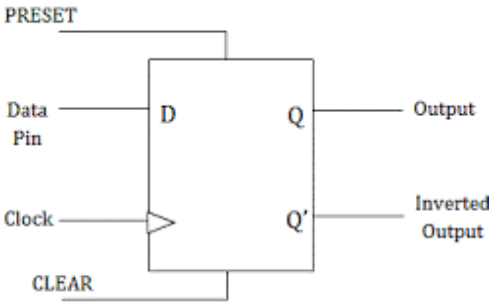
- Four different representations of a D Flip-Flop



Transistor level Schematic



Gate level Schematic



Logic Symbol

Full Custom Designer Engineer

Verilog Programmer

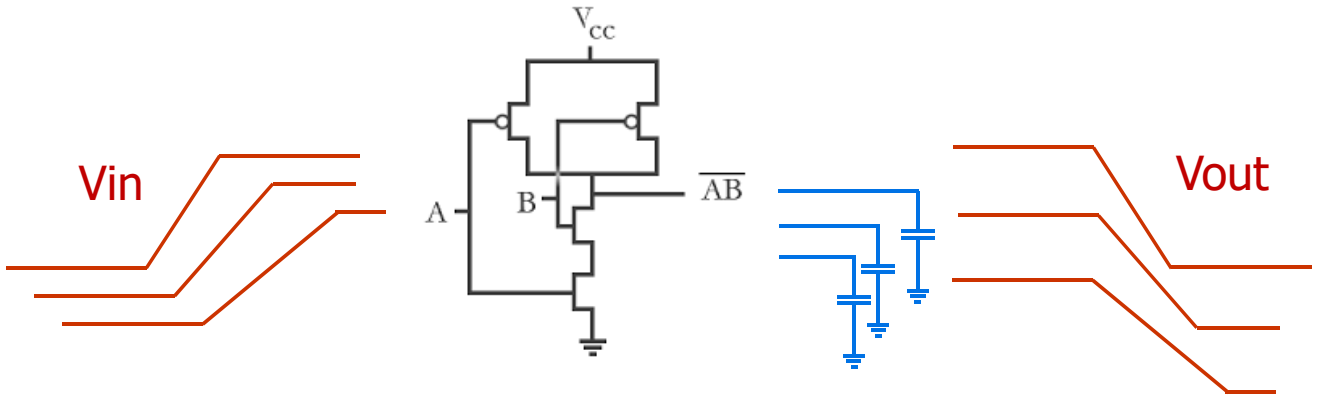
```
module flipflop(Q,D,Clk);
  input D,Clk;
  output Q; reg Q;
    always @(posedge Clk)
      Q <= D;
endmodule
```

Verilog

Abstracted Design Data

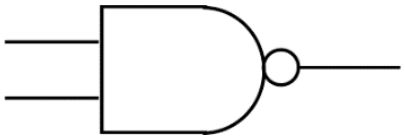
- Never be able to simulate 100,000 component design without abstractions
  - Transistor level simulation with timing would take way too long

- Run many simulations on individual standard cells to build an abstracted model



Abstractions Enables Faster Tools

- Move from transistor simulation to
  - Gate level simulation
  - Static Timing Analysis



Logic Symbol

```
module nand1(c,a,b);
 output c;
 input a,b;
 wire d;
 and1 u1(d,a,b);
 inv u2(c,d);
endmodule
```

Logic Simulation Model

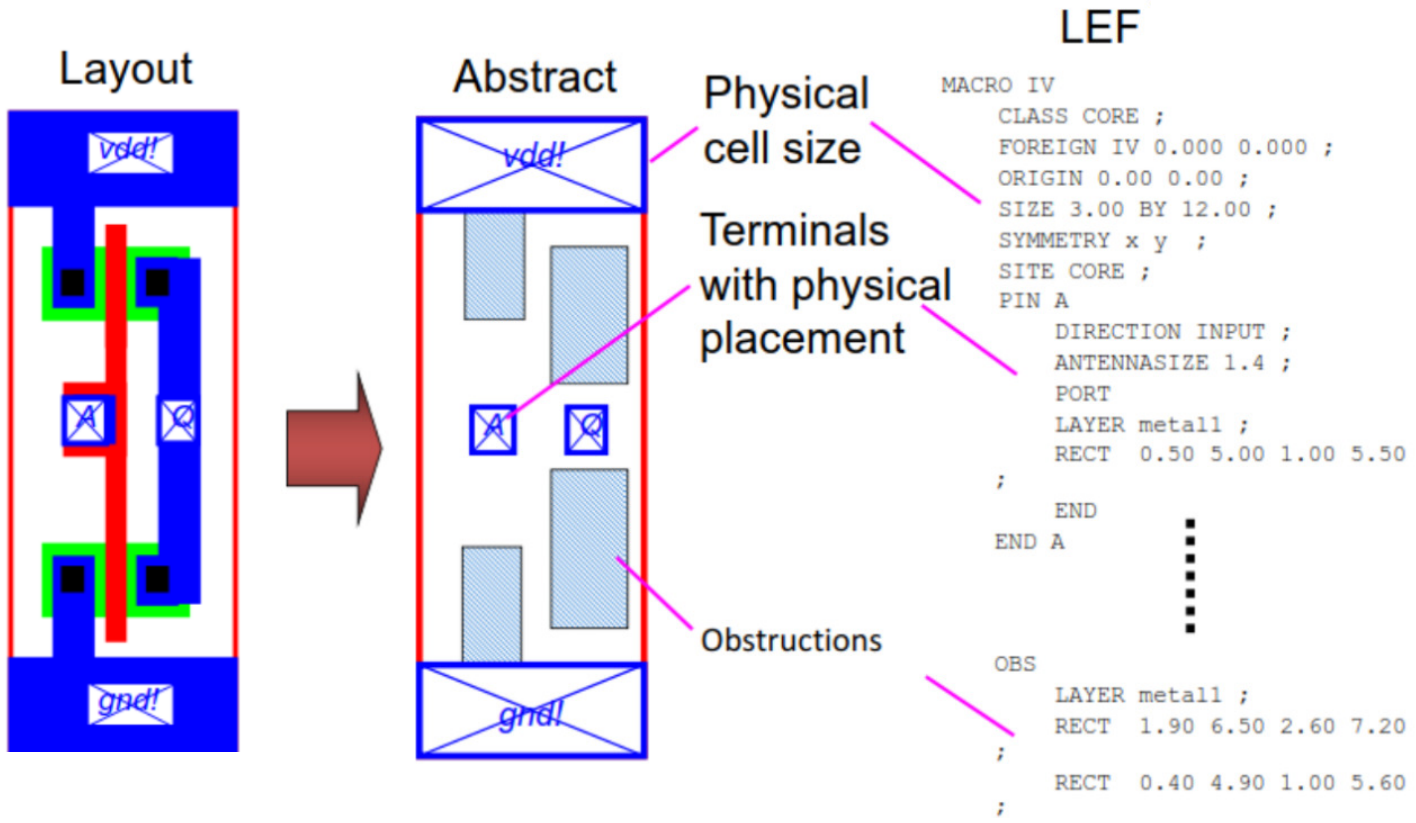
```
pin (C) {direction : output ;function : "~(A + B)" ;
}
lu_table_template(wire_delay_table_template) {
  variable_1 : fanout_number;
  variable_2 : fanout_pin_capacitance;
  variable_3 : driver_slew;
  index_1 ("1.0 , 3.0");
  index_2 ("0.12, 4.24");
  index_3 ("0.1, 2.7, 3.12");}

lu_table_template(trans_template) {
  variable_1 : total_output_net_capacitance;
  index_1 ("0.0, 1.5, 2.0, 2.5");
}
wire_load("05x05") {
  resistance : 0 ;
  capacitance : 1 ;
  area : 0 ;
  slope : 0.186 ;
  fanout_length(1,0.39) ;
  interconnect_delay(wire_delay_table_template)
  values("0.00,0.21,0.3", "0.11,0.23,0.41", \ "0.00,0.44,0.57", "0.10 0.3, 0.41;
}
```

Static Timing Model

Abstraction Reduces Design Data

- Increases Capacity

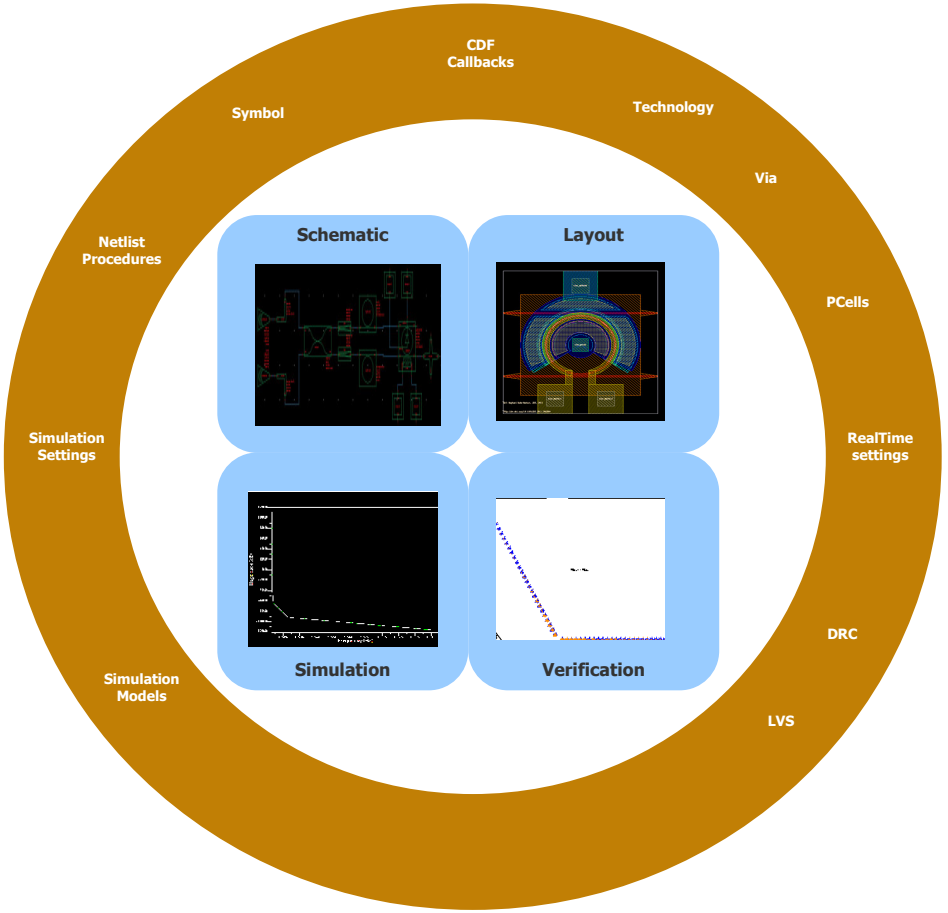


Standards for Photonics

- Designers & foundries love
  - Lessens their work
- What is needed?
  - Simulation netlist format
    - De facto today with modified spice
  - A foundry **P**rocess **D**esign **K**it
  - Others?

Integrated Photonics PDK

- Manufacturing layers and verification rules
- Set of foundry pre-characterized devices (parameterized or fixed)
- Maturity has been questionable
  - Devices you need but not at the performance you want!
  - Designers may spend few cycles to optimize their devices

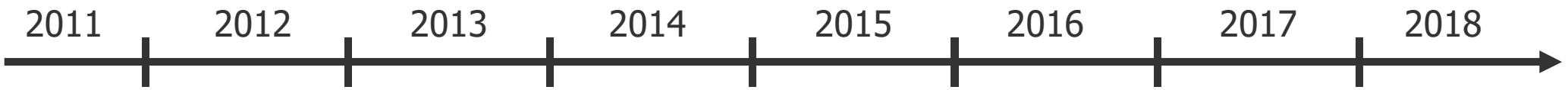


Recap: Electronics Versus Photonics

	Electronics
Design Flow	Traditional Analog, digital and Analog Mixed-signal design flows
Community	Seasoned designers with 30+ years of CAD knowledge
PDK	Technology/process options and metal stacks based PDKs advanced nodes
	Traditional foundries: TSMC, GF, UMC, SMIC, X-FAB, TowerJazz, etc
	Traditional devices categories: MOS, capacitor, resistor, diodes, inductors and BJTs
	Average of ~200 components per PDK
	DRC, LVS, PEX and PERC

MENTOR & PHOTONICS

Mentor Is Not New to Photonics



Educational

SI-EPIC

CMC

webinar

webinar edX

webinar

webinar

webinar edX AIM ACADEMY

Consortiums & Research

OPSIS

plat4M

NANOELEC.

cea leti

AIM photonics

Photonic Software Partners

lumerical

LUCEDA

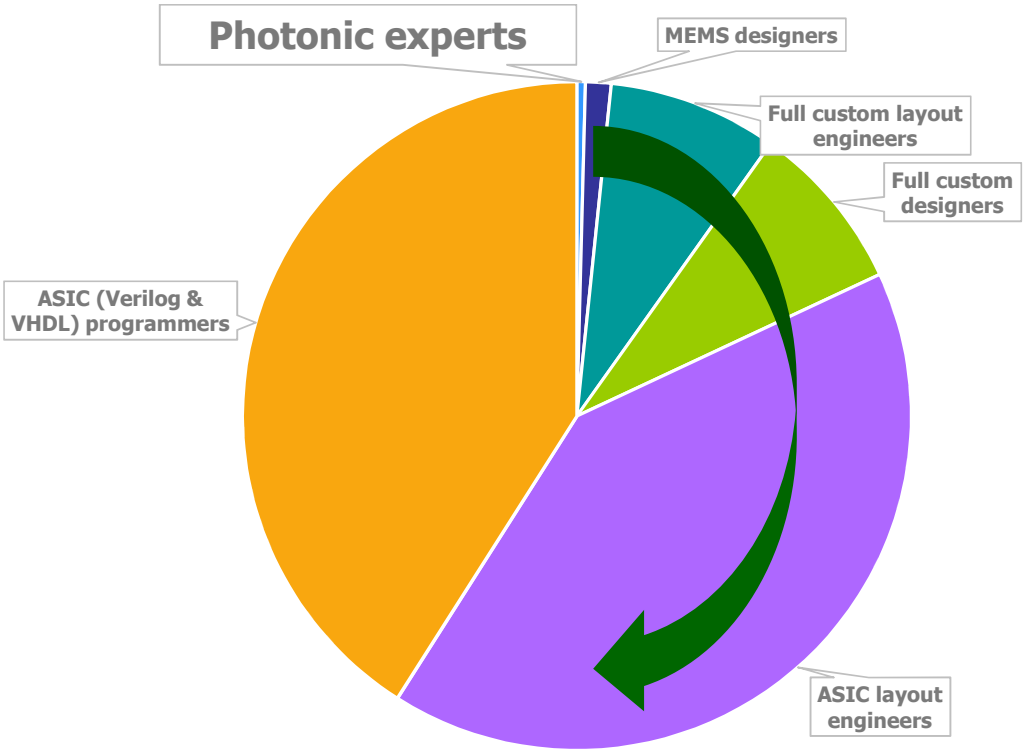
VPIphotonics

Optiwave

Mentor A Siemens Business

Mentor's Focus

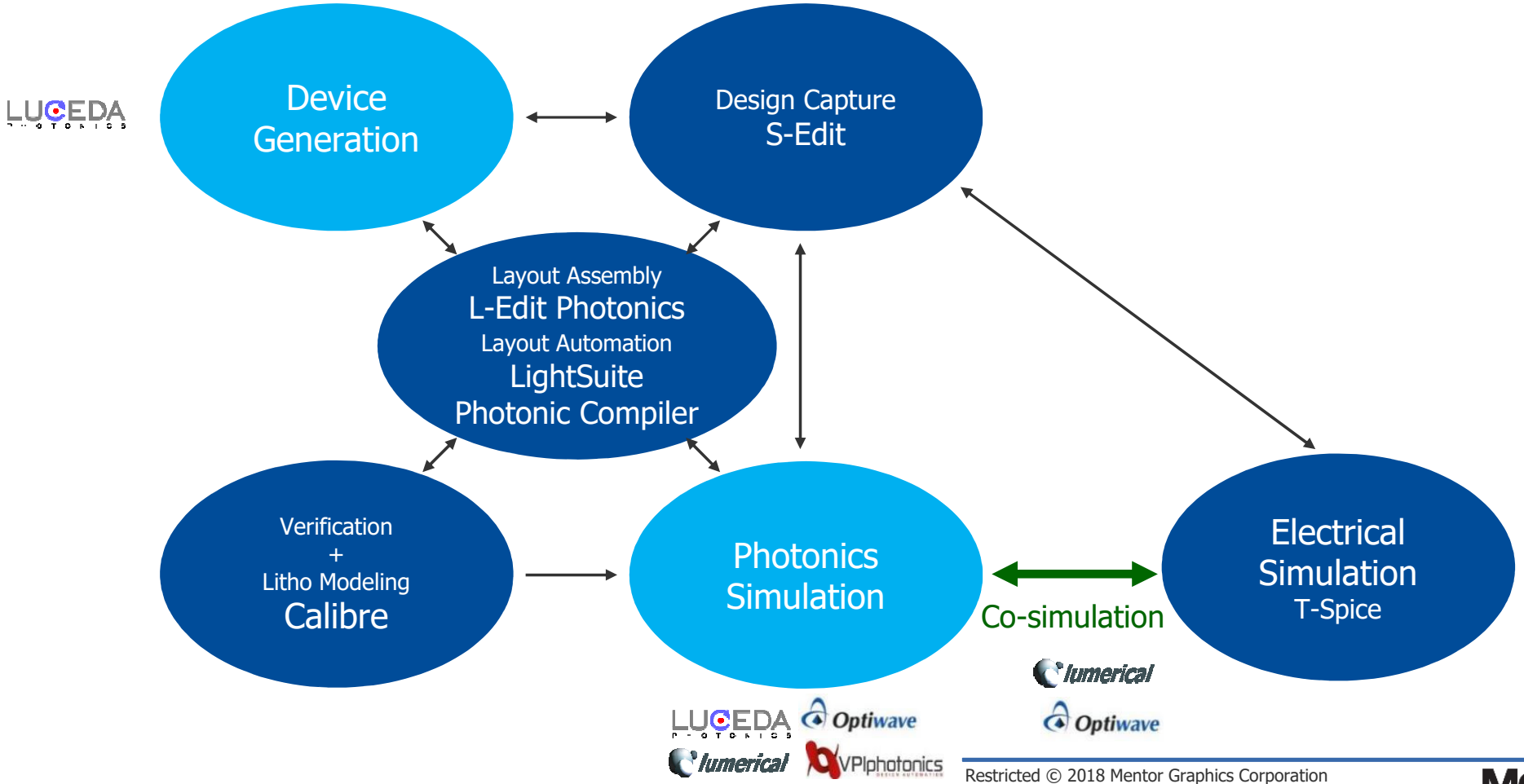
- Productivity improvements for the photonics experts



- Enable the IC designer for photonic design

DESIGN TOOLS

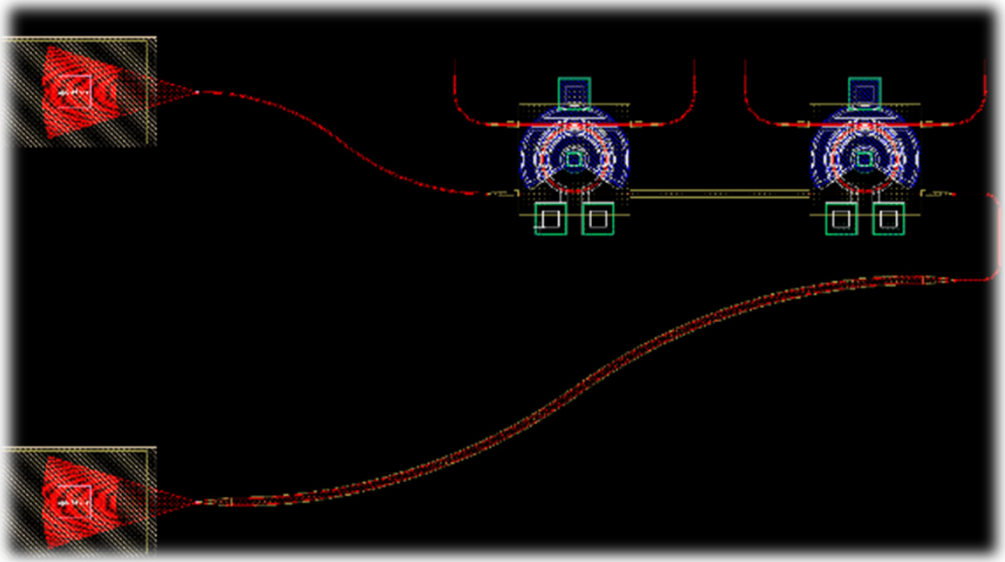
Integrated Photonics Design Flow



Expand the User Base

L-Edit Photonics

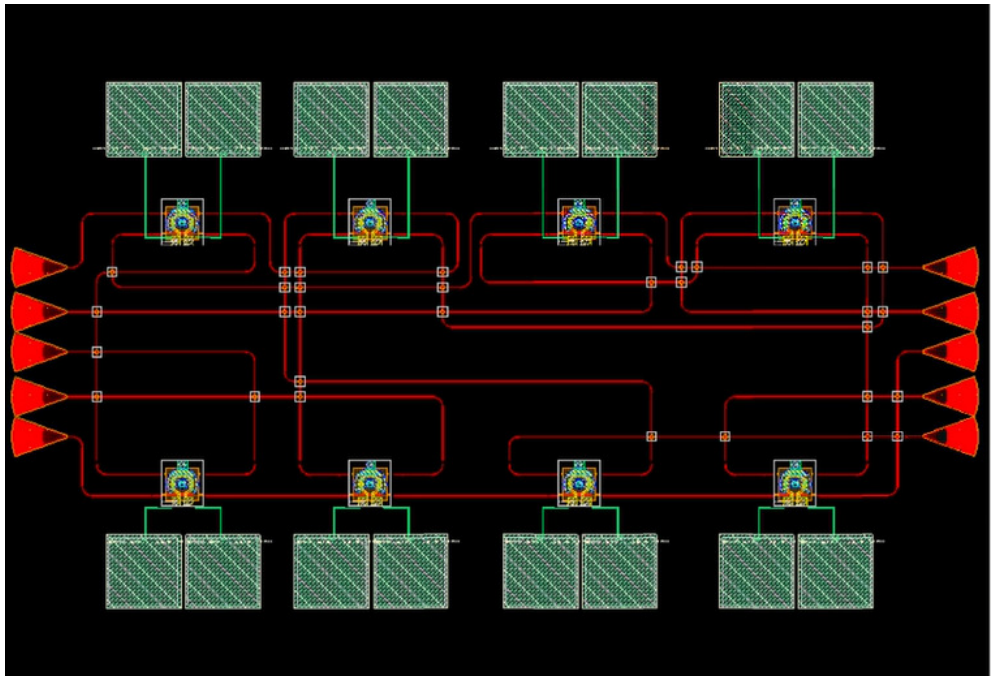
- Enables IC layout engineers
- Photonic design in a IC layout editor
- Focused on layout centric design
  - Schematic optional flow
- Photonic specific functionality
  - Simple waveguide creation and editing
  - Crossing insertion
  - Precision snapping to optical pins
  - Waveguide to pin checking
  - Exports simulation netlist
    - Luceda
    - Lumerical
    - Optiwave
    - VPIphotonics



Productivity Improvements

LightSuite Photonic Compiler

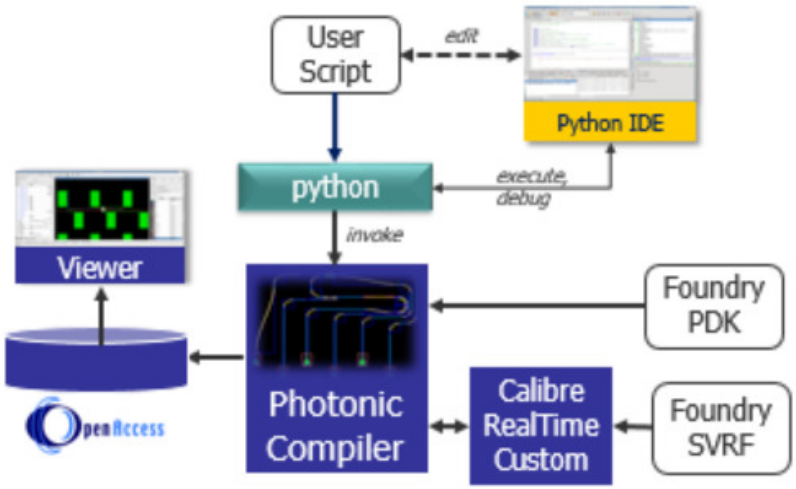
- Industry's first integrated electrical/photonic layout automation tool
- Places components from the PDK
- Routes both photonic waveguides and electrical nets
- Enables "what if" analysis
  - Rapidly produces a new layout
- Produces a DRC correct design
  - Correct by Calibre
  - Requires Calibre RealTime license
  - eqDRC based SVRF rules
- Built on standards
  - OpenAccess
  - Python
  - PDK



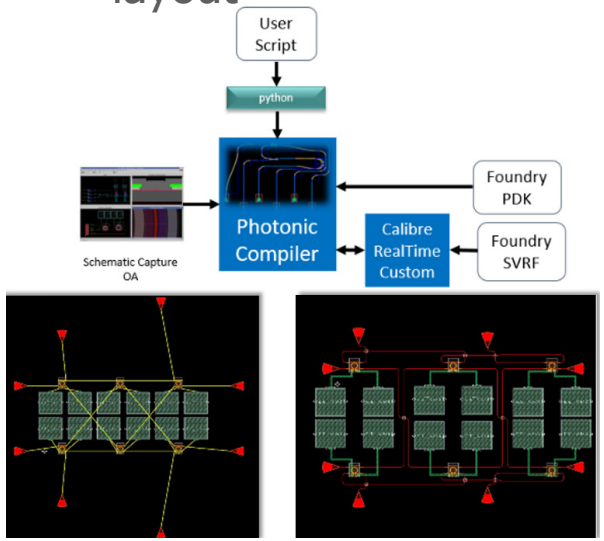
LightSuite Photonic Compiler

Supported Flows

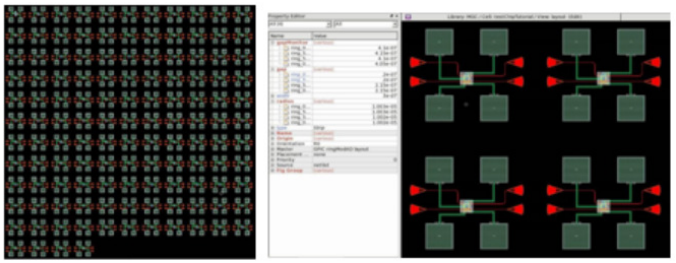
- **Script Driven**
  - Photonics expert
  - User has complete control



- **Schematic Driven Layout**
  - IC designer
  - Schematic defines layout



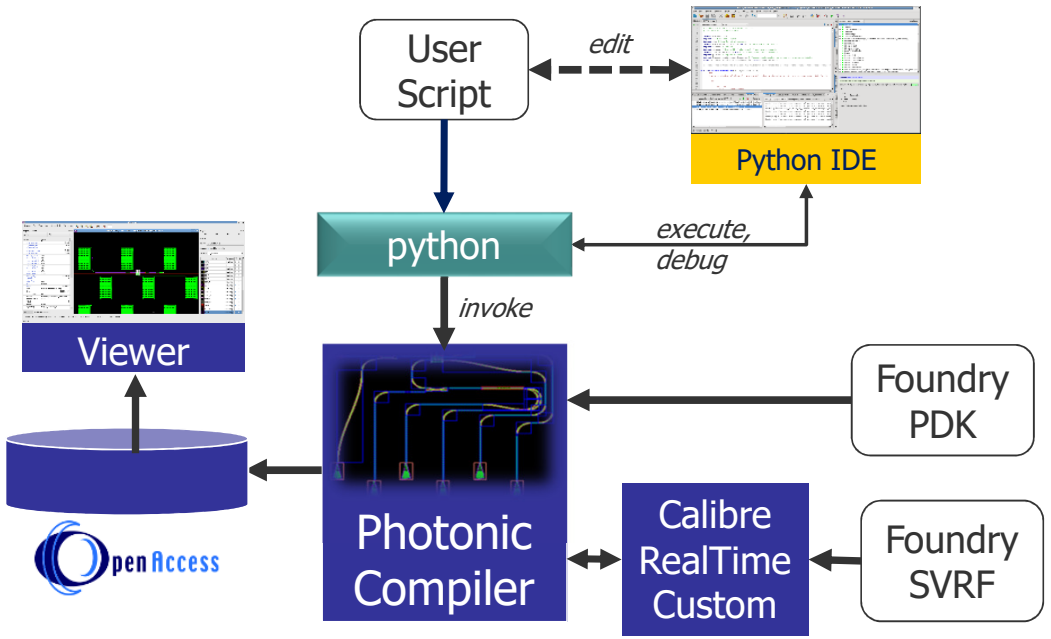
- **Test Chip**
  - PDK developers
  - Place Pcells & sweep parameters



Productivity Improvements for Photonics Experts

LightSuite Photonic Compiler – Script Driven Flow

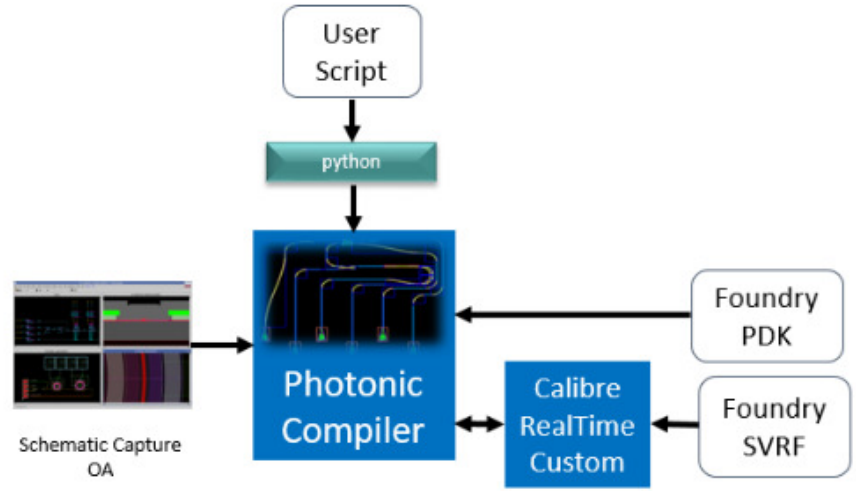
- Script Driven flow
  - User interacts with a Python IDE
  - Start LightSuite Photonic Compiler
  - Viewer shows layout progress
  - Components are placed
  - Optical waveguides routed
  - Electrical signals routed
  - Resulting design saved in OA
- Calibre RealTime Custom runs in the background
  - Every placement move
  - Every route, waveguide or electrical net

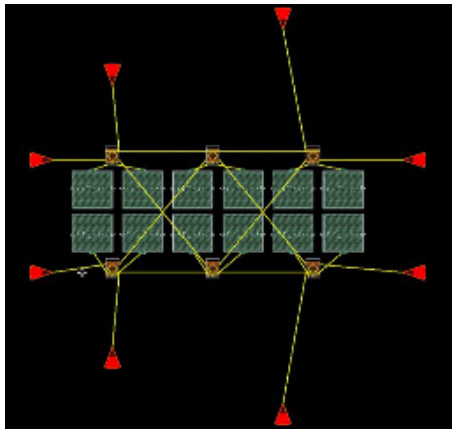


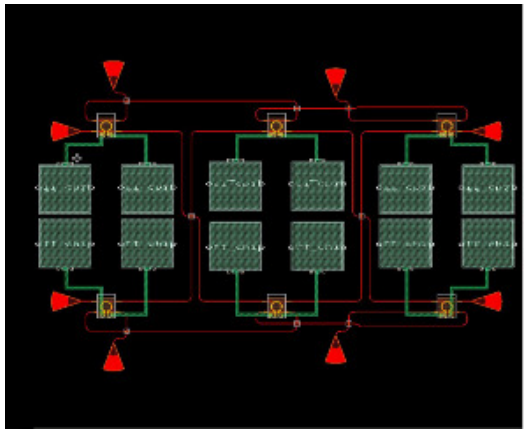
Expand the User Base for IC Designers

LightSuite Photonic Compiler – Schematic Driven Layout Flow

- Schematic Driven Layout flow
- Small python script
- Limited control
  - — schematic defines layout
    - – Relative placements
    - – Connectivity



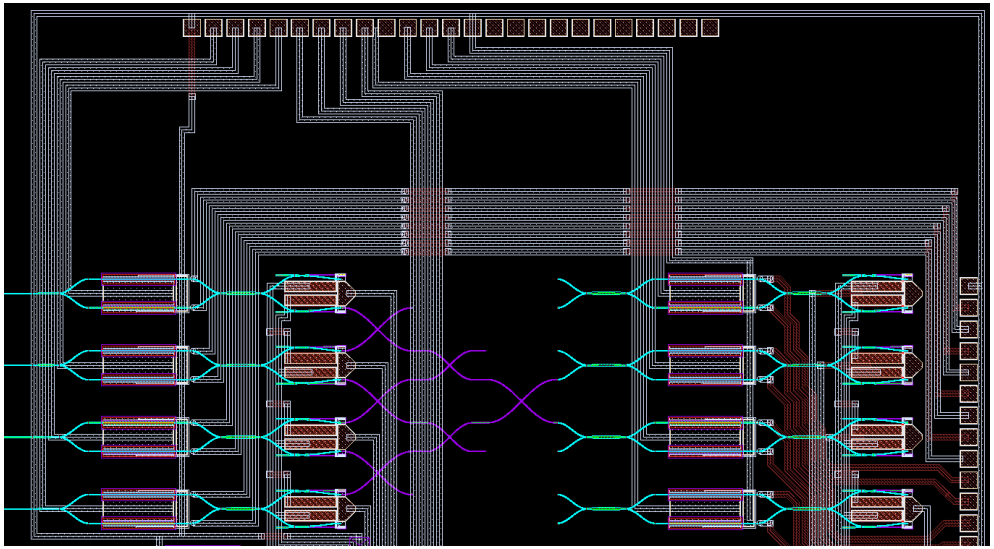




LightSuite Photonic Compiler

Examples in Design

- Close to 400 components
- Placed & routed - DRC clean
- 9 minutes vs approximately 2 weeks for manual layout



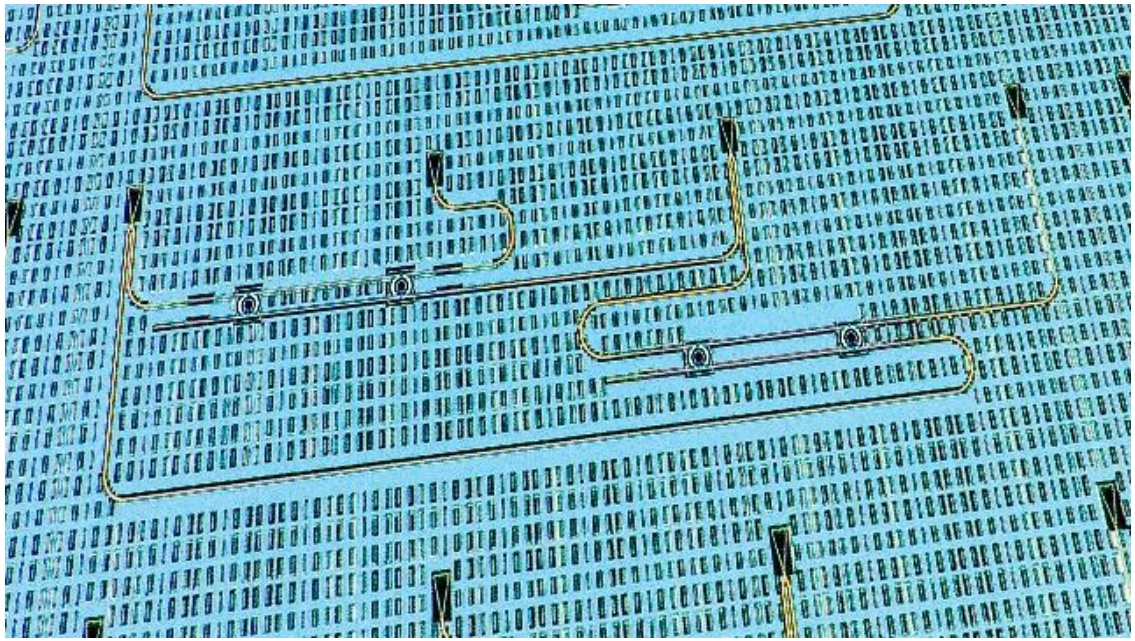
- Placed and routed 66,000 components in just under 11 hours, DRC clean

LightSuite Photonic Compiler

Success Story

Hewlett Packard Enterprise

"LightSuite Photonic Compiler fixes the biggest roadblocks preventing industry-wide adoption of electro-optical design and simulation of photonic chips.
Photonic chips promise amazing performance, but designing circuits today is just too difficult and requires specialized knowledge. LightSuite Photonic Compiler circumvents those challenges and enables scalability. I'm thrilled to have worked with Mentor to develop this tool to make it possible for anyone to design and build photonic circuits as easily as designing electronic circuits."



Ashkan Seyedi, Research Scientist
Hewlett Packard Enterprise

Mentor® A Siemens Business

PHYSICAL VERIFICATION TOOLS

Physical Verification

eqDRC – addressing DRC Photonics Challenges

- Concentric arcs:
  - Fabrication constraint :

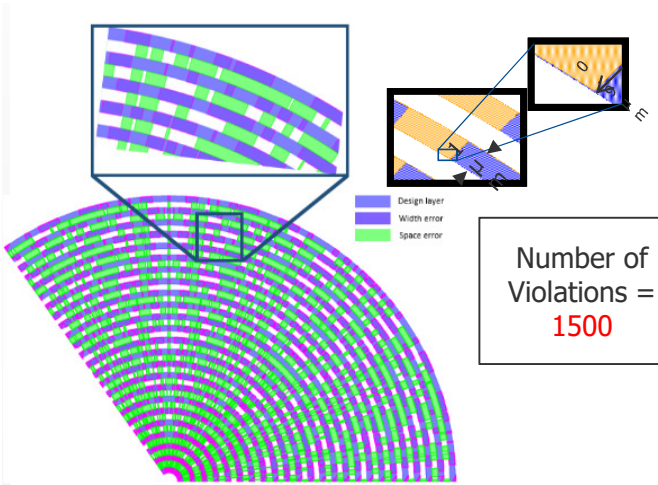
Width > 1 µm, Space > 1 µm

Error_width := width < 1 µm
Error_space := space < 1 µm
} Traditional DRC Check

New DRC Check using Calibre eqDRC

All_Thin_rod := Width (rod) < 1 µm
W = Width (Thin_rod_width)
α = Angle (Thin_rod_width)
L = Length (thin_rod_width)
If (0 < α < max_angle) OR (L < max_length)
Then:
Error_rod_width := Width(rod) < (1 -tol*) µm
Else:
Error_rod_width := Width(rod) < max_width µm

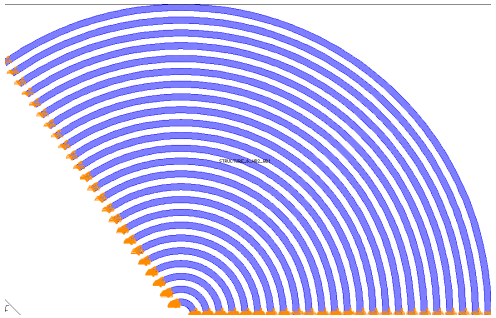
*.tol tolerance determined by applying tolerance factor according to fabrication grids and DRC rounding factors. (2sqrt(2). Grid)



Concentric Arcs with DRC violations

Number of Violations = 1500

Number of Violations = 145



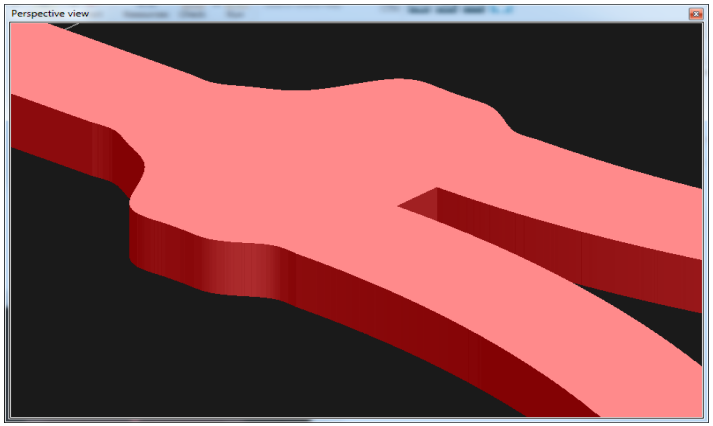
DRC Post Processing using EqDRC capabilities

"*Silicon Photonics Design Rule Checking:Application of a Programmable Modeling Engine for Non-Manhattan Geometry Verification*", presented at *VLSI-SoC 2014*

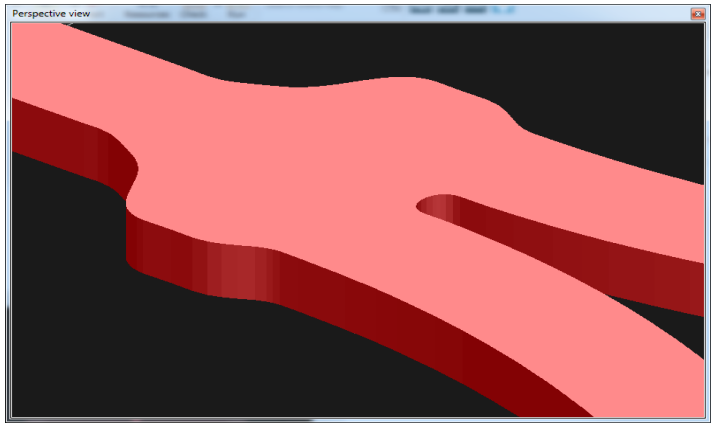
Physical Verification

Calibre LFD Workflow

- Lithographic processes will distort drawn shapes in silicon
- Designers use Calibre LFD software with to simulate the process and improve their designs with respect to manufacturability.



As Drawn



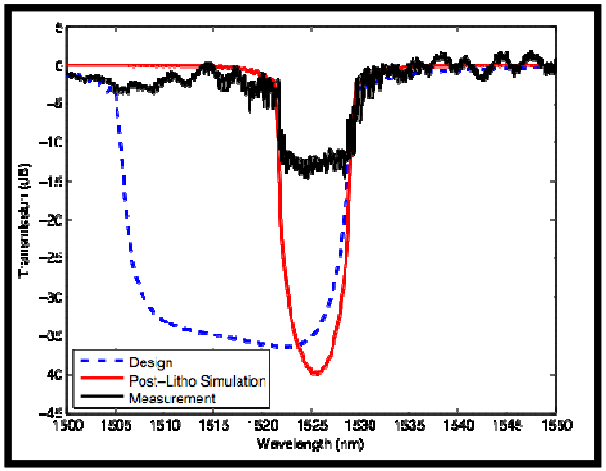
Simulated as Manufactured

Significantly Reduce Manufacture Iteration through Simulation

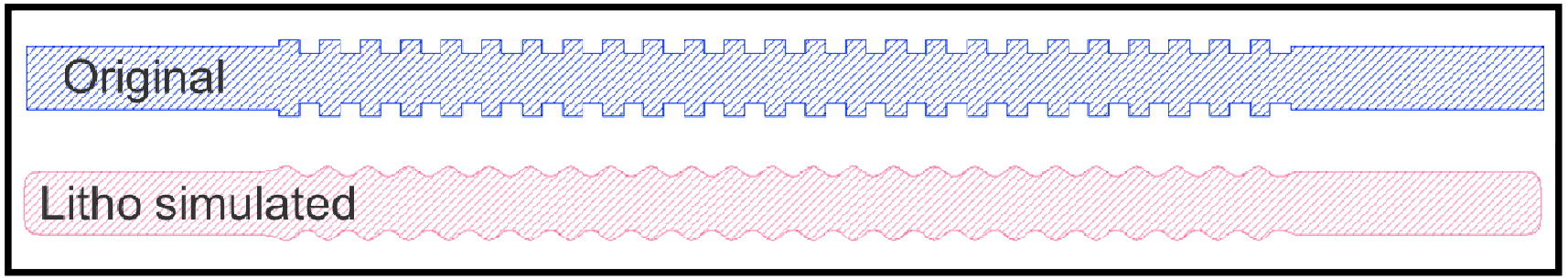
Physical Verification

Impact of Lithography on Silicon Photonics

- Modeled layout passed to simulation
  - Updated S-parameters
- Updated FDTD Simulations match measured data



Xu Wang, e al., "Lithography Simulation for the Fabrication of Silicon Photonic Devices with Deep-Ultraviolet Lithography", *IEEE GFP*, 2012



Mentor's Photonic Design Flows

Automated and Manual

Schematic Driven Automated Flow

Tanner Design (S-Edit)
Schematic Capture

LUCEDA PHOTONICS CAPHE
VPIphotonics VPI-TC
lumerical INTERCONNECT
Optiwave OptiSpice

LightSuite Photonic Compiler
Photonic Layout Automation
Calibre RealTime Custom

L-Edit Photonics
Or any OA based Layout Editor

Calibre nmDRC, nmLVS
Physical Verification

Script Driven Automated Flow

LightSuite Photonic Compiler
Photonic Layout Automation
Calibre RealTime Custom

LUCEDA PHOTONICS CAPHE
VPIphotonics VPI-TC
lumerical INTERCONNECT
Optiwave OptiSpice

L-Edit Photonics
Or any OA based Layout Editor

Calibre nmDRC
Physical Verification

Schematic Driven Manual Flow

Tanner Design (S-Edit)
Schematic Capture

LUCEDA PHOTONICS CAPHE
VPIphotonics VPI-TC
lumerical INTERCONNECT
Optiwave OptiSpice

L-Edit Photonics (L-Edit IC)
Photonic Circuit Design

Calibre nmDRC, nmLVS
Physical Verification

Layout Centric Manual Flow

L-Edit Photonics
Photonic Circuit Design

LUCEDA PHOTONICS CAPHE
VPIphotonics VPI-TC
lumerical INTERCONNECT
Optiwave OptiSpice

Calibre nmDRC
Physical Verification

Photonic PDKs, iPDK's + Calibre Rule Files + Partner Simulation Models

FOUNDRY SUPPORT

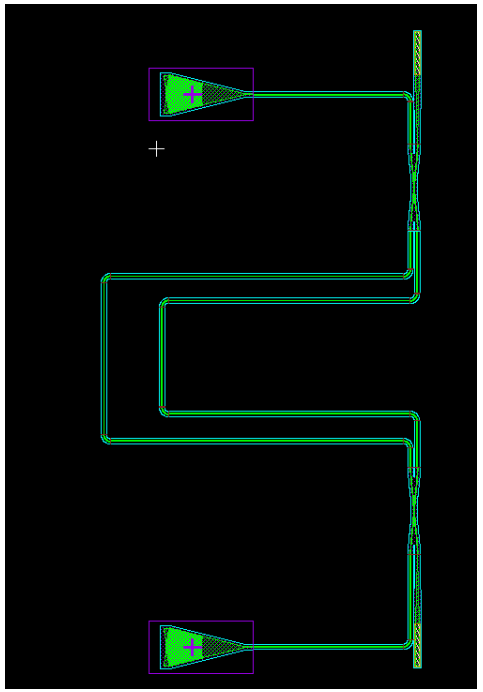
CEA-Leti PDK on Mentor Flow

- Passive components
  - Waveguides
    - Bends, Sbend, Sticks
    - Crossings
    - Tapers
  - MMI, directional coupler
  - Grating couplers
- Active components
  - Ring modulators
  - Photo detector
- PDK support both
  - LightSuite Photonic Compiler
  - L-Edit Photonics

L-Edit Photonics Support

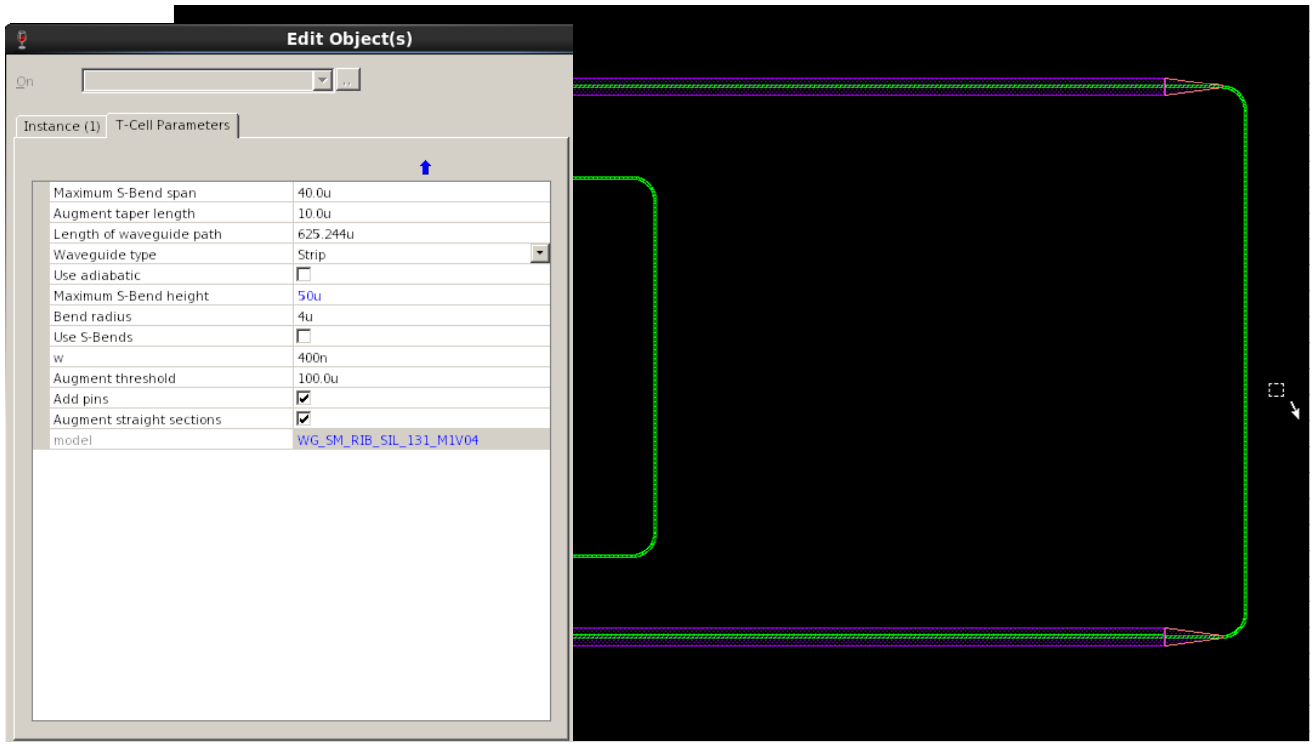
Manual Layout with CEA-Leti PDK

- Stand alone photonic design with L-Edit
- L-Edit Photonics features configured in CEA-Leti PDK
  - Hierarchical waveguide P-Cell creation/conversion and editing
  - Crossing element insertion
  - Exports simulation netlist
- Focused on layout centric design
  - Schematic optional



Hierarchical Waveguide P-Cell

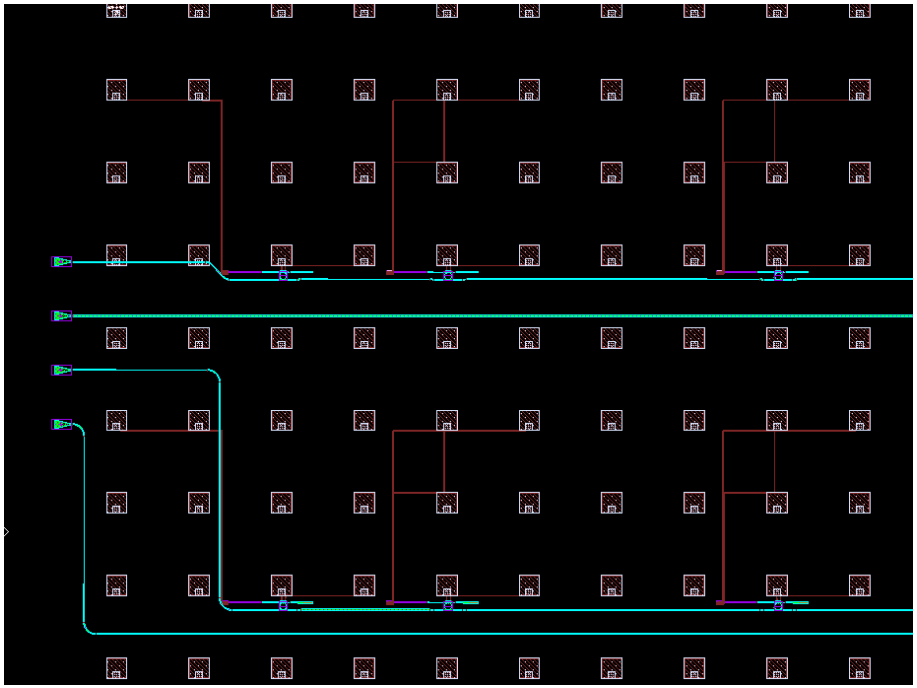
- Uses CEA-Leti components for waveguide routing
- Automatic cladding based on lengths
  - Taper insertion
- Controllable length

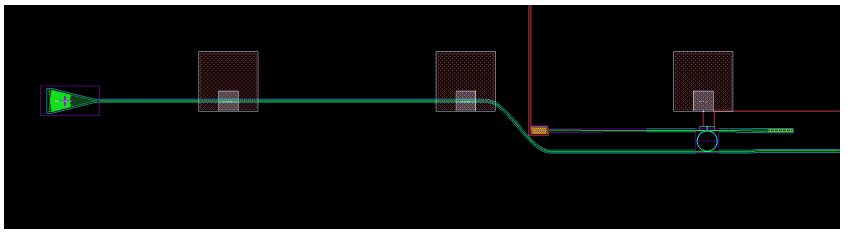


LightSuite Photonic Compiler Support

Script Driven Flow with CEA-Leti PDK

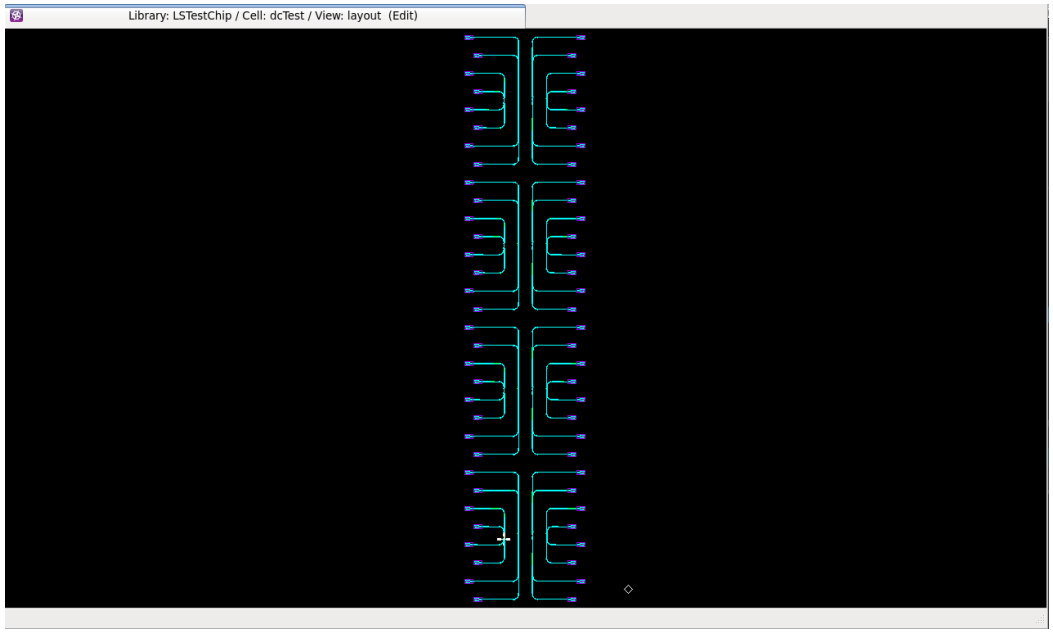
- Places components from the CEA-Leti PDK
- Routes both photonic waveguides and electrical nets
- Designer to setup P&R with Python IDE
  - Rapidly produces a new layout
- Produces a DRC correct design
  - Correct by Calibre
  - Requires Calibre RealTime license
  - eqDRC based SVRF rules

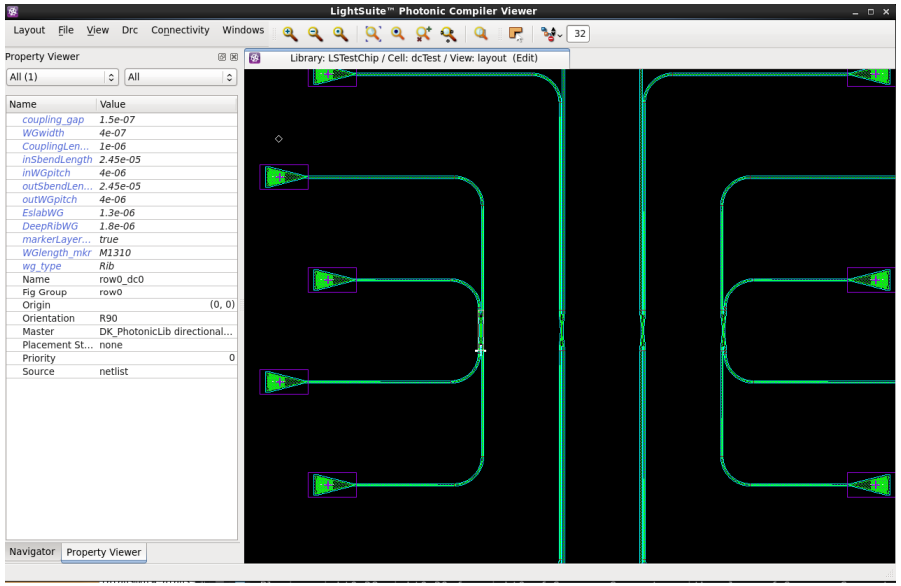




LightSuite Photonic Compiler

Test Chip Flow with CEA-Leti PDK





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