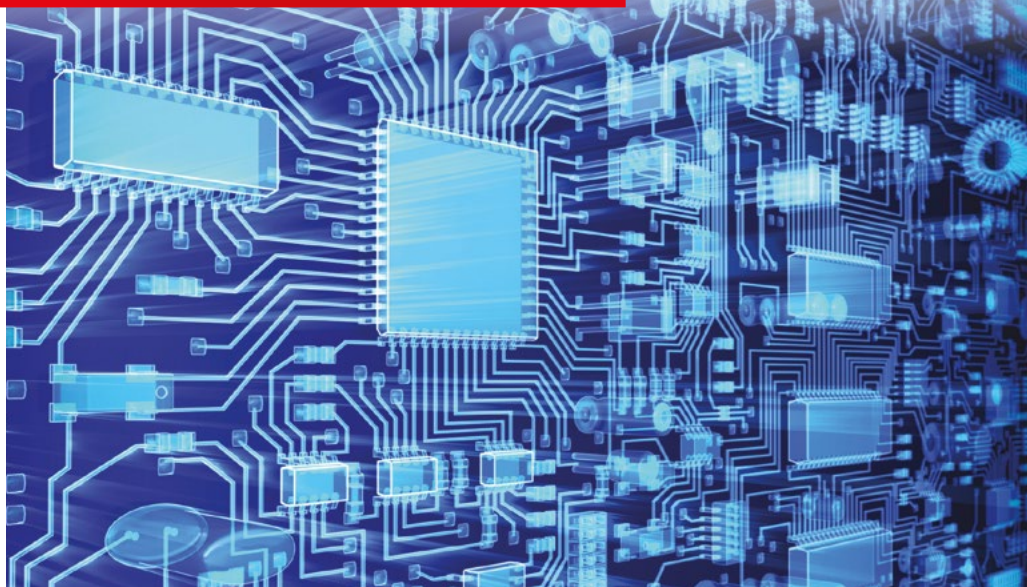


leti
cea tech

MICRO- ELECTRONICS

At the heart
of emerging applications



Leti, technology
research institute

Contact:
leti.contact@cea.fr

What about Moore's Law?

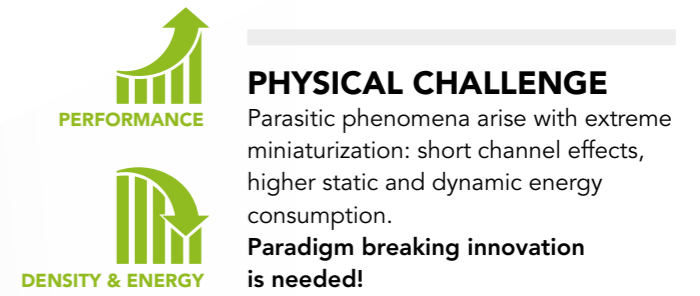
Microelectronics and technology downscaling are in high demand for developing ultra-low power solutions for future IoT and disruptive computing. They enable groundbreaking innovation in application domains such as healthcare, smart cities and mobility, logistics and manufacturing, and energy.

Computers have transformed society in the last 50 years, through downscaling of transistors and storage devices in keeping with Moore's law (doubling of transistor density every 2 years at constant cost).

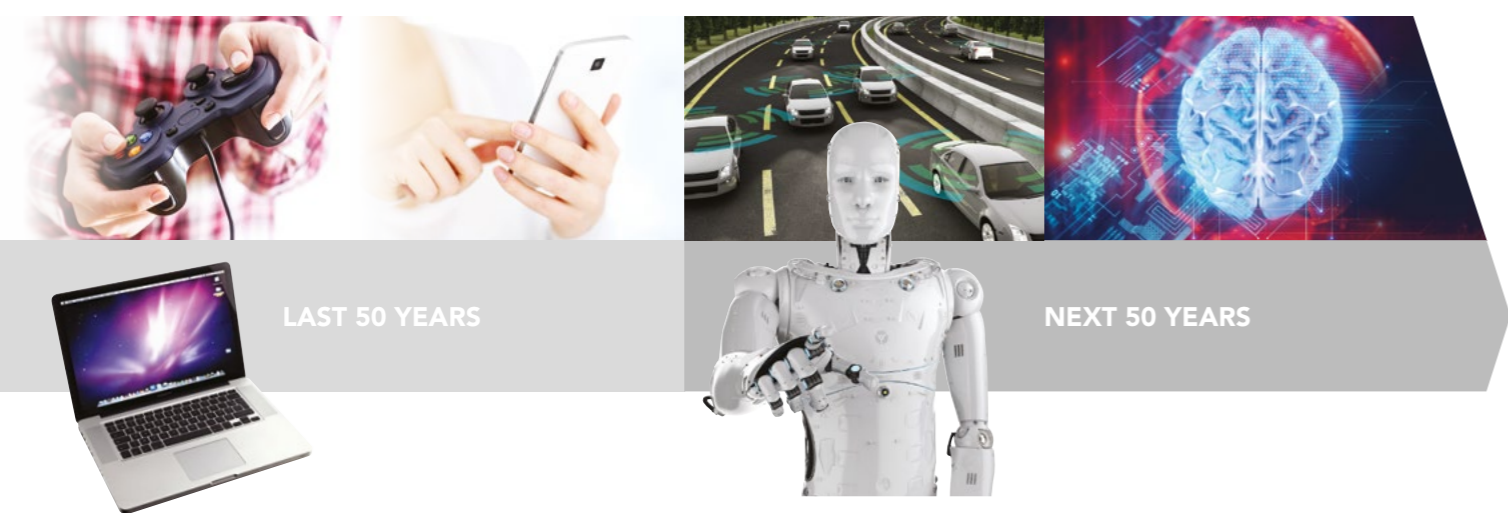
Transistor miniaturization has been the main catalyst of semiconductor market growth. 2D-planar integration has cut integrated circuit cost, while increasing operating speed.

However, extreme size reduction generates **parasitic phenomena**: short channel effects, greater variability, increased static and dynamic energy consumption. To address these issues, **new materials** have been introduced (for the gate, the channel and the contact access) **and architectural changes** have been proposed (SOI transistors, double gate, multi-channel transistors, FinFETs, etc.).

The number of transistors integrated into chips and their interconnection distance continues to increase. However, delays at interconnections limit integrated circuits performance, thereby reducing the benefits of unit transistor performance enhancement. To improve the situation, aluminium was replaced by lower resistance copper, less resistive, and dielectric insulators were made porous. This scaling law is now reaching its limits and system-on-chip integration is moving towards heterogeneity.



ECONOMIC CHALLENGE
Higher process development cost and fewer players for leading edge nodes. **Major investment need in shared R&D of scaling alternatives!**

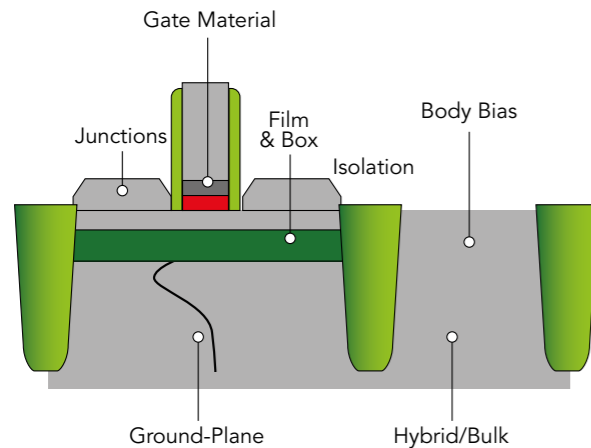


COMPUTERS HAVE TRANSFORMED SOCIETY IN THE LAST 50 YEARS, THROUGH DOWNSCALING OF TRANSISTORS AND STORAGE DEVICES IN KEEPING WITH MOORE'S LAW...

LETI'S OFFER

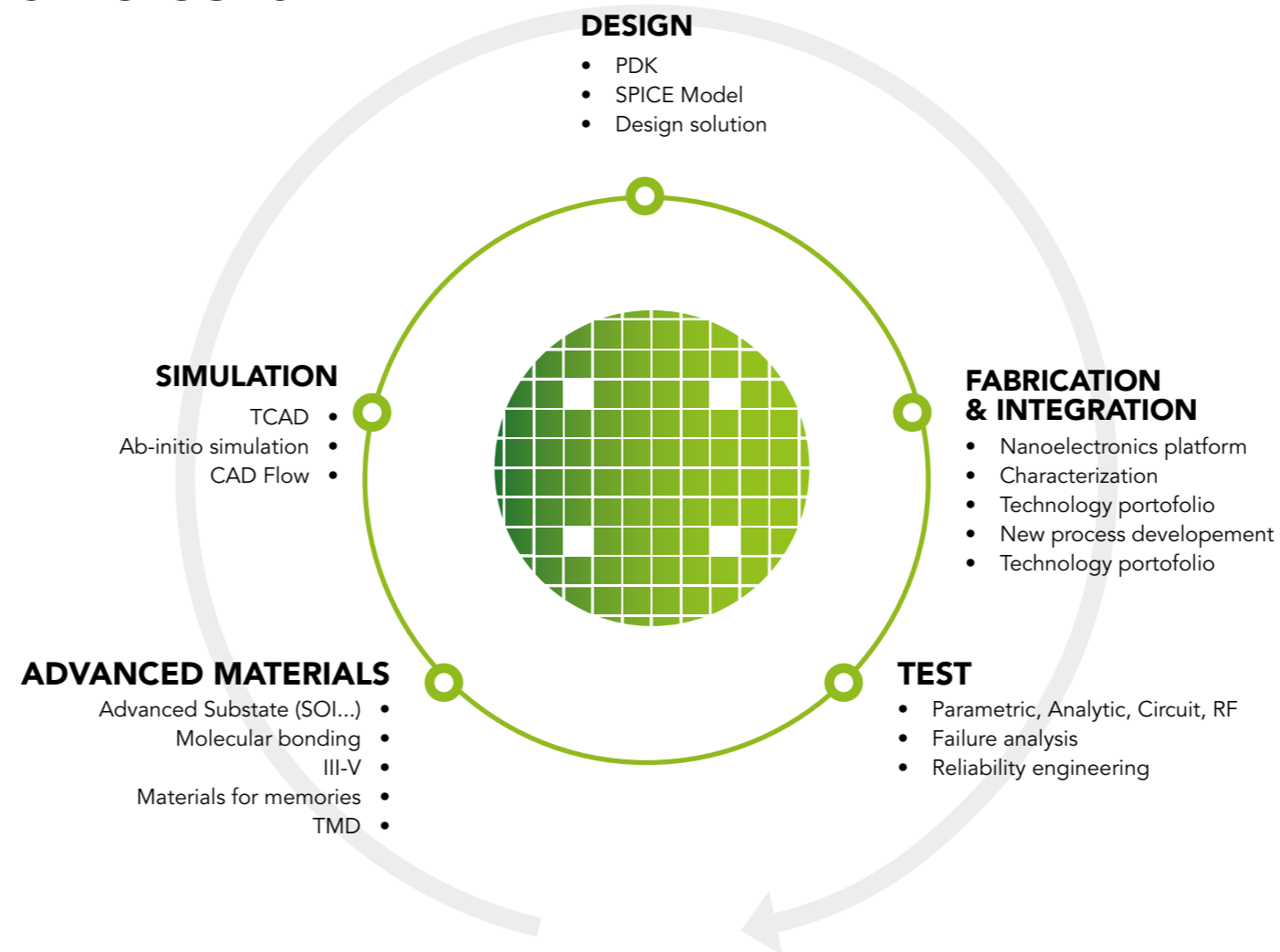
A COMPLETE PROTOTYPE BUILDING TOOLBOX USING MOST ADVANCED TECHNOLOGIES

Leti has invested heavily and for many years in its place as a premier research institute worldwide. It is now home to hi-tech microelectronics cleanrooms, a range of advanced characterization tools that are unique in the world. As a world leader in innovation, Leti focuses on energy efficient technologies offering performance/cost trade-offs to provide the European ecosystem with alternative differentiated solutions.



LETI: A PIONEER OF FDSOI TECHNOLOGY

Fully Depleted Silicon On Insulator thin film technology provides major benefits for future advanced technological nodes. Thin silicon film technology ensures electrostatic gate control of the transistor channel. This control is much better than that provided by conventional architectures. Leti is recognized as an FDSOI center of competence worldwide with its 30-year R&D heritage.



8" & 12" NANO-ELECTRONICS PLATFORM

Nanoelectronics platform develops advanced transistors, integrated circuits and non-volatile memory. It is also where FDSOI—today used to mass-produce chips worldwide—was born. The platform also conducts 3D integration R&D.

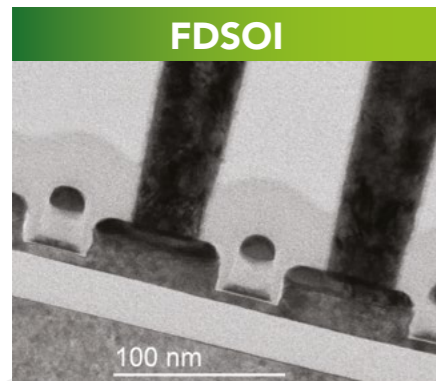
8,500 sq. m
of clean rooms

70
patents filed per year

€25 million
annual investment

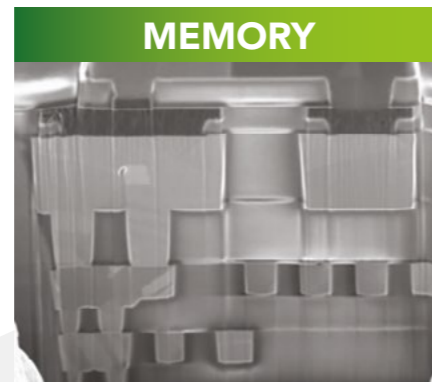
TECHNOLOGY PORTOFOLIO

TECHNOLOGICAL INNOVATION FOR PERFORMANCE AND ADDED VALUE



Low variability planar multi- v_{th} technology

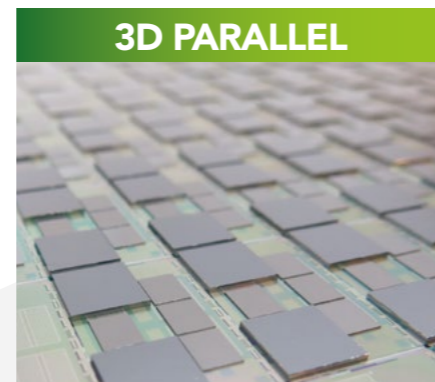
- High-k metal gate: V_{th} and low gate leakage
- Multistep implantation
- Undoped thin body
- Back implementation: static and dynamic VT adjustment
- Box: total dielectric isolation, extended body biasing



Memory Advanced Demonstrator (MAD)

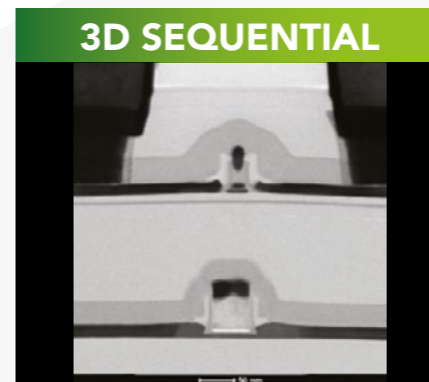
Early Stage Vehicle Technology Assessment

- Advanced materials integration
- 1T-1R from single bit to Mbit arrays
- BEOL selectors
- Innovative designs: Crossbar, Neuromorphic, TCAM
- Memory point scaling down to 40 nm
- Modeling & Simulation
- Test & Characterization
- Cycle time: 3 months



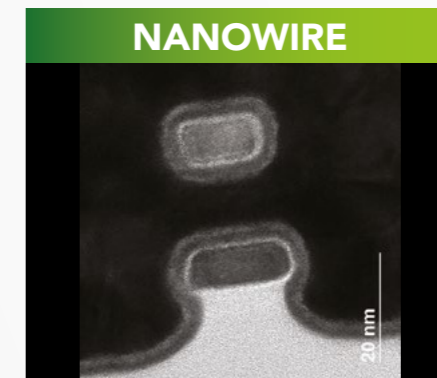
TSV and hybrid bonding

- Fine pitch and cost competitive approach for 3DVLSI integration.
- 3D offer embracing TSV and hybrid bonding
- Next stage: Wafer-to-Wafer and Chip-to-Wafer prototyping services (including self-assembly)



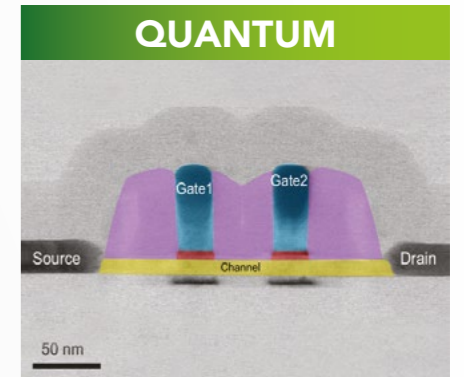
CoolCube™

- Cold (500°C) top tier process with state-of-the-art performance demonstrated
- Low cost process under assessment
- Inter Metal Levels available
- Full low T° route established
- Dedicated MPW MaskSet is running, next PG open for design/circuit collaboration
- Technology ready for transfer to fab for manufacturing qualification



SOI and bulk intergration

- Original process integration of stacked nanowire
- Gate last and self aligned contact
- Strain development
- Strain characterization
- Compact model: Leti-NSP nanowire



Si Qubits

- 1st demonstration of Silicon Spin Qbits 300mm CMOS compatible
- Fabrication and characterization of elementary cells for a quantum computer based on Silicon CMOS
- Control of multi-qubit devices and basic quantum algorithms
- Cryogenic CMOS electronics for Qbit control



ABOUT LETI

Leti is a technology research institute at CEA Tech and a recognized global leader in miniaturization technologies enabling smart, energy-efficient and secure solutions. Committed to innovation, its teams create differentiating solutions for Leti's industrial partners.

By pioneering new technologies, Leti enables innovative applicative solutions that ensure competitiveness in a wide range of markets. Leti tackles critical, current global issues such as the future of industry, clean and safe energies, health and wellness, safety & security...

Leti's multidisciplinary teams deliver solid micro and nano technologies expertise, leveraging world-class pre-industrialization facilities.

For more than 50 years, the institute has been building long-term relationships with its industrial partners providing tailor-made solutions and a clear intellectual property policy.

Leti, technology research institute

Commissariat à l'énergie atomique et aux énergies alternatives

Minatéc Campus | 17 avenue des Martyrs | 38054 Grenoble Cedex 9 | France

www.leti-cea.com

